Comment i-423

PROPOSED ACCEPT IN PRINCIPLE

Multiple editorial changes are required in both the PCS Receive and PCS Transmit functions subclauses to address the lack of clarity pointed out by the commenter.

147.2.2.2 When generated

The PCS generates PMA_UNITDATA.request (tx_sym) synchronously with every ~~PCS transmit clock cycle~~ symb_timer expiration. The symb_timer is defined in 147.3.2.7.

147.3.2 PCS Transmit

Globally replace in this clause all occurrences of:

- pcs_txen with TX_EN
- pcs_txer with TX_ER
- pcs_txd with TXD

NOTE: this includes all occurrences in figures 147-4 and 147-5.

147.3.2.2 Variables

tx_sym

5B symbol to ~~transmit~~ be conveyed to the PMA Transmit function by the means of the PMA_UNITDATA.request primitive specified in 147.2.2.~~, generated from the MII data or directly passed from tx_cmd in SILENT state when optional PLCA reconciliation sublayer is implemented.~~

147.3.2.4 Function

ENCODE

~~In the PCS transmit process, this function takes as its arguments 4 bits of input data, scrambles it as defined in 147.3.2.6 and returns the corresponding 5B symbol as defined in Table 147–1.~~

This function takes a 4 bit input parameter Sc_n<3:0> and returns a 5B symbol according to the following procedure:

1. Convert Sc_n<3:0> into Sd_n<3:0> as specified in 147.3.2.6.

2. Convert Sd_n<3:0> (4B symbol) into the corresponding 5B symbol defined in Table 147-1.

147.3.2.5 Abbreviations

STD

Alias for 5B symbol timer done~~., synchronous to PCS TX clock~~

147.3.2.6 Self-synchronizing scrambler

An implementation of a self-synchronizing scrambler by a linear-feedback shift register is shown in Figure 147–6. The bits stored in the shift register delay line at time n are denoted by Scrn<16:0>. The '+' symbol denotes the exclusive OR logical operation. ~~At every MII clock cycle, for every bit of TXD[3:0], the scrambler is advanced by one bit, and the output bit Sdn[i] represented by the exclusive-OR of Scrn[13], Scrn[16] and TXD[i] is shifted in as a new Scrn[0], with i ranging from 0 to 3 (i.e., LSB first)~~ When Sc_n<3:0> is presented at the input of the scrambler, Sd_n<3:0> is produced by shifting-in each bit of Sc_n<3:0> as Sc_n<i>, with i ranging from 0 to 3 (i.e., LSB first). The scrambler is reset upon execution of the PCS Reset function. If the PCS Reset is executed, all bits of the 17-bit vector representing the self-synchronizing scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeroes. At every STD, if no data is presented at the scrambler input via Sc_n<3:0>, the scrambler may be fed with arbitrary inputs.

147.3.2.7 Timers

Insert the following text:

symb_timer

A continuous free-running timer. PMA_UNITDATA.request messages are issued by the PCS concurrently with symb_timer_done (see 147.2.2).

Continuous timer: The condition symb_timer_done becomes true upon timer expiration.

Restart time: Immediately after expiration, timer restart resets the condition symb_timer_done.

Duration: 400 ns ± 100 ppm (see 22.2.2.1)

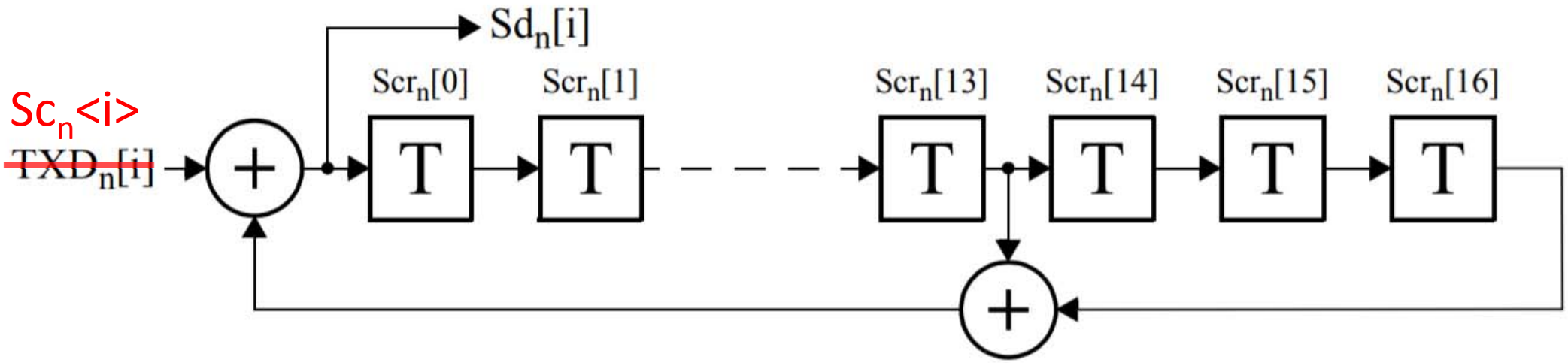

Figure 147–6—Self-synchronizing scrambler

Additionally, change all square brackets ‘[]’ with angular brackets ‘<>’

147.3.3 PCS Receive

Globally replace in this clause all occurrences of:

- pcs_rxdv with RX_DV
- pcs_rxer with RX_ER
- pcs_rxd with RXD

NOTE: this includes all occurrences in figures 147-7 and 147-8.

147.3.3.2 Variables

RX_n

~~Received 5B symbol generated by PMA receive at time n.~~

The rx_sym parameter of the PMA_UNITADATA.indication primitive defined in 147.2.1. The ‘n’ subscript denotes the rx_sym conveyed in the most recent recv_symb_conv_timer cycle. The ‘n-x’ subscript indicates the rx_sym conveyed ‘x’ cycles behind the most recent one.

147.3.3.4 Functions

DECODE

~~In the PCS Receive function, this function takes as its arguments one 5B symbol, decodes the corresponding nibble as defined in Table 147–1, descrambles it as defined in 147.3.3.7, and returns the descrambled result as defined in 147.3.3.7. If a violation of the encoding rules is detected, PCS Receive asserts the signal RX_ER for at least one symbol period.~~

This function takes a 5B symbol input parameter and returns a 4 bit value Dc_n<3:0> value according to the following procedure:

1. Convert the 5B input symbol into Dr_n<3:0> by performing a reverse lookup of Table 147-1. If no 4B value is associated to the given 5B symbol, the PCS Receive function shall assert RX_ER for at least one symbol period and Dr_n<3:0> may be set arbitrarily.

2. Convert Dr_n<3:0> to Dc_n<3:0> as specified in 147.3.3.7.

147.3.3.5 Abbreviations

RSCD

~~Alias for Receive Symbol Conversion Done, synchronous to PCS RX clock.~~

Alias for recv_symb_conv_timer_done.

Insert new subclause 147.3.3.x between 147.3.3.7 and 147.3.3.8 named Timers

with the following text:

recv_symb_conv_timer

A continuous timer which expires when the PMA_UNITDATA.indication message is generated (see 147.2.1).

Continuous timer: The condition recv_symb_conv_timer_done becomes true upon timer expiration.

Restart time: Immediately after expiration, timer restart resets the condition recv_symb_conv_timer_done.

Duration: timed by the PMA_UNITDATA.indication message generation.

147.3.3.7 Self-synchronizing descrambler

The PCS Receive function ~~shall~~ descrambles the 5B/4B decoded data stream and returns the ~~proper nibble for generation~~ value of RXD[3:0] to the MII. The descrambler shall employ the polynomial defined in 147.3.2.6. The implementation of the self-synchronizing descrambler by linear-feedback shift register is shown in Figure 147–9. The bits stored in the shift register delay line at time n are denoted by Dcrn[16:0]. The '+' symbol denotes the exclusive OR logical operation. ~~At every MII clock cycle, each bit of Drn[3:0] is shifted in as new Dcrn[0], and the descrambler is advanced by one bit. The output bit RXD[i] represented by the exclusive-OR of Dcrn[13], Dcrn[16], and Drn[i] is generated~~When Dr_n<3:0> is presented at the input of the descrambler, Dc_n<3:0> is produced by shifting-in each bit of Dr_n<3:0> as Dr_n<i>, with i ranging from 0 to 3 (i.e., LSB first). The descrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all the bits of the 17-bit vector representing the self-synchronizing descrambler state are arbitrarily set. The initialization of the descrambler state is left to the implementer. At every RSCD, if no data is presented at the descrambler input via Dr_n<3:0>, the descrambler may be fed with arbitrary inputs.

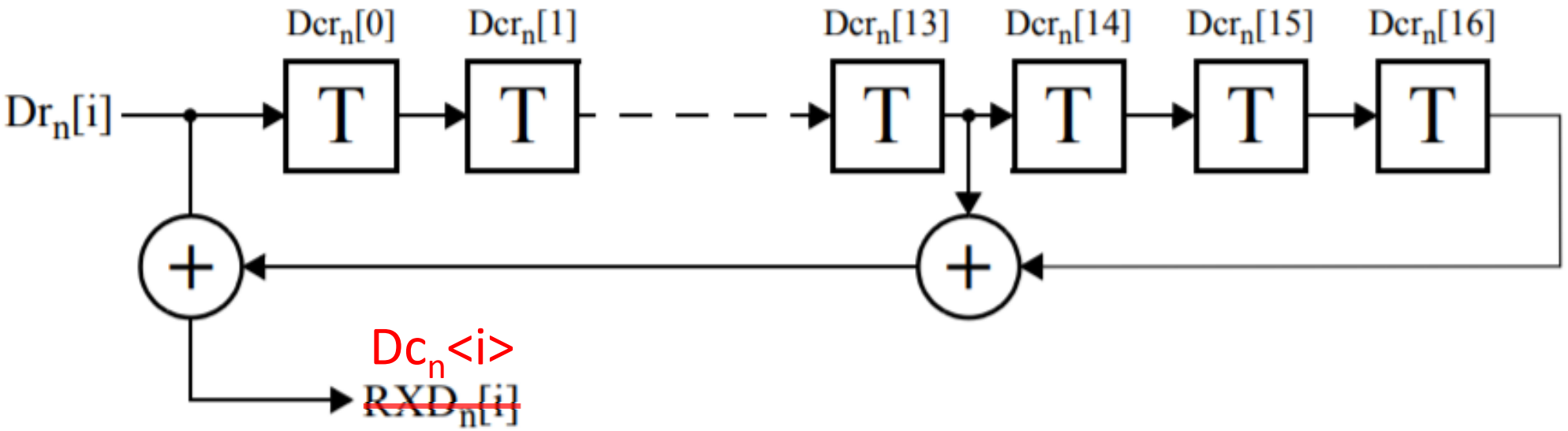

Figure 147–9—Self-synchronizing descrambler

Additionally, change all square brackets ‘[]’ with angular brackets ‘<>’

147.4.3 PMA Receive function

The PMA Receive function recovers encoded clock and data information from the DME encoded stream received at the MDI.

The clock recovery provides a synchronous clock for sampling the signal on the pair. While it may not drive the MII directly, the clock recovery function is the underlying root source of RX_CLK.

Note that in order to meet the specifications of 147.5.5.1, the PMA Receive function should achieve proper synchronization on both the DME stream and the 5B boundary within 1.2 us.