10 Mb/s Single Twisted Pair Ethernet

10BASE-T1L Changes

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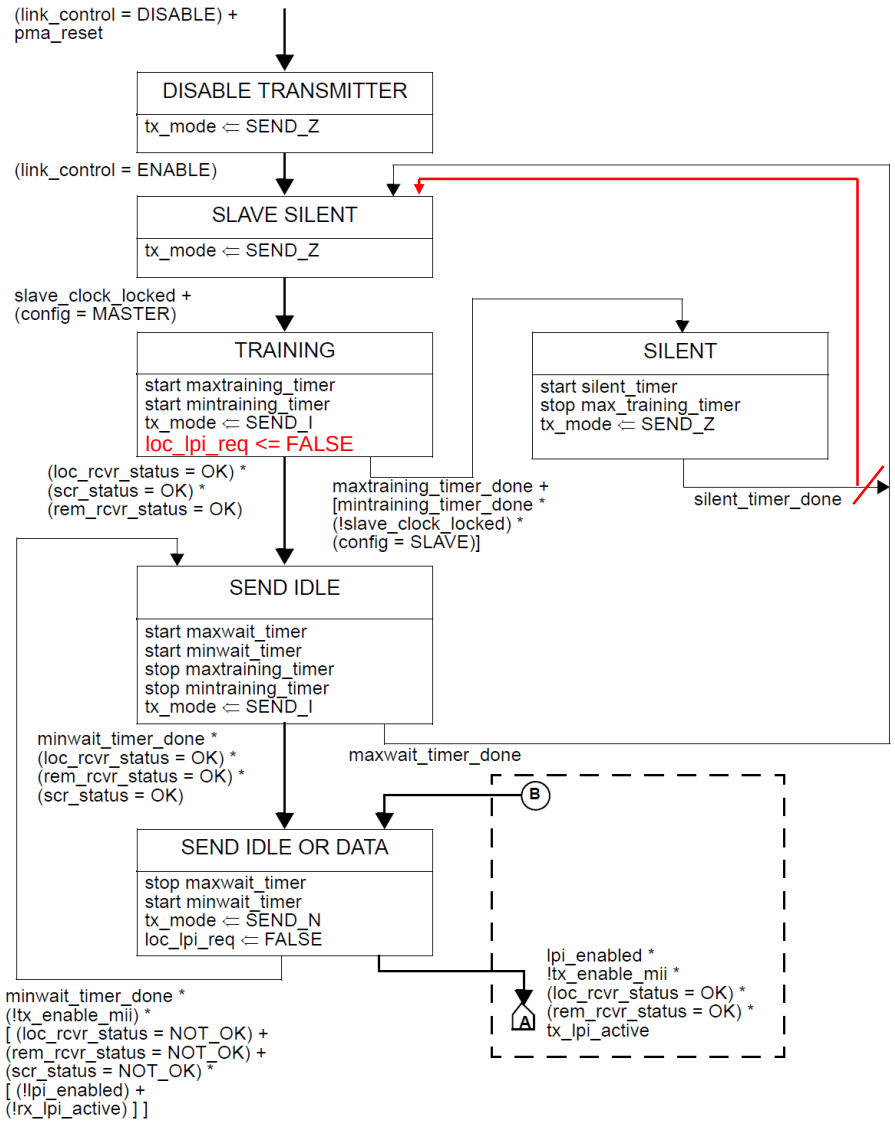
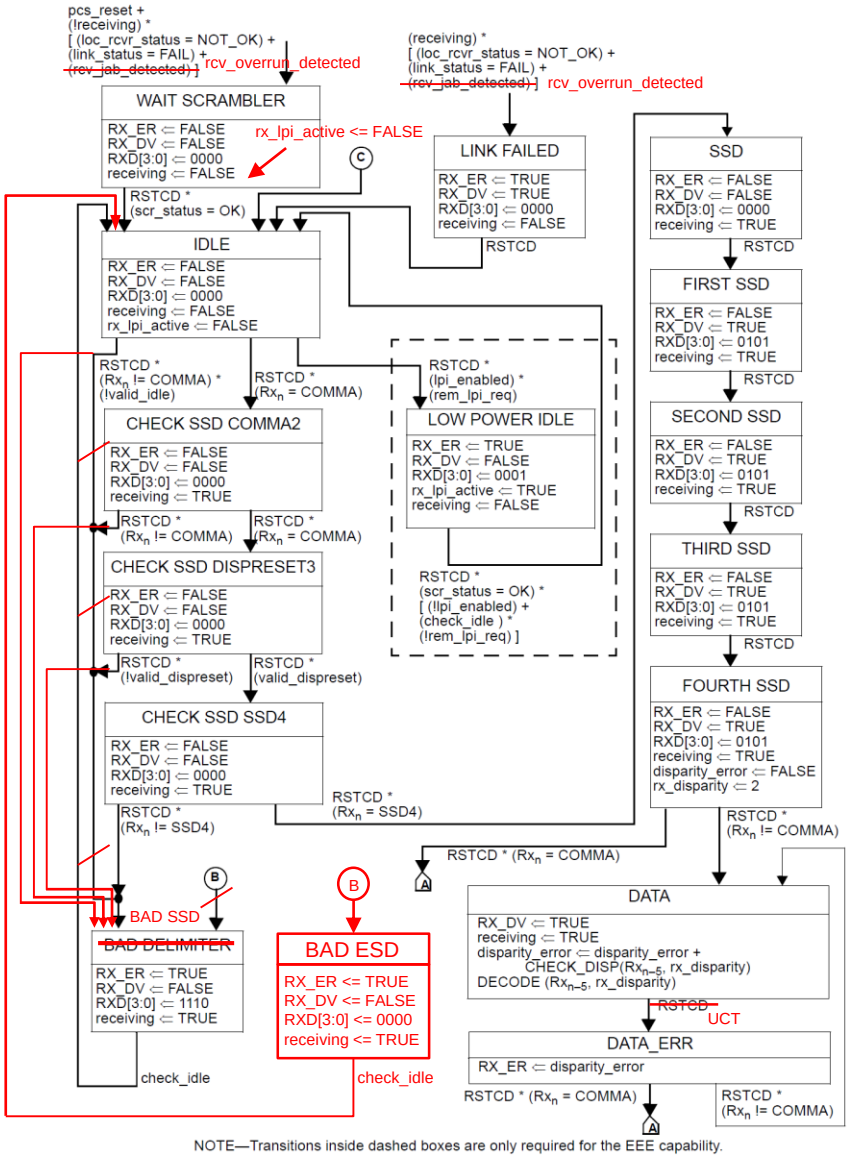
PHY Control State Diagram Changes



- Move arc of SILENT state exit condition directly to SLAVE SILENT state (editorial style correction).
- Initialize “loc_lpi_req“ variable the first time the PHY starts to transmit data (otherwise having “loc_lpi_req” uninitialized the remote PHY may accidently initially be signaled to go into LPI mode).
- This is necessary because “loc_lpi_req” is used in the PCS scrambler definition, which can change the SEND_I encoding used in SEND IDLE.”

PCS Receive State Diagram Changes



- Variable “rx_lpi_active” needs to be initialized at the beginning of the state diagram. This variable is used by PMA Receive, which otherwise could accidently switch the receiver into low power idle state.
- Currently reception of a bad SSD as well as a bad ESD both ends up in BAD DELIMITER state. Within this state a False Carrier Indication is signaled over the MII.
- A False Carrier Indication in other IEEE802.3 clauses is only provided when receiving a bad SSD encoding, not a bad ESD encoding.
- Thus the BAD DELIMITER state needs to be splitted into two separate states: BAD SSD, which is executed when receiving a bad SSD and thus providing a False Carrier Indication over the MII and BAD ESD, which is executed when receiving a bad ESD and thus not providing a False Carrier Indication over the MII.
- Change variable name “rcv_jab_detected” to “rcv_overrun_detected” (this was missed in D3.0).
- Change the “RSTCD” condition to an “UCT” condition between DATA and DATA_ERR states,
- The other changes are related to editorial style.

LPI Timing Changes

- The following timings are estimated for a 10BASE-T1L PHY:

Time	Description
0.5 µs	TX PCS Latency (minimum latency of the PCS transmit path).
10 µs	TX AFE/DSP Stabilize Time (time to enable and stabilize the AFE and initialize the transmit filter).
10 µs	RX Signal Energy Detection Time (time the RX AFE needs to detect if there is signal energy on the link segment).
30 µs	RX Signal Detect and AFE/DSP Stabilize Time (shorter for an ASIC implementation) (time to enable and stabilize the AFE and initialize the DSP in the PMA).
100 µs	RX Clock Readjustment Time (time provided to readjust the clock after the quiet phase).
100 µs	RX Filter Training Time (for an ASIC implementation this may be as low as 50 µs) (time provided during refresh to do a short FSE, DFE and EC filter training).
0.5 µs	RX PCS Latency (minimum latency of the PCS receive path).
20 µs	Time to reliably detect the wake indication within the idle data stream.

- These numbers also include an estimate for a possible implementation in a high speed MCU, which, compared to an ASIC implementation may need some additional time during initialization and training.

LPI Timing Changes

- The timings shown on the previous slide will then convert to the following wake timings:

Parameter	New Time	D3.0 Time	Description
$T_{phy\_wake\_tx}$	10.5 µs	---	TX PCS Latency + TX AFE/DSP Stabilize Time
$T_{phy\_shrink\_tx}$	**10 µs**	10 µs	$T_{phy\_wake\_tx}$ - $T_{phy\_prop\_tx}$ (TX PCS Latency)
$T_{phy\_wake\_rx}$	240.5 µs	---	RX Signal Energy Detection Time + RX Signal Detect and AFE/DSP Stabilize Time + RX Clock Readjustment Time + RX Filter Training Time + RX PCS Latency
$T_{phy\_shrink\_rx}$	**240 µs**	220 µs	$T_{phy\_wake\_rx}$ - $T_{phy\_prop\_rx}$ (RX PCS Latency)
$T_{w\_sys\_rx}$	**20 µs**	220 µs	Time to reliably detect the wake indication within the idle data stream.
$T_{w\_sys\_tx}$	**270 µs**	220 µs	$T_{w\_sys\_rx}$ + $T_{phy\_shrink\_tx}$ + $T_{phy\_shrink\_rx}$
T_{w_phy}	**250.5 µs**	220 µs	$T_{phy\_wake\_rx}$ + $T_{phy\_shrink\_tx}$

- The parameters in bold in the table above are the suggested values for 10BASE-T1L in Table 78-4.
- $T_{w\_sys\_rx}$ is changed significantly compared to the value in D3.0. This is needed due to an erroneous value for $T_{w\_sys\_rx}$ in D3.0, the other timing values are adapted based on the timing estimates on the previous slide.
- Summing the LPI timings of the table on the previous slide (without the PCS latencies and wake indication time), this results in a refresh time of **T_r = 250 µs** (2500 bit times or 625 triple ternary symbols).
- Suggestion for the sleep time is to keep it identical with the refresh time and also set it to **T_s = 250 µs.**
- Suggestion for the quiet time is to keep it as **T_q = 6000 µs** (60 000 bit times or 15 000 triple ternary symbols).
- Suggestion is to also remove the tolerances currently in D3.0 to provide an exact timing (as there is an exact quiet/refresh cycle, it may be easier to synchronize the LPI cycles between both PHYs).

LPI Timing Changes

- The LPI timings currently stated in draft D3.0 result in a refresh to quiet ratio of **$T_r : T_q = 1 : 30$**.
- The new suggested LPI timings result in a refresh to quiet ratio of **$T_r : T_q = 1 : 24$**.

- Background for this change is, that as a 10BASE-T1L PHY has a pretty low communication speed and as technology is evolving implementations on high speed MCUs or programmable DSPs are in principle already possible and may get suitable in the future.

- These implementations would need some additional time for e.g. initializing the filters or during training, as the training is not implemented directly in logic, but in a software program, which may need more cycles for computation.

- Therefore the LPI sleep/refresh and wake timings have been relaxed by 50 µs (for $T_{w\_sys\_tx}$) compared to the timings in D3.0. The quiet time has been kept as it is.

- Based on the tables on the previous slides the following parameters for the LPI timers are set:

Timer Name	New Value	D3.0 Value
lpi_sleep_timer	**250 µs** (2500 bit times equal to 625 triple ternary symbols)	200 – 210 µs
lpi_quiet_timer	**6000 µs** (60 000 bit times equal to 15 000 triple ternary symbols)	6000 – 6300 µs
lpi_refresh_timer	**250 µs** (2500 bit times equal to 625 triple ternary symbols)	200 – 210 µs
lpi_wake_timer	**250 µs** (2500 bit times equal to 625 triple ternary symbols)	200 – 210 µs

Return Loss Changes

- Currently the return loss for a 10BASE-T1L link segment is defined as:

$$RL \geq \begin{Bmatrix} 9 + 9 \times f & 0.1 \leq f < 0.5\ MHz \\ 13.5 & 0.5 \leq f \leq 20\ MHz \end{Bmatrix} dB$$

- Assuming a symbol rate of 7.5 MS/s (133.33 ns/Symbol), a short link segment, with e.g. a length of typ. 12 m (12 m x 2 x 5.5 ns/m = 132 ns) leads, due to multiple reflections between the two MDIs, to nearly a doubling of the return loss compared to measuring the return loss for a long cable (as the insertion loss is pretty low for such short cables).

- Assuming a minimum characteristic impedance of the cable of 80 Ω (fieldbus cables are defined between 80 and 120 Ω), this leads to a reflection factor of:

$$|\Gamma| = \frac{|Z - Z_0|}{Z + Z_0} = \frac{20\ \Omega}{180\ \Omega} = 0.111$$

- This is equal to 19 dB. Assuming a short cable with no relevant insertion loss, the return loss may be as low as 13 dB for a cable with a characteristic impedance of 80 Ω.

- Therefore the following return loss specification is suggested:

$$RL \geq \begin{Bmatrix} 9 + \mathbf{8} \times f & 0.1 \leq f < 0.5\ MHz \\ \mathbf{13} & 0.5 \leq f \leq 20\ MHz \end{Bmatrix} dB$$

- The expected impact on a PHY implementation is small, as the RL is only decreased by 0.5 dB compared to the value in D3.0. For a PHY in 1.0 V_{pp} operating mode this results in an additional reflection of approx. 14 mV_{pp}, for a PHY in 2.4 V_{pp} operating mode the additional reflection is approx. 33 mV_{pp}.

Coupling Attenuation and TCL Changes

- For details see presentation about 10BASE-T1L conducted immunity testing: http://www.ieee802.org/3/cg/public/Jan2019/Graber_3cg_01c_0119.pdf

- As for E_1 and E_2 the same 3 V test level during conducted immunity testing is used, the required coupling attenuation also needs to be of the same value. Therefore the coupling attenuation for E_1 needs to be changed from min. 40 dB to min. 50 dB:

Frequency (MHz)	(dB)		
	E_1	E_2	E_3
0.1 to 20	**≥ 50**	≥ 50	≥ 60

- During conducted immunity testing a frequency sweep in 1 % steps is performed. The 10BASE-T1L PHY is able to adapt to this frequency sweep.
- Applying a tonal noise interferer (sweeping in 1 % steps with a duration of 10 ms per step) to the FPGA based 10BASE-T1L evaluation board, a maximum amplitude of approx. 180 mV_{pp} can be reached without causing bit errors (running over a link segment with 25.4 dB IL @ 3.75 MHz in between the two boards).
- Based on this measurement for a conducted immunity test the values of 50 dB (E_1 and E_2) and 60 dB (E_3) are sufficient and provide a margin of approx. 10 dB.
- In practical applications it is typically assumed that the noise levels are significantly lower than during EMC testing.

Coupling Attenuation and TCL Changes

- As for unshielded cables the same test levels for conducted immunity testing are used, the TCL values for unshielded cables need to be in the same range as the coupling attenuation values for shielded cables:

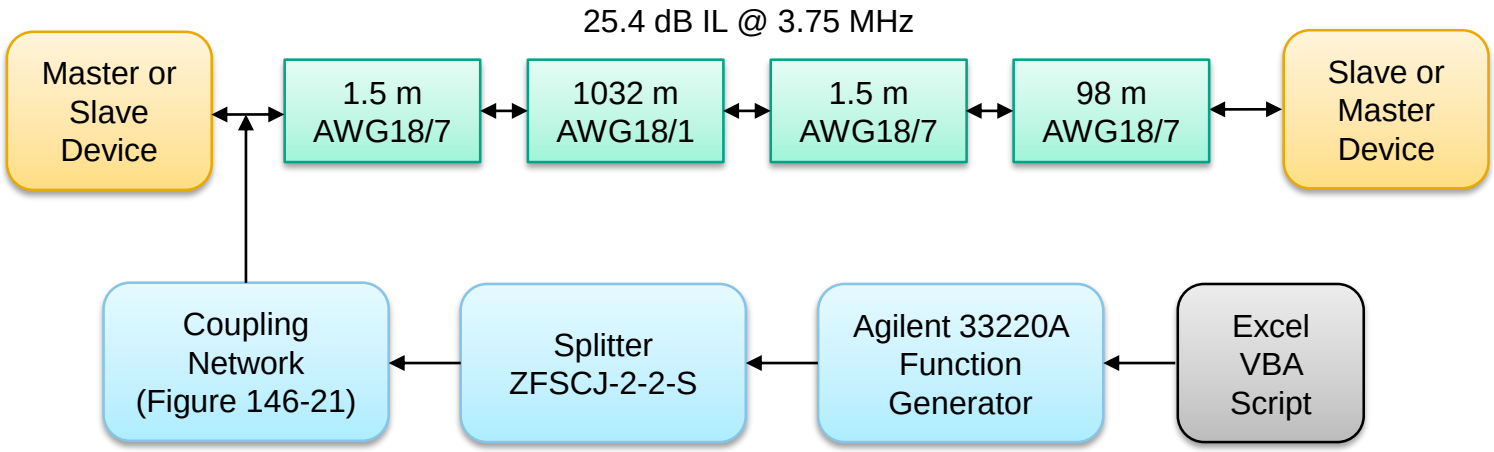
	Frequency (MHz)	E_1	E_2
TCL	**$0.1 \le f \le 10$**	**≥ 50 dB**	**≥ 50 dB**
	$10 < f \le 20$	**≥ $50 - 20 \log_{10}(f / 10)$ dB**	**≥ $50 - 20 \log_{10}(f / 10)$ dB**

- The suggested TCL values have a flat limit line below 10 MHz. For the TCL definitions in the current 802.3cg D3.0 draft the TCL values get quite high (up to 86 dB for 2.4 V and E_2), which makes it difficult to measure, while for the PHY itself it gets more critical in the higher frequency range, as the signal in the lower frequency range is significantly stronger.
- In the frequency range above 10 MHz, there is a decrease in the required mode conversion value by 20 dB per decade, which reflects the behavior of a first order low pass filter within the PHY input circuitry.
- At 10 MHz the required TCL value for E_1 is 12 dB higher and for E_2 it is 2 dB higher than defined in draft D3.0. The difference is again related to using the same test levels for E_1 and E_2 (as the test levels are identical for E_1 and E_2).
- Suggestion is to remove the ELTCTL values from D3.0 (similar to 10BASE-T1S, where also only mode conversion (MC) is specified).

Backup Slides

Tonal Noise Measurement Setup

- Below the test setup for the tonal noise test (0.1 to 20 MHz) is shown:



- The maximum allowed tonal noise amplitude (sine wave sweep) without causing bit errors at the output of the coupling network is about 180 mV_{pp} doing a frequency sweep with a 1 % increase between two nearby frequencies.
- A frequency dependent attenuation of the test setup (splitter, coupling network, MDI input impedance, characteristic impedance of the cable, etc.) is taken into account and compensated within the Excel VBA Script.

Thank You