10 Mb/s Single Twisted Pair Ethernet

10BASE-T1L Draft 0.3 Technical Comments

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146.1.2 Operation of 10BASE-T1L

- **Page 62, Lines 33 to 35:**

  Suggested is to use Clause 98 compatible auto-negotiation method including DME coding, but at a lower baud rate of 625 kBit/s (see also presentation 10BASE-T1L and Clause 98).

  Negotiation between high speed auto-negotiation data rate (16.667 MBit/s) and low speed auto-negotiation data rate (625 kBit/s) needs to be defined.

- **Page 62, Lines 52 to 53:**

  Currently the draft only contains the possibility to transmit the low power idle status. There needs to be more detailed work to adopt EEE (Clause 78) within the task force.

146.3.4 PCS Receive

- **Page 78, Lines 29 to 34:**

  The description of $Sr_n[2]$ and $Sr_n[3]$ is only a hint and not really necessary (if anybody thinks a little about this it should be clear), so the suggestion is to remove it.

- **Page 79, Lines 41 to 46 and Page 80, Figure 146-10:**

  This diagram was just for explanation, it is not really needed for implementing the standard, so the suggestion is to remove it.

- **Page 79, Lines 11 to 13:**

  The maximum size of an Ethernet frame is 1518 bytes (1.2144 ms transmit time plus preamble and inter-frame gap). Therefore with some headroom this timer can be set to 2 ms ± 100 µs. Jabber normally does not happen (even if an ESD is not correctly detected, receiving the next comma sequence will recover the state machine). The only need for this timer really is to recover from a loss of the scrambler lock, but in this case something completely went wrong.
  Thinking about Jumbo Frames it can make sense to increase the timer value. Jumbo Frames can be of size 9 kB, 12 kB, 14 kB or 16 kB. 100BASE-T1 e.g. allows from the timing frames up to 12 kB size. The question to the group is, what we want to support. One possibility could also be to go for the maximum 16 kB size, which leads to a time of 13.1216 ms, so e.g. 16 ms +/- 100 µs can be used.

146.3.5 PCS Loopback

- **Page 81, Lines 24 to 31:**

  It is right, that the comparison is done on top of the MAC layer and not by the MAC layer itself. In principle it is clear, how the PCS loopback should work, so the suggestion is to remove this paragraph.

146.4.4 PHY Control function

- **Page 84, Line 37:**

The maximum training time of 3000 ms results from the low symbol rate (which significantly slows down the training process compared to e.g. a 100BASE-T1 PHY). Additionally there is need to adopt the equalizer to a significant higher insertion loss and especially the echo canceller to a significantly higher return loss (as the intention is to use cables e.g. down to 70 ohms characteristic impedance, e.g. Belden 3076F cable).

My personal suggestion is to really keep the 3000 ms as this allows enough time for the echo canceller training during the phase search at the master side (the slave could in principle train faster). Theoretically we could speed up things by e.g. using some initial configurations for the echo canceller, which likely would decrease the needed training time, but this will limit possible implementations, what we should not do in this standard (there is also extremely likely several protected IP in the field of speeding up the training process).

For industrial applications this time is uncritical, as the booting of a device after powering up will take significantly longer and the PHY link-up process starts in parallel to the device initialization. For automotive applications even speeding up things very likely would not get into the 100 ms range without having a stored pre-trained coefficient set.

146.4.5 Link Monitor function

- **Page 85, Lines 47 to 53:**

  In principle we do not need it, but it could be an explanation, why the state machine is having the clock_recovered completed path (and it allows for a different implementation waiting until the training is ready), so my personal view would be to keep it, but finally it depends on the groups' decision if we want to keep it or not.

- **Page 86, Lines 27 to 31:**

  The reason for only having this very simple link monitor state machine is, that most of the link monitor functionality is already handled by the PHY control state machine, as it is also needed there. If the local or remote receiver status are bad or there is no scrambler lock, then the PHY control state machine switches automatically back to SEND_Z mode (going over SEND_I mode before) to get both PHYs in sync again. The link status therefore can be derived from the tx_mode value.

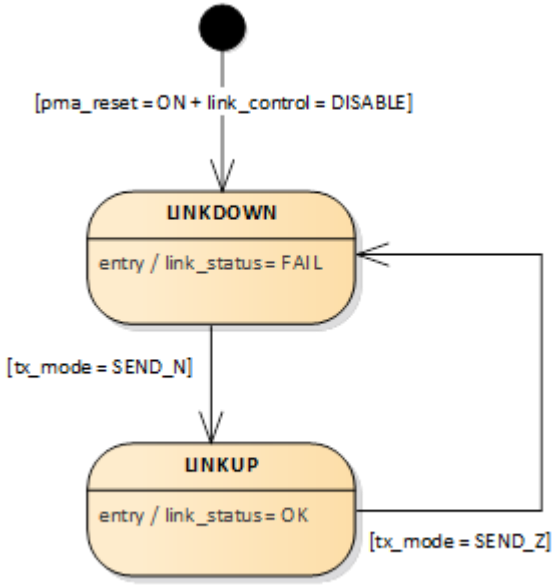
  The link_status is ok, if the PHY is in SEND_N mode or (temporarily) in SEND_I while it is trying to recover the link. If the PHY starts a retraining, the PHY control state machine automatically goes to SEND_Z and the link status is then set to FAIL. As most of the functionality is therefore already in the PHY control state machine, the Link Monitor state machine got such simple.

146.4.5 Link Monitor function

- **Page 86, Lines 27 to 31 (continued):**

As other PHYs also specify a link monitor state diagram and to keep the structure of this PHY aligned, it also uses a (very simple) link monitor state machine (alternatively we could split the SEND IDLE state in the PHY control state machine to include the logic into the PHY control state machine and omit the link monitor state machine).

The mode_changed flag is accidently coming from implementation details. It should have been left out here as it is not necessary to implement it in the state machine (it is enough to just compare for the tx_mode variable).



Variables (to be added to the draft document):

tx_mode	The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
	Values: SEND_Z, SEND_N, or SEND_I
link_status	The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
	Values: OK or FAIL

146.4.7 State Diagram

- **Page 87, Lines 39 to 40 (training_timer):**

  See comments for **146.4.4 PHY Control function**.

- **Page 87, Lines 43 to 45 (max_wait_timer):**

  The 200 ms ± 2 ms timer value provides enough time for a PHY to recover a failed link (e.g. caused by a significant disturbance) before starting a complete retraining, which takes up to 3000 ms.

  Disturbances (e.g. caused by adding devices or field switches) could last for some 10 ms on the line while communication over the link may not be possible, but this should not cause the link to completely fail. Therefore after the disturbances have finished, the PHY would have to recover the clock again and perhaps adjust some coefficients (which may have seen some effects from the disturbance also). All this should be finished within the 200 ms. As the disturbances are normally only up to 40 ms long and the clock recovery e.g. takes another 10 ms, theoretically we could also decide to reduce this time, but this could limit possible implementations.

  I personally would keep the 200 ms as this time is still low compared to the time needed for a complete retraining of up to 3000 ms.

146.4.7 State Diagram

- **Page 87, Lines 49 to 53 (minwait_timer):**

  20 µs ± 1 µs (190 - 210 bit times) seem to be suitable as this time is short enough compared to a minimum frame size of 64 bytes. This time is needed to cleanly handle the state transitions and allow for transmission of at least enough data so that the remote PHY can sync) so that the suggestion is to keep the typ. 200 bit times, which is well below the 512 bit times of a 64 byte telegram, even if the timer has to elapse 2 times.

146.5.1 EMC tests

- **Page 88, Lines 12 to 15:**

  The EMC tests described here on chip level need review from a chip vendor. Another option would be to leave them out and rely on system level tests.

  Input from the task force is needed, which way we want to go and which chip level EMC tests make sense.

  It also needs to be discussed if a unification between the long reach 10BASE-T1L and the short reach 10BASE-T1S PHY makes sense.

146.5.4 Transmitter electrical specifications

- **Page 90, Lines 3 to 14:**

  A transmitter with 1.0 V_{pp} and a transmitter with 2.4 V_{pp} would be interoperable at the same link segment as long as it is no intrinsically safe powered link segment. Nevertheless the SNR or the maximum reach is lower in such as case compared to having two transmitters using 2.4 V_{pp} transmit level. A decision of the task force how to handle this within the standard is required.

- **Page 90, Lines 16 to 28:**

  As the test pattern 2 has been adopted to have an alternating 10 times “+1” and 10 times “-1” transmitted, my personal opinion is to keep the 10 bit times pulse duration of this test. As the first and the last bit partly have a rising or falling signal, the inner 9 bits are taken. The maximum droop is specified to be 20 % for this pulse. This would be equal to approx. 10 % droop for a 5 bit times pulse (which is the maximum pulse length in a 4B3T coding). Taking e.g. the clamping diodes in intrinsically safe applications into account, this droop should not cause a significant conductance of the clamping diodes in forward direction, affecting the echo canceller.

146.5.4 Transmitter electrical specifications

- **Page 90, Lines 35 to 48:**

  The transmit jitter is mainly burdening the echo canceller of the local PHY. For the far end receiver this is much less critical. Currently 10 ns are defined as maximum transmit jitter. For the far end receiver this should work (at the sampling is in the middle of the bit and therefore some jitter can be tolerated). For the echo canceller likely a significant lower jitter would be necessary to provide a good signal quality depending on the set phase. Nevertheless as this is implementation dependent, depending on how the echo canceller is implemented, the PHY will have to produce a lower transmit jitter by its own.

  Therefore in principle we could keep the 10 ns (which have already been adopted), but we could also think about reducing the transmit jitter (e.g. to 1 ns).

- **Page 90, Line 42 to Page 91, Line 11 and Page 91, Line 16 to Page 94 Line 20:**

  Some current measurements show, that the rise and fall times are much less critical as originally thought. Therefore likely there will be a significant relaxing of the rise and fall time requirements. We should discuss within the task force, if instead of the fixed “normalized test pattern” it would be better to use a PSD template and how to get there.

146.5.5 Receiver electrical specifications

- **Page 94, Lines 47 to 49 and Page 95, Lines 1 to 19:**

  It needs to be discussed, if the suggested test is suitable for the intended application or if a better test is available.

  The absolute maximum limits for a typical evaluation board with the latest implementation having a link segment with an IL of 25.4 dB @ 3.75 MHz are approx. -98 dBm/Hz for an AWGN noise with a BW of 10 MHz (tested with the Spirent noise tester).

  The absolute maximum limit for in-band noise connecting a second master PHY using a resistor divider is 36 mV_{pp}. Due to the high attenuation of the link segment, only shielded cables are suitable for long reach applications.

  From both limits we would have to subtract some margin for tolerances. Which values to finally use needs to be discussed with the group.

- **Page 95, Lines 31 to 34:**

  It is suggested to keep the mentioned values of 2.76 V_{pp} and 1.15 V_{pp} (1.15 V should still work for the clamping diodes even over temperature).

146.7.1.4 Maximum link delay

- **Page 95, Line 31:**

  Including AWG14 cable, which has a lower IL than AWG18 cable, we should think about adding some margin for e.g. up to 1500 m of cable.

  Assuming a maximum propagation delay of 5.5 ns per meter this leads to a total propagation delay over the link segment of 8250 ns.

  This parameter should not be too critical (e.g. when comparing it to the PHY latency it is in the same range). As we have a full-duplex PHY, there is no collision domain, which would have an influence on the minimum packet length.

Further Things that need Discussion

- PHY delay constraints:
  - What is the maximum allowed propagation delay time on the transmit path of the PHY?
  - What is the maximum allowed propagation delay time on the receive path of the PHY?
- Electrical/Networking safety requirements:
  - Use the same as in other standards?
  - Add additional application specific requirements?
- Environmental safety requirements:
  - Environmental, mechanical climatic, chemical, electrical requirements?
- EMC requirements on system level:
  - MICE environment?
  - Additional application specific requirements?
- MDI return loss specification.
- Required MDI fault tolerance (especially as there is no transformer isolation):
  - Short circuit tolerance
  - Ground fault tolerance
  - Maximum applicable external voltage

  Maximum allowed inrush current (due to capacitive coupling in a powered system, e.g. 60 V / 50 Ω = 1.2 A)
- Including of the informative annex for intrinsic safety (see also 10BASE-T1L Clause 146 Rev. F.pdf).

Thank You