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The Art of Silicon Sculpting

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IEEE802.3cg TF

Short Reach PCS, PMA and PLCA baseline proposal

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  - Adoption of Electrical Specifications
- PMA
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  - Definition of primitives
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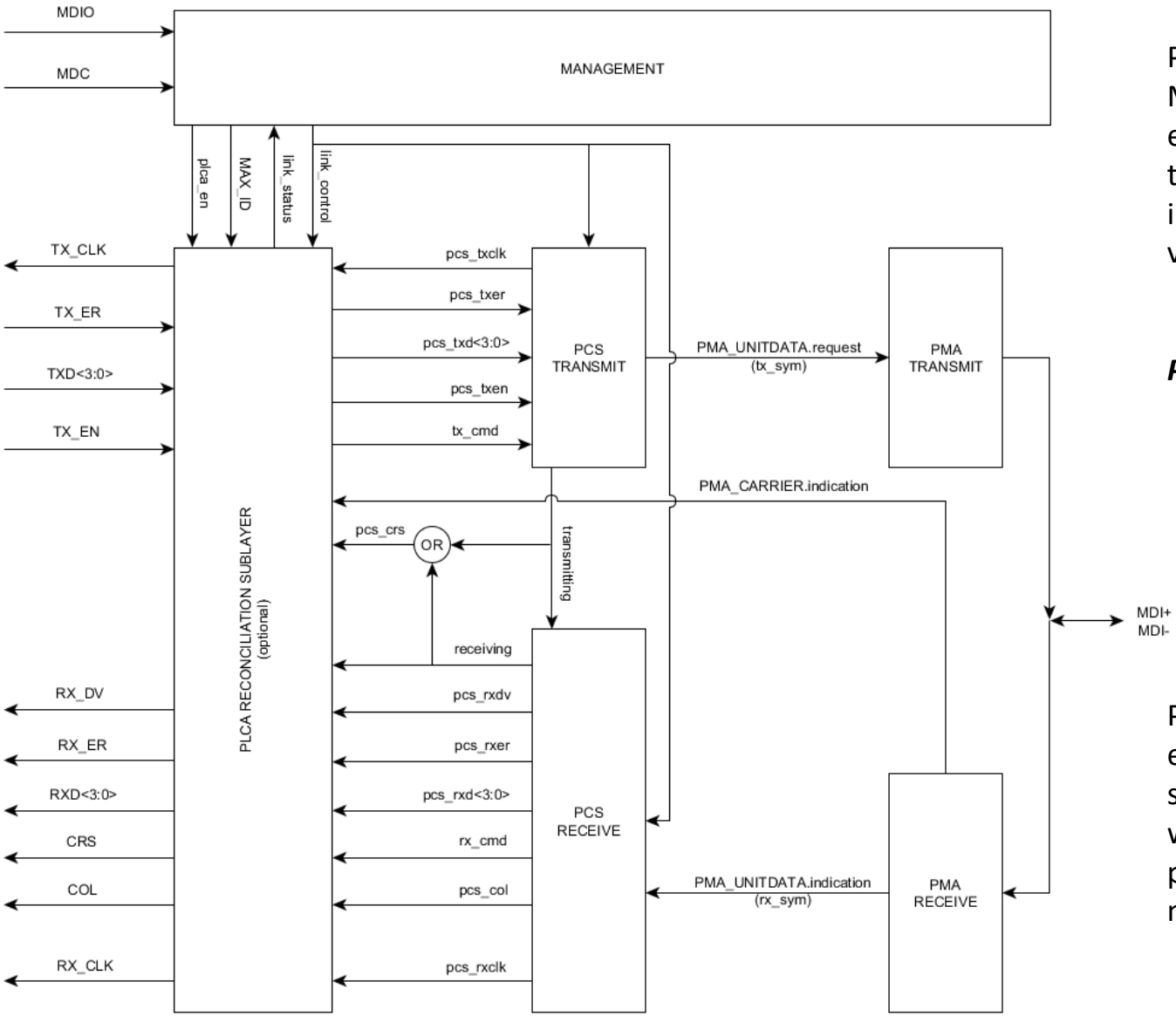
  - Adoption of TX state machine
  - Adoption of RX state machine
  - Adoption of MII clause 22
- PLCA
  - Adoption of state machines
  - Definition as optional reconciliation sublayer

Overview



MII

PCS functions converts MII data to 4B/5B encoded symbols for the PMA to serialize into a DME encoded voltage levels

Proposed text in 148.1

PLCA is an optionally enabled feature for the short reach use case which improves performance over a multidrop network.

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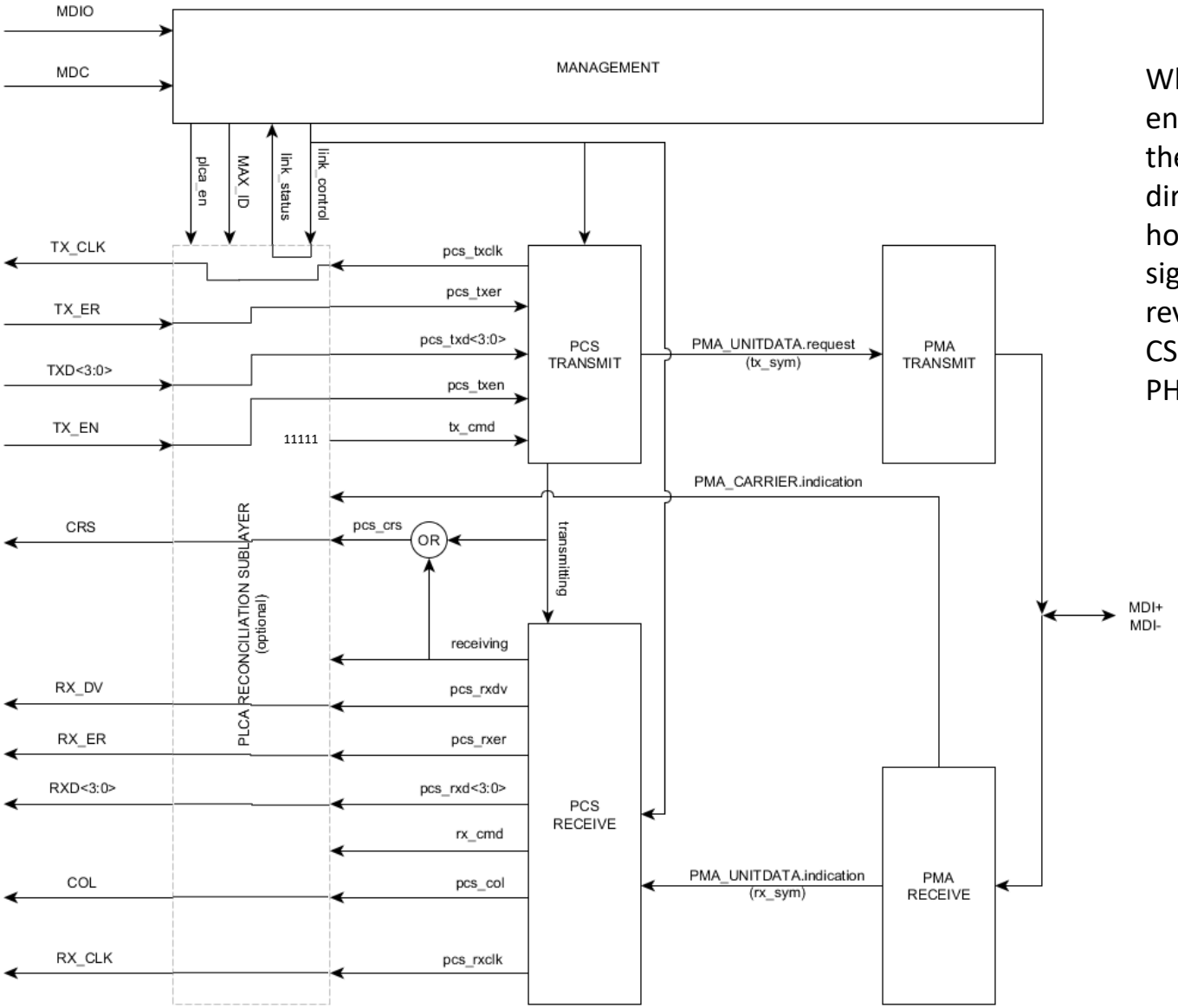
Overview – NO PLCA

MII



When PLCA is not enabled/implemented the PCS functions maps directly to the homonymous MII signals, and the system reverts to a standard CSMA/CD compliant PHY.

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PCS

4B/5B Encoding

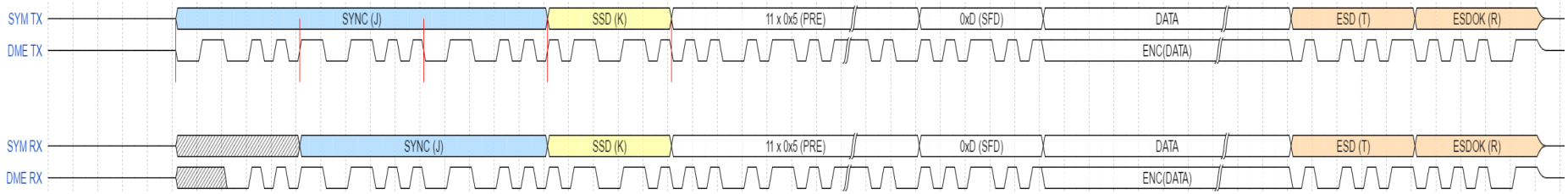
Name	4b	5b	Name	4b	5b	Special Function
0	0000	11110	I	-	11111	SILENCE
1	0001	01001	J	-	11000	SYNC
2	0010	10100	K	-	10001	SSD
3	0011	10101	T	-	01101	ESD
4	0100	01010	R	-	00111	ESDOK
5	0101	01011	H	-	00100	ESD
6	0110	01110	N	-	01000	BEACON
7	0111	01111				
8	1000	10010				
9	1001	10011				
A	1010	10110				
B	1011	10111				
C	1100	11010				
D	1101	11011				
E	1110	11100				
F	1111	11101				

PROPOSED TEXT IN 147.3.3.1.2

CODES REPRESENTING VALID 4B DATA

CODES USED FOR SIGNALING

Packet TX/RX (descriptive)



- PCS TX function replaces the first four 5B-encoded nibbles of packet preamble with the following symbol sequence, to allow receiver synchronization:
  - J, J, J, K (00011 00011 00011 10001)
- PCS TX function then inserts 5B encoded MII data followed by ESD and either ESDOK or EDERR symbols depending on TX_ERR state during packet transmission
- PMA RX exploits the first three '0' DME bits of the first 'J' symbol to synchronize on DME stream, then uses the following two 'J' symbols to align on 5B boundary
- PCS RX detects the 'JK' sequence to regenerate at the proper point in time the packet preamble conveyed to MII, along with the packet data following the SFD.
- RX_ER is regenerated from ESD sequence accordingly
- Pretty similar to what PCS functions do in 802.3bw (100base-T1 PHY).
- ***Proposed Text in 147.3.2.1 and 147.3.4.1***

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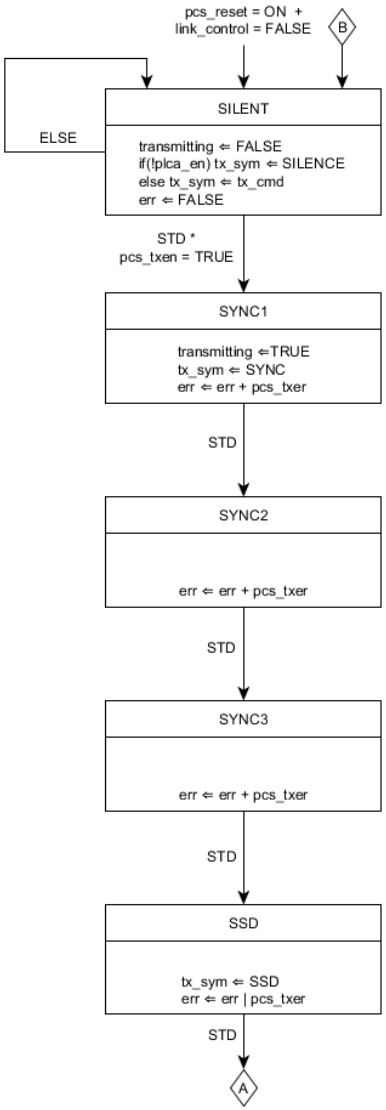
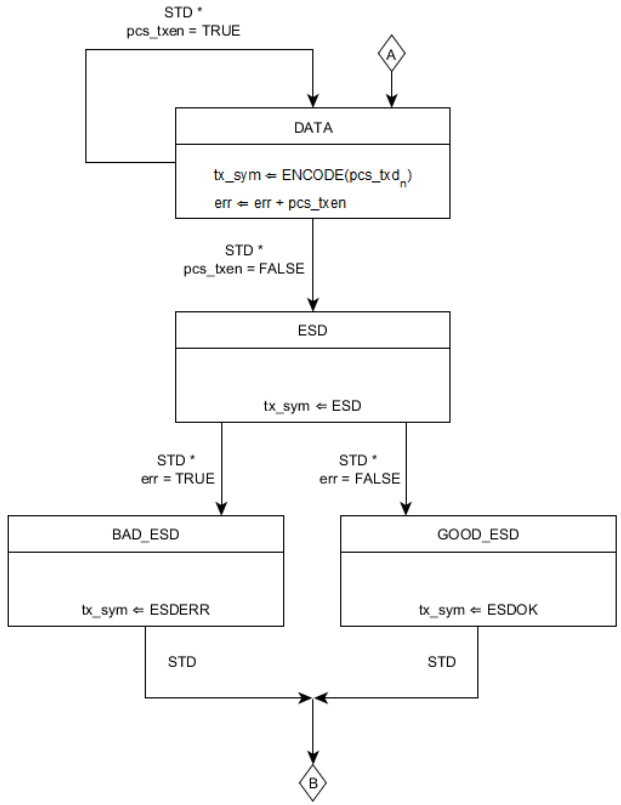
PCS Transmit State Machine





PROPOSED TEXT IN
147.3.4.1.4

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PCS TRANSMIT: variables

- **pcs_reset**: The pcs_reset parameter set by the PCS Reset function.
  - Value: ON or OFF
- **pcs_txen**: The TX_EN signal of the MII as specified in .. When optional PLCA is enabled, this signal is generated as specified in .. When set to FALSE transmission is disabled. When set to TRUE transmission is enabled.
  - Value TRUE or FALSE
- **pcs_txer**: The TX_ER signal of the MII as specified in .. When optional PLCA is enabled, this signal is generated as specified in .. When set to FALSE it indicates a non-errored transmission. When set to TRUE it indicates an errored transmission
  - Value: TRUE or FALSE
- **pcs_txd**: The TXD signal of the MII as specified in .. When optional PLCA is enabled, this signal is generated as specified in .. The signal represent a 4B nibble to transmit
- **tx_cmd**: 5B symbol to be transmitted when the PCS Transmit function is in SILENT state. The tx_cmd variable is set by the optional PLCA reconciliation sublayer to signal a BEACON condition or to commit a time slot as described in 148.2.1.1. When PLCA functions are not implemented, tx_cmd shall be set to the special 5B symbol 'I' (1,1,1,1,1) representing SILENCE.
- **tx_sym**: 5B symbol to transmit, generated from the MII data or directly passed from tx_cmd in SILENT state when optional PLCA reconciliation sublayer is implemented.

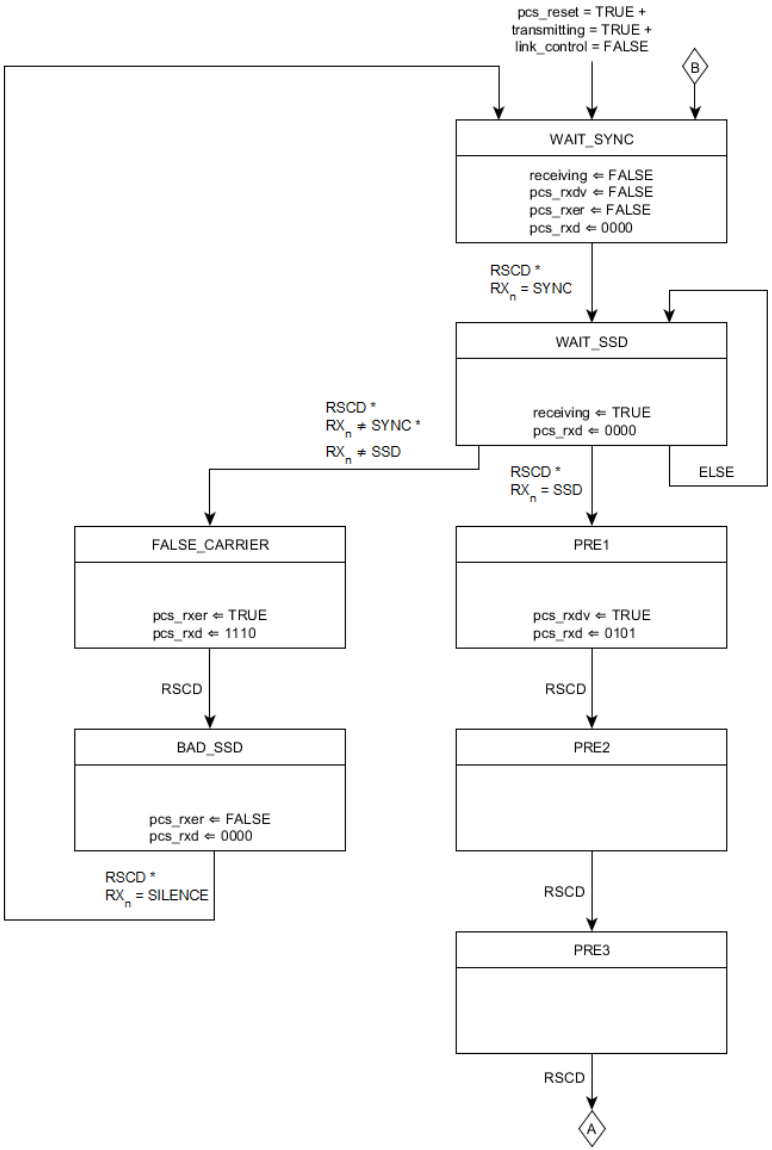
PCS TRANSMIT: variables

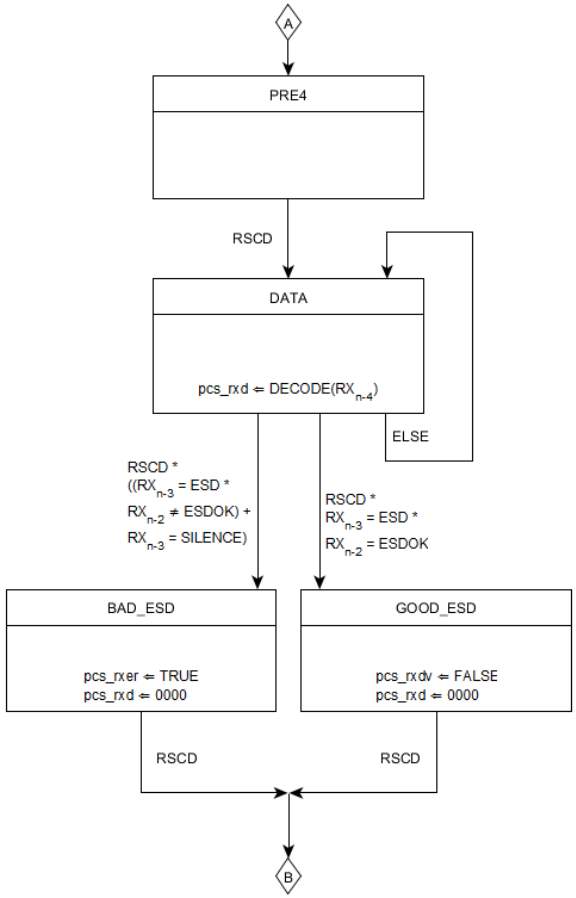
- **transmitting**: the transmitting variable is set in the PCS data transmission as defined in figure… When this variable is set to TRUE it indicates a transmission is ongoing.
  - Value: TRUE or FALSE
- **err**: the err variable is set in the PCS data transmission as defined in figure… This variable is used to detect a pcs_txer during transmission; if such error is detected, a ESDERR symbol is sent at the end of transmission
  - Value: TRUE or FALSE
- **link_control**: This variable is generated by management or set by default. When set to FALSE all PCS functions are switched off and no data can be sent or received.
  Values: TRUE or FALSE.
- **SYNC**: 5B symbol defined as 'J' in 4B5B encoding
- **SSD:** 5B symbol defined as 'K' in 4B5B encoding
- **ESD**: 5B symbol defined as 'T' in 4B5B encoding
- **ESDERR**: 5B symbol defined as 'H' in 4B5B encoding
- **ESDOK**: 5B symbol defined as 'R' in 4B5B encoding
- ***Proposed text in 147.3.3.1.1***

PCS TRANSMIT: functions, abbreviations

- **ENCODE**: In the PCS transmit process, this function takes as its arguments the pcs_txd input data and returns the corresponding 5B symbol as defined in table
  - ***Proposed text in 147.3.3.1.2***
- **STD**: alias for symbol timer done, synchronous to PCS TX clock
  - ***Proposed text in 147.3.3.1.4***

PCS Receive State Machine





PROPOSED TEXT IN 147.3.4.1.5

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PCS RECEIVE: variables

- **receiving**: the receiving variable is set in the PCS data receive as defined in figure… When this variable is set to TRUE it indicates a receive is ongoing.
  - Value: TRUE or FALSE
- **pcs_rxdv**: The RX_DV signal of the MII as specified in 22.2.2.7.
- **pcs_rxer**: The RX_ER signal of the MII as specified in 22.2.2.10.
- **pcs_rxd**: PCS decoded data synchronous to RX_CLK.
- **RXn**: Received 5b symbol generated by PMA receive at time n
- **SILENCE**: A 5B symbol defined as 'I' in 4B5B encoding
- ***Proposed text in 147.3.4.1.1***

PCS RECEIVE: functions, abbreviations

- **DECODE**: in the PCS Receive process, this function takes as its arguments the sym_rx input data from PMA and returns the corresponding 4B MII data as defined in table ...
  - ***Proposed text in 147.3.4.1.2***
- **RSCD**: alias for Receive Symbol Conversion Done, synchronous to PCS RX clock
- ***Proposed text in 147.3.4.1.4***

PCS Loopback

- The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to a one (or PCS loopback mode is enabled by a similar functionality if MDIO is not implemented). In this mode, the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium. The PCS loopback data flow is illustrated in Figure 146–11.

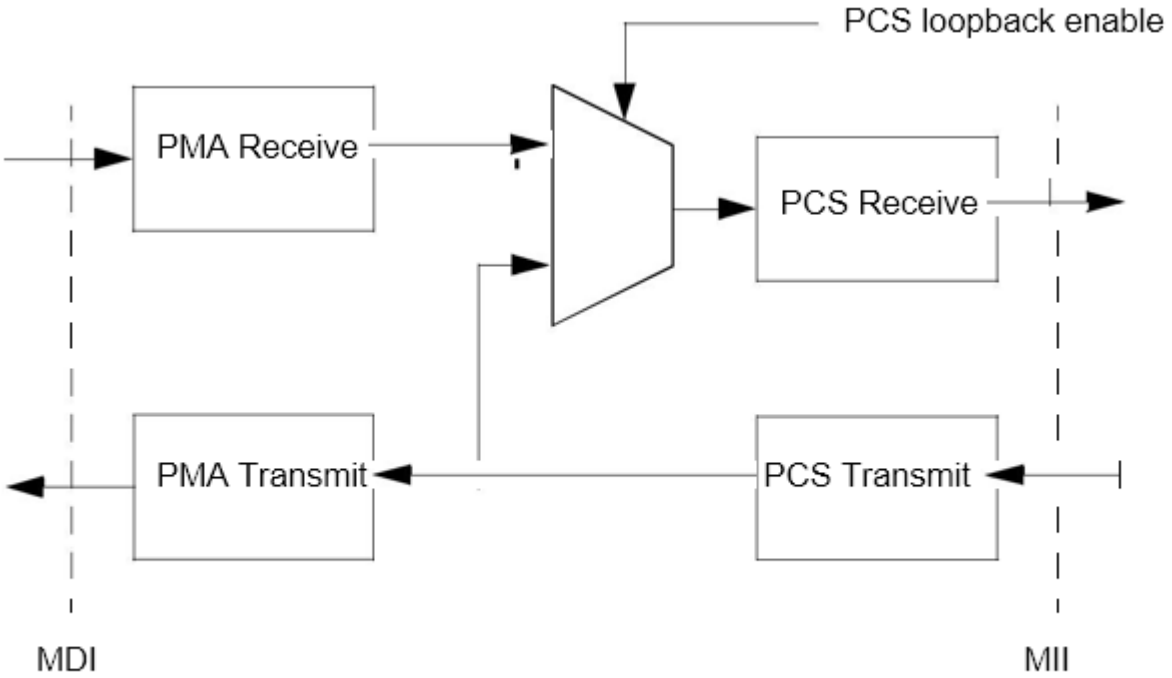

Figure 146–11—PCS loopback data flow

PROPOSED TEXT IN 147.3.5

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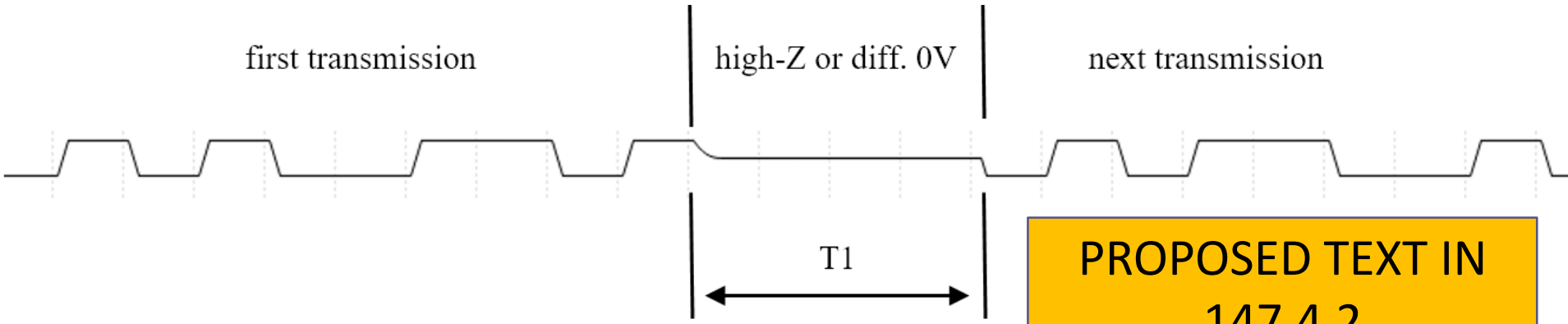
CRS, COL

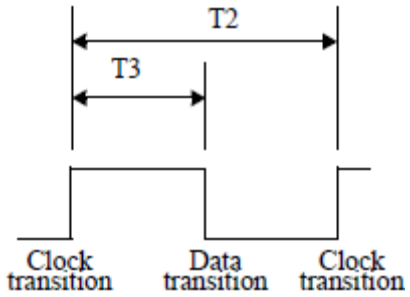
- When operating in half-duplex mode, the 10BASE-T1S PHY shall detect physical collisions on the media during data transmission. When collisions are detected, the PHY shall assert the signal COL on the MII for the duration of the collision or until TX_EN signal is FALSE.
- A collision may be detected by monitoring the rx_sym parameter conveyed through the PMA_UNITDATA.indication primitive for a SYNC, SSD symbol sequence (that is a 'JK' 5B sequence) and verify matching against the transmitted symbol sequence after the SSD. A collision results in a mismatch in the symbol sequence.
- ***Proposed text in 147.3.6***
- When operating in half-duplex mode, the 10BASE-T1S PHY shall sense when the media is busy and convey this information to the MAC asserting the signal CRS on the MII as specified in clause 22.x.
- CRS is generated by PCS Receive as the logical OR of the "transmitting" and "receiving" variables.
- ***Proposed text in 147.3.7***

PMA & PMD

Line Coding



PROPOSED TEXT IN 147.4.2



5B data is shifted out LSB first, and encoded with Differential Manchester Encoding (DME)

DME uses the presence or absence of transitions between these two voltage levels to encode data, thus the polarity is irrelevant.

	Parameters	Min	Typ	Max	Units
T1	Delay between transmissions	200			ns
T2	Clock transition to clock transition		80		ns
T3	Clock transition to data transition (data = 1)		40		ns

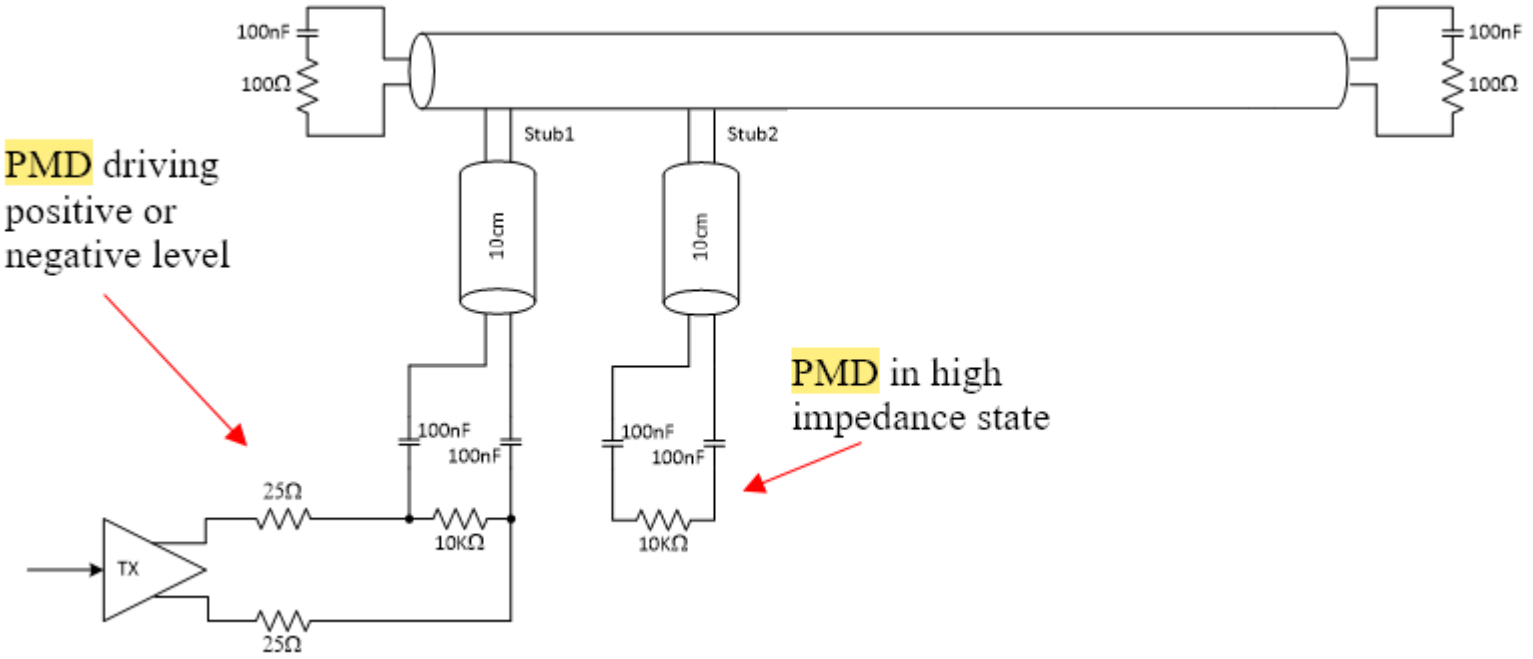
Line Coding

- Transmitter Baud Rate tolerance shall be ± 100ppm of nominal frequency (see T2 and T3)
  - ***Proposed text in 147.5.4.5***
- Transmitter peak differential output:
  - When measured with 100 Ω termination, transmit differential signal at MDI shall be within range of 1 V ± 30% peak-to-peak
  - ***Proposed text in 147.5.4.1***

PMD Electrical Specifications

- The PMD shall be able to drive a line consisting of the MDI and a twisted pair copper cable with nominal characteristic impedance of 100 Ohms.
- In order to support point-to-point operating mode, the PMD shall provide fixed 100 Ohm termination +/- 10% and shall be able to drive positive, negative and zero differential voltage levels as specified in . . .
  corresponding respectively to DME positive, negative and silence line states.
- In order to support multidrop operating mode, the PMD shall provide fixed 50 Ohm termination +/- 10% and shall be able to drive positive or negative voltage levels and go to high impedance state as specified in . . . corresponding respectively to DME positive, negative and silence line states.
- In Multidrop configuration the MDI shall be terminated by two 100 Ohm nominal resistances at the edges as in figure 3. When not driving the MDI, the PMD shall insert a fixed termination of 10 KOhms.
- ***Proposed text in 147.6.2***

PMD Electrical Specifications



PROPOSED TEXT IN 147.6.2

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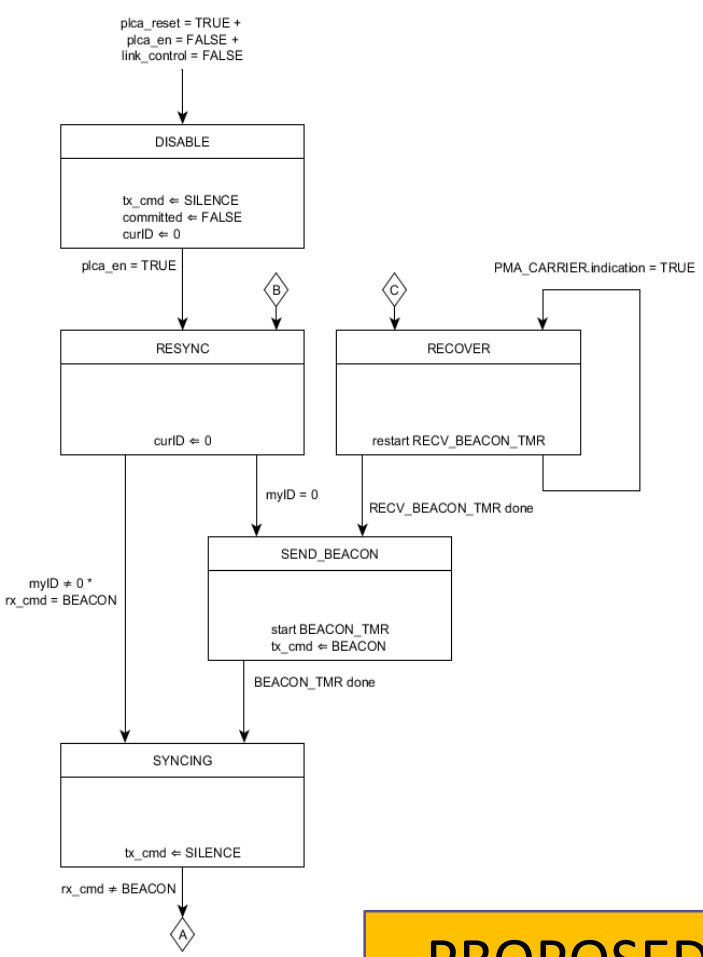
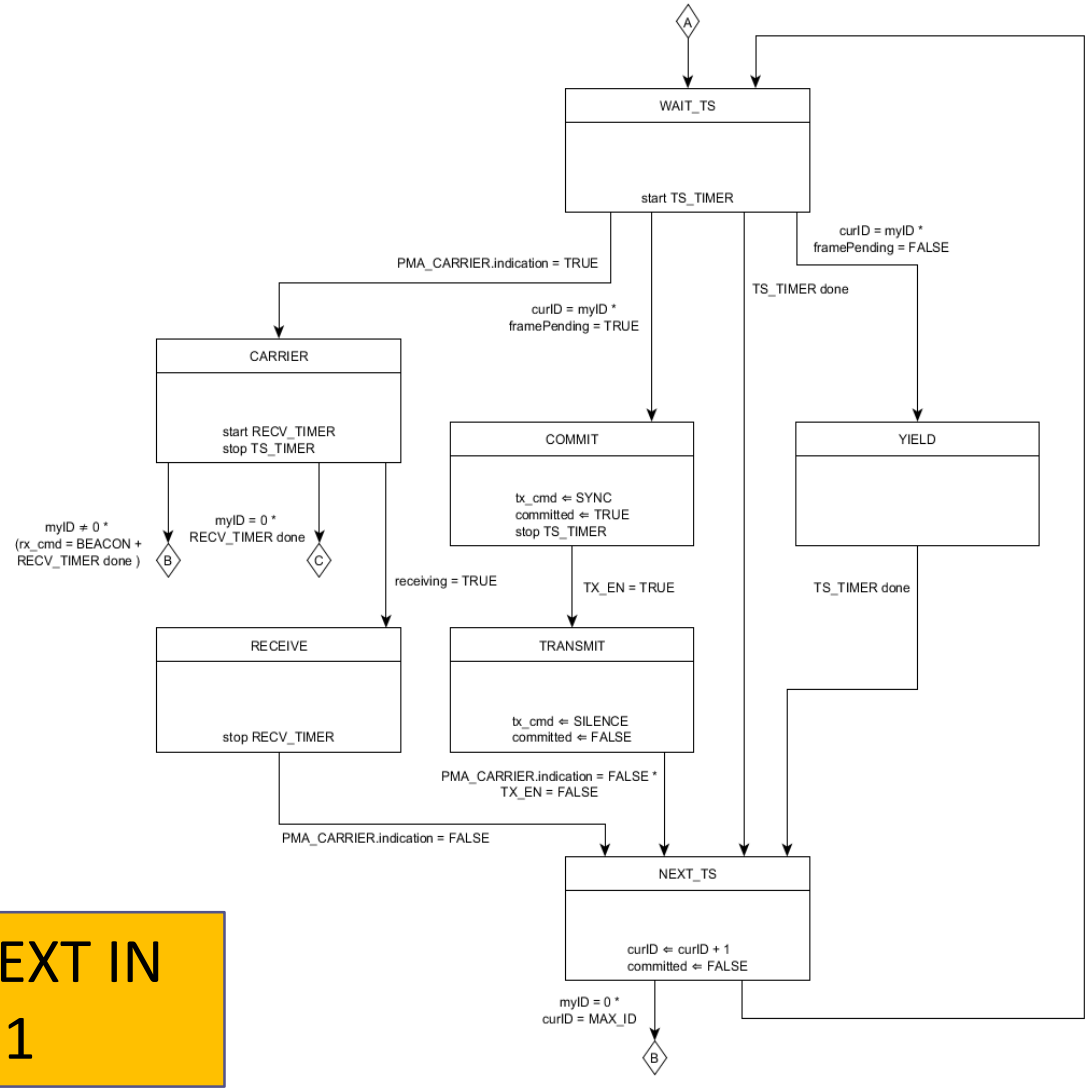
Test Modes

- Test mode 1 - Transmitter output voltage, timing jitter
- Test mode 2 - Transmitter output droop test mode
- Test mode 3 – Transmitter distortion test and PSD mask
- When test mode 1 is enabled, the PHY shall repeatedly transmit the data symbol sequence (+1, -1). See 147.4.2 for transmit clock requirements.
- When test mode 2 is enabled, the PHY shall transmit ten "+1" symbols followed by ten "-1" symbols. This sequence is repeated continually.
- When test mode 3 is enabled, the PHY shall transmit continually a pseudo-random sequence of “+1” and “-1” symbols. TBD: how to generate the sequence.
- ***Proposed text in 147.5.2***

PLCA

PLCA functions





PROPOSED TEXT IN 148.2.1.1

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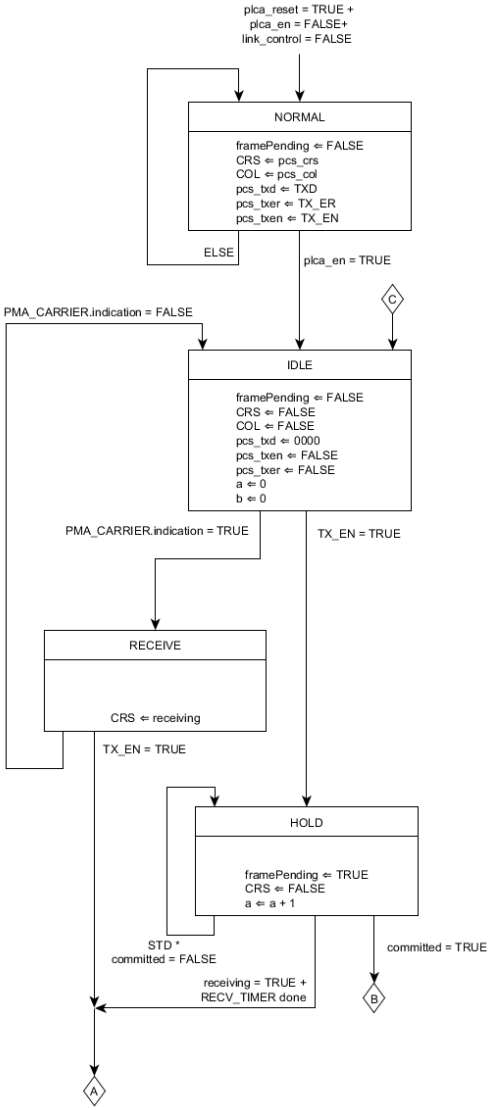
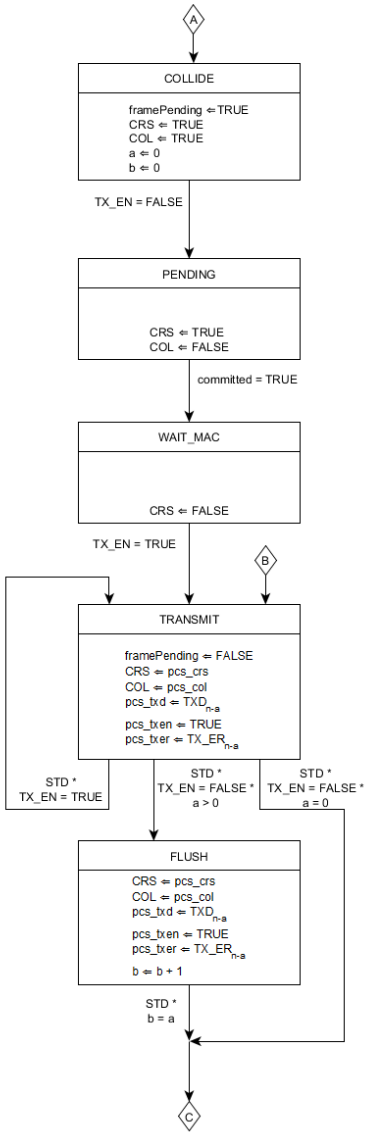
PLCA functions





PROPOSED TEXT IN 148.2.2.1

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PLCA: variables

- **plca_en**: generated by management interface, enables PLCA functions. When set to FALSE the TX functions revert to standard CSMA/CD.
  - Value: TRUE or FALSE
- **link_control**: generated by management interface, enables PCS TX and RX functions. When set to FALSE MII data from MAC is discarded and receiver functions are disabled.
  - Value: TRUE or FALSE
- **link_status**: generated by PLCA reconciliation sublayer, informs the management interface that the PHY is ready to send/receive data via MII interface.
  When PLCA function is not enabled/implemented link_status shall be continuously assigned to the link_control current value.
  - Value: TRUE or FALSE
- **myID:** generated by the management interface, represents the PLCA time slot ID assigned to the PHY. Special value '0' is assigned to the master node, indicating the PHY shall generate BEACON signals as described in ...
  - Value: integer value from 0 (master) to MAX_ID
- **MAX_ID:** generated by the management interface, indicates the number of time slots to be allocated, that is the maximum number of PHYs that can join the multidrop network. This parameter is only meaningful for the master PHY (myID = 0), for slave PHYs is a don't care.
  - Value: integer number from 0 to 255
- **committed:** internal variable used to synchronize PLCA Control and Data functions as depicted in ... It is set by PLCA Control state machine to signal that the current time slot has been committed and the PLCA Data state machine is now allowed to convey MII data to the PCS.
  - Value: TRUE or FALSE
- **framePending:** internal variable used to synchronize PLCA Control and Data functions as depicted in ... The PLCA Data state machine sets this variable when it detects the MAC is ready to send a packet in order to have the PLCA Control state machine actually commit the next available time slot.
  - Value: TRUE or FALSE
- ***Proposed text in 148.2.1.2***

PLCA: timers

- **BEACON_TIMER**: represents the time for which the master PHY signals a BEACON condition on the line when a PLCA cycle starts. It shall be set to 20 BT to allow the slave PHYs to properly recover the signal.
- **RECV_TIMER**: the time a PHY waits after PMA detects a carrier on the line (i.e. it is aligned at least on DME bit stream as described in ...) and the PCS RX actually achieves synchronization. The purpose of this timer is to allow early detection of carrier on the line to minimize time slot skew (see ...) allowing smaller time slots (see TS_TIMER) and increased efficiency. In presence of false carrier events, this timer expires and triggers a recovery function as described in ... (slave PHY waits for a new BEACON while master PHY waits for all slaves to be silent before sending a new BEACON). Timer value is implementation defined but shall be greater than PHY total RX latency including PMD, PMA and PCS RX.
- **TS_TIMER**: this is the time slot timer, as defined in (...). It shall be set according to maximum allowed PHY TX and RX latencies and maximum MDI to MDI propagation delay, as reported in (...).
  For a 25m cable and 10BT of total RX+TX latency a safe default value is 20BT (see ...).
- **RECV_BEACON_TIMER:** during a recovery operation (see ...) the master PHY needs to wait for all slave PHYs to be silent before sending a new BEACON.
  This timer value shall be set at least to TS_TIMER * (MAX_ID + 1) for safe operations.
- ***Proposed Text in 148.2.1.4***

Thank You !