ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

Clause 104 Modifications for 10SPE

HEATH STEWART

Presentation Objectives

- Accommodate 10SPE Long Reach
  - Additional PHY capacitance
  - 1km Fieldbus Type A STP cabling
- Propose changes to Clause 104 SCCP to support 10SPE
  - Modifications to SCCP timing
  - Add clarity for PD reservoir capacitor recharge
  - Add clarity to TSLOT by splitting into RESET, READ, and WRITE variants

Justification

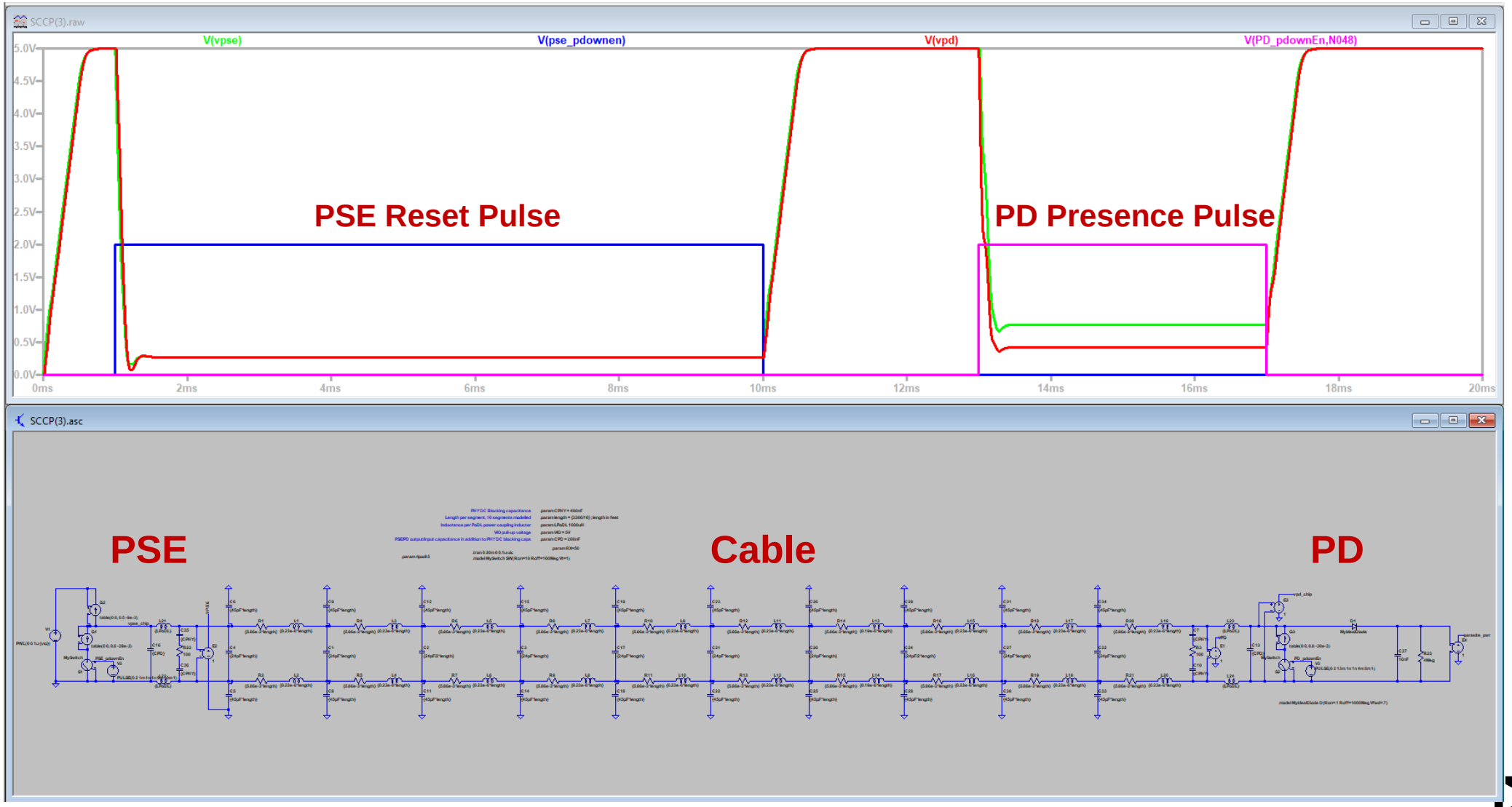
- PoDL provided two separate means of positively identifying a PD
  - Detection – Used for engineered systems requiring < 10ms start-up eg automotive
    - Not compatible with resistance of 10SPE Long Reach cable
  - Classification – Used for discoverable systems
    - Based on 1-Wire™
    - Does not require valid detection
    - PD relies on “parasite power” for PSE during classification sequence
- PoDL classification is appropriate for 10SPE Long Reach
  - Can be readily adapted to higher PHY and cable capacitance
  - T_R, rise time, and T_F, fall time, must be extended
  - To avoid slower bit rate, tighten PD timing uncertainty budget
    - Was: +/-50%
    - Propose: +/-30%

Presentation Objectives

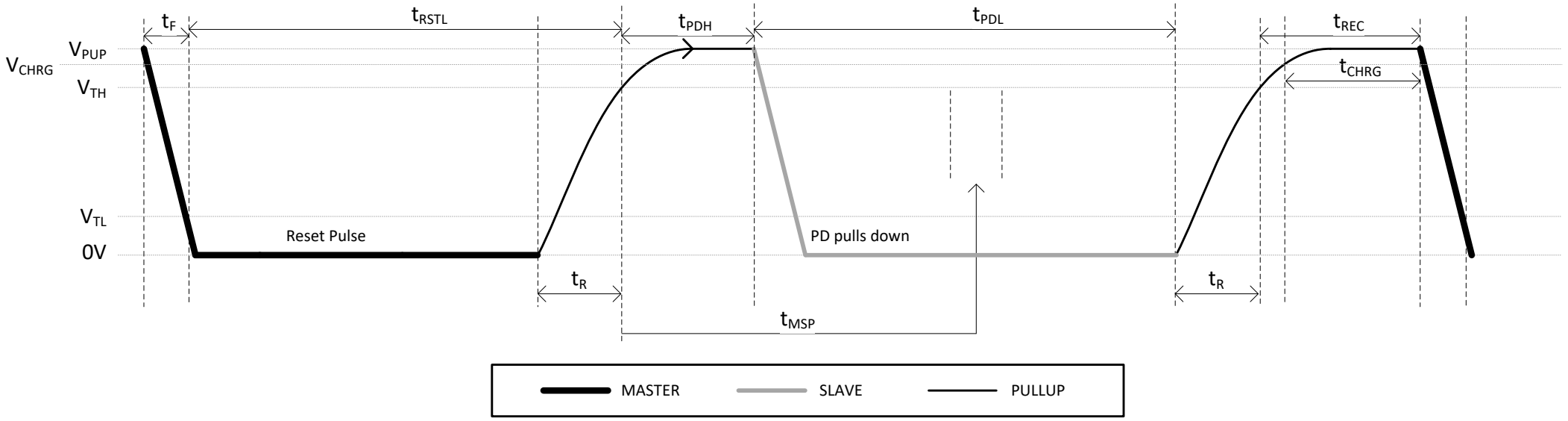
- Modify Table 104-8 SCCP Electrical Requirements
  - Add clarity for PD reservoir capacitor recharge
    - Create $V_{CHRG, min} = V_{PUP, min} * 90\%$
    - Create $t_{CHRG, min} = 200us$
  - Track changes to PHY and cable capacitance
    - Change C_{IN_Class} to 400nF
    - Change C_{Bus} to 72nF (TBD)
  - Add clarity to T_{SLOT} by splitting into RESET, READ, and WRITE variants
    - Add $t_{RSTSLOT}$, $t_{WRITESLOT}$, $t_{READSLOT}$ as shown in following slides
    - Remove t_{SLOT}
  - Modifications to SCCP timing as shown in following slides

Spice Model of SCCP System

1km Fieldbus Type A Cable (STP), C_{PHY} = 400nF



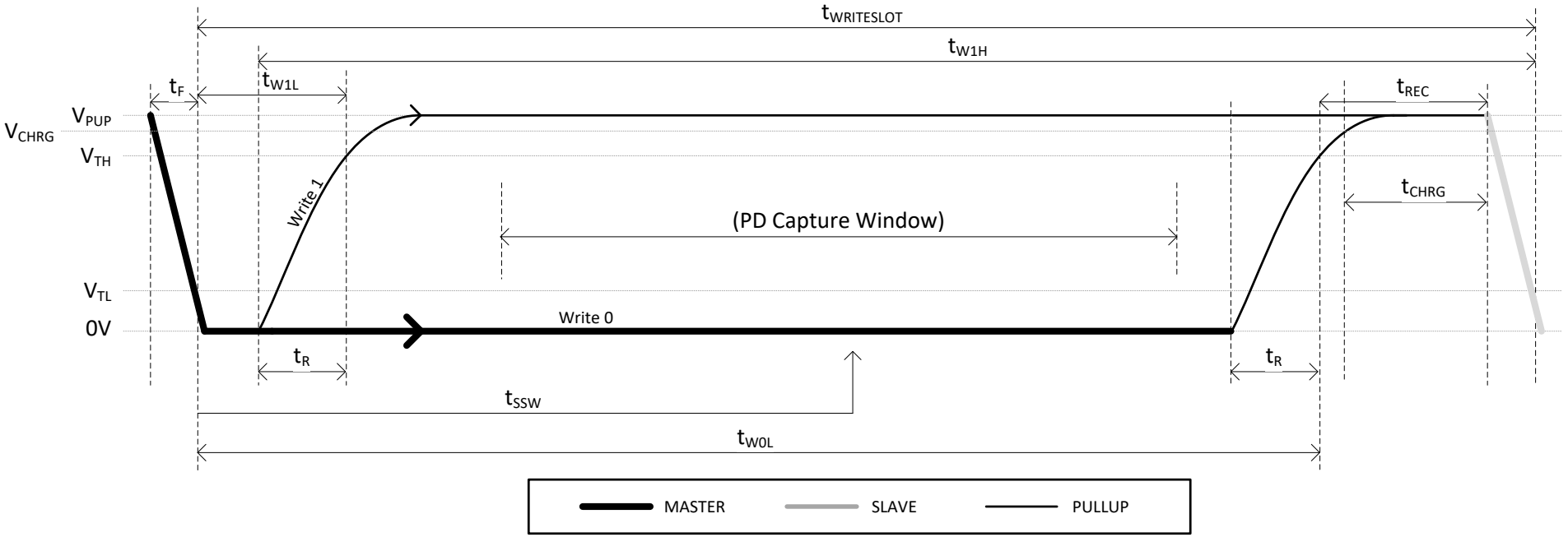
Reset command timing proof



Symbol	Min	Typ	Max	Unit	Note
t_F			**250**	us	5V pu vs 100Ohm pd
t_R			**500**	us	9mA PSE pu / 0.4uF C_{chan} V_{TL} to V_{CHRG}
t_{RSTL}	**8**	9	**10.5**	ms	PSE LO time for Reset pulse
t_{PDH}	**0.7**	1.0	**1.3**	ms	PD HI, measured from rising edge V_{TH}
t_{PDL}	**2.8**	4.0	**5.2**	ms	PD LO, presence pulse, pulldown duration
t_{MSP}	**1.8**	2.0	**2.2**	ms	PSE presence capture, measured from rising edge V_{TH}
t_{REC}	**270**	300	**330**	us	Charge PD SCCP reservoir capacitor
t_{CHRG}	**200**			us	Critical PD SCCP reservoir capacitor charging region
$t_{SLOT,RST}$			18.6	ms	
t_{LO}			10.5	ms	PD must maintain state

Red indicates changed parameters
***Bold** indicates parameters captured in SCCP electrical requirements*

Write 0/1 slot timing proof



Symbol	Min	Typ	Max	Unit	Note
t_F			250	us	5V pu vs 100Ohm pd
t_R			500	us	9mA PSE pu / 0.4uF C_{chan} V_{TL} to V_{CHRG}
t_{W1L}	90		610	us	
t_{SSW}	0.77	1.1	1.43	ms	PD capture measured from falling edge V_{TL}
t_{W0L}	1.8	2.0	2.2	ms	PSE hold time for Write 0 symbol
t_{REC}	270	300	330	us	Charge PD SCCP reservoir capacitor
t_{CHRG}	200			us	Critical PD SCCP reservoir capacitor charging region
$t_{WRITESLOT}$			2.78	ms	

Red indicates changed parameters
***Bold** indicates parameters captured in SCCP electrical requirements*

Read 0/1 slot timing proof

Symbol	Min	Typ	Max	Unit	Note
t_F			**250**	us	5V pu vs 100Ohm pd
t_R			**500**	us	9mA PSE pu / 0.4uF C_{chan} V_{TL} to V_{CHRG}
t_{W1L}	90		**610**	us	
t_{MSR}	**0.9**	1	**1.1**	ms	PSE capture, from falling edge V_{TL}
t_{ROL}	**1.75**	2.5	**3.25**	ms	PD release, from falling edge V_{TL}
t_{REC}	**270**	300	**330**	us	Charge PD SCCP reservoir capacitor
t_{CHRG}	**200**			us	Critical PD SCCP reservoir capacitor charging region
$t_{READSLOT}$			**3.83**	ms	Read symbol duration

Red indicates changed parameters
***Bold** indicates parameters captured in SCCP electrical requirements*

Conclusion

- Technical feasibility has been established
- Ongoing mixed signal, system level validation
- Track 10SPE developments