Canova Tech

The Art of Silicon Sculpting

PIERGIORGIO BERUTO

ANTONIO ORZELLI

IEEE 802.3cg

PLCA strict precedence mode

November 7th, 2018

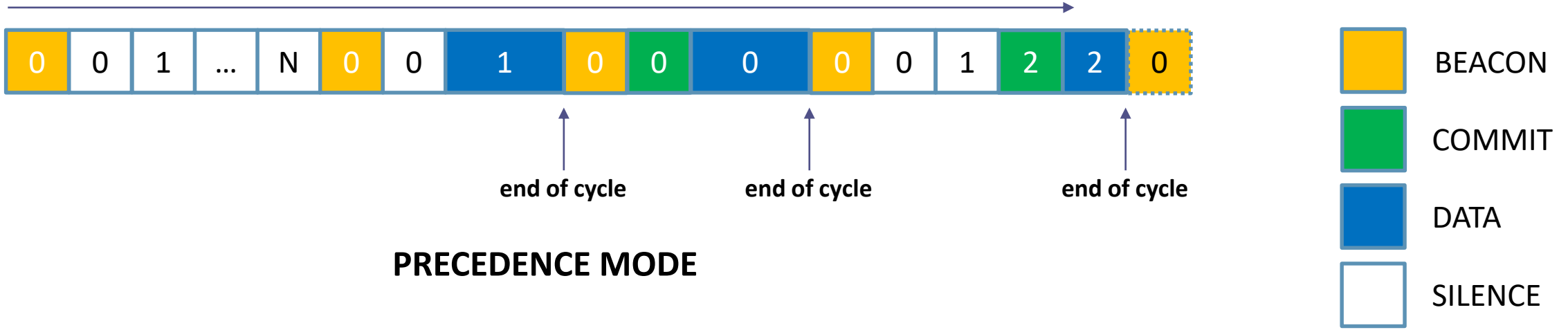
Outline

- Request from Michael Rentschler and Venkat Iyer (Microchip) for having prioritization features in PLCA: http://www.ieee802.org/3/cg/public/adhoc/iyer_rentschler_3cgah_01_102418.pdf
  - Prioritization based on PLCA node ID assignment (0 = highest)
    - Similar to CAN bus
  - Requires multiple ID assignment for dynamic prioritization
    - As pointed out in the 24th October 2018 ad-hoc, this has scope issues for 802.3cg
    - discussion is ongoing in the NEA as well
  - Based on explicit signaling which can trigger physical collisions (PRQ) at specific times
    - not really inline with PLCA (which avoids physical collisions)
    - yields multiple subtle implications which would require careful changes in C148 and C147
- This presentation provides a simpler, equivalent alternative for static precedence
  - In scope with 802.3cg
  - **Optional** - Enabled by management entity (disabled by default)
  - Not based on explicit signaling
  - Not mutually exclusive with proposed PLCA burst mode, combined give maximum flexibility

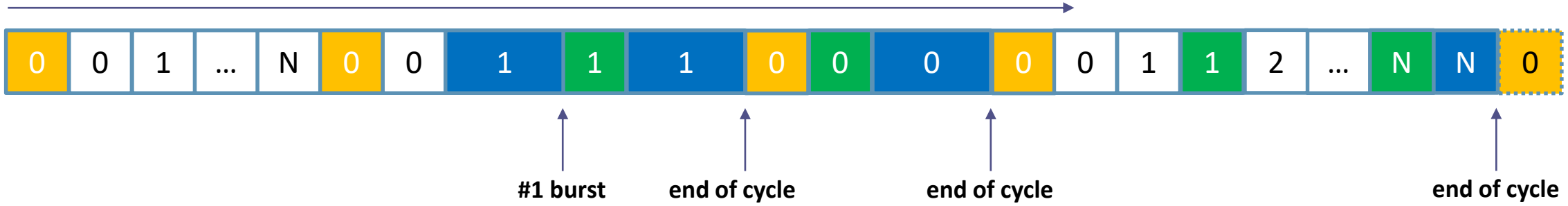
Proposed solution

- Working principle:
  - PLCA cycle terminates after ANY packet is sent by any node
  - PLCA "master" sends a new BEACON to start a new cycle after (at least) one IPG
- What you get is:
  - As long as a node with lower ID (higher priority) has something to send, other nodes with higher IDs will wait
  - After a node transmitted a packet, higher priority nodes would get a chance to transmit again because the cycle starts over
  - That is: **strict, static precedence**

Example



PRECEDENCE MODE



COMBINED WITH BURST MODE
(node #1 configured for max_bc = 1)

Changes to State Diagrams (C148)

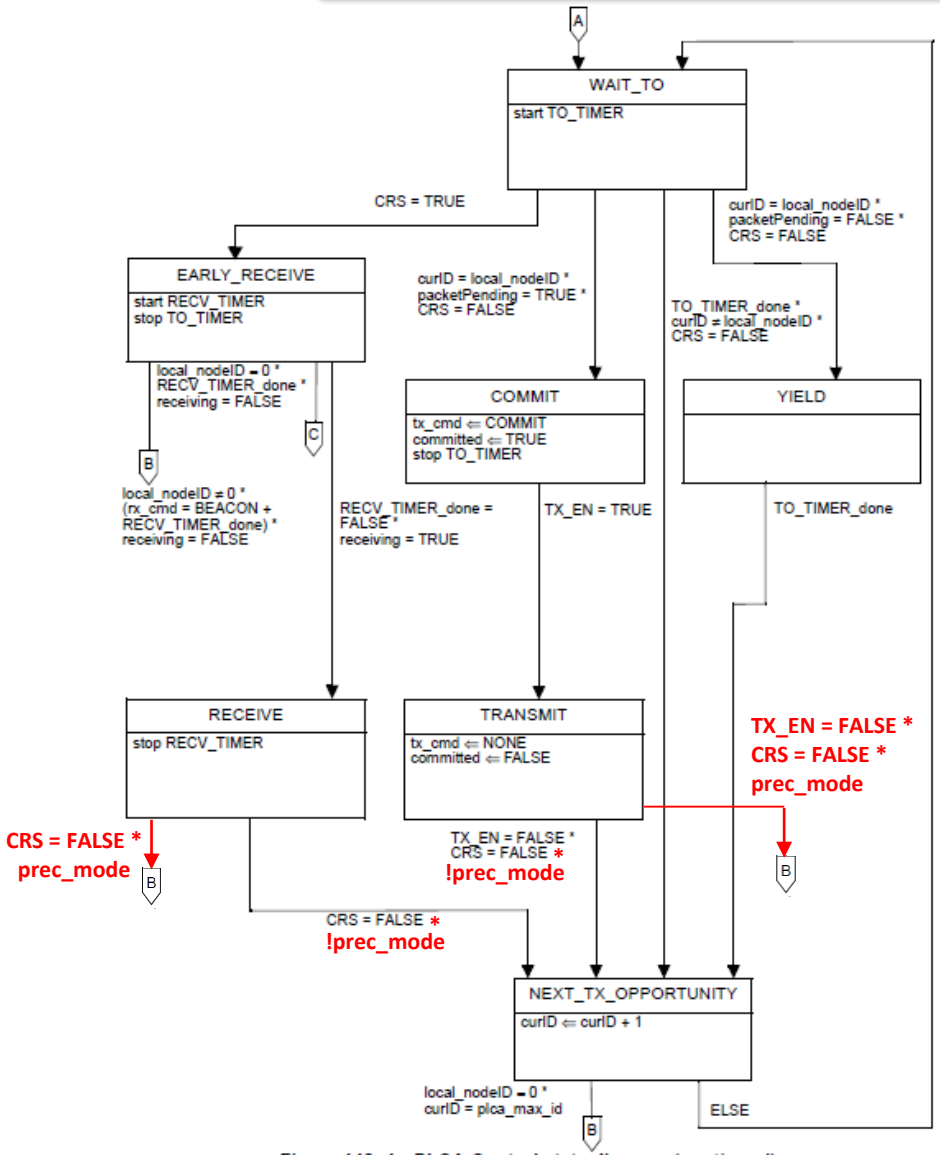


Figure 148–4—PLCA Control state diagram *(continued)*

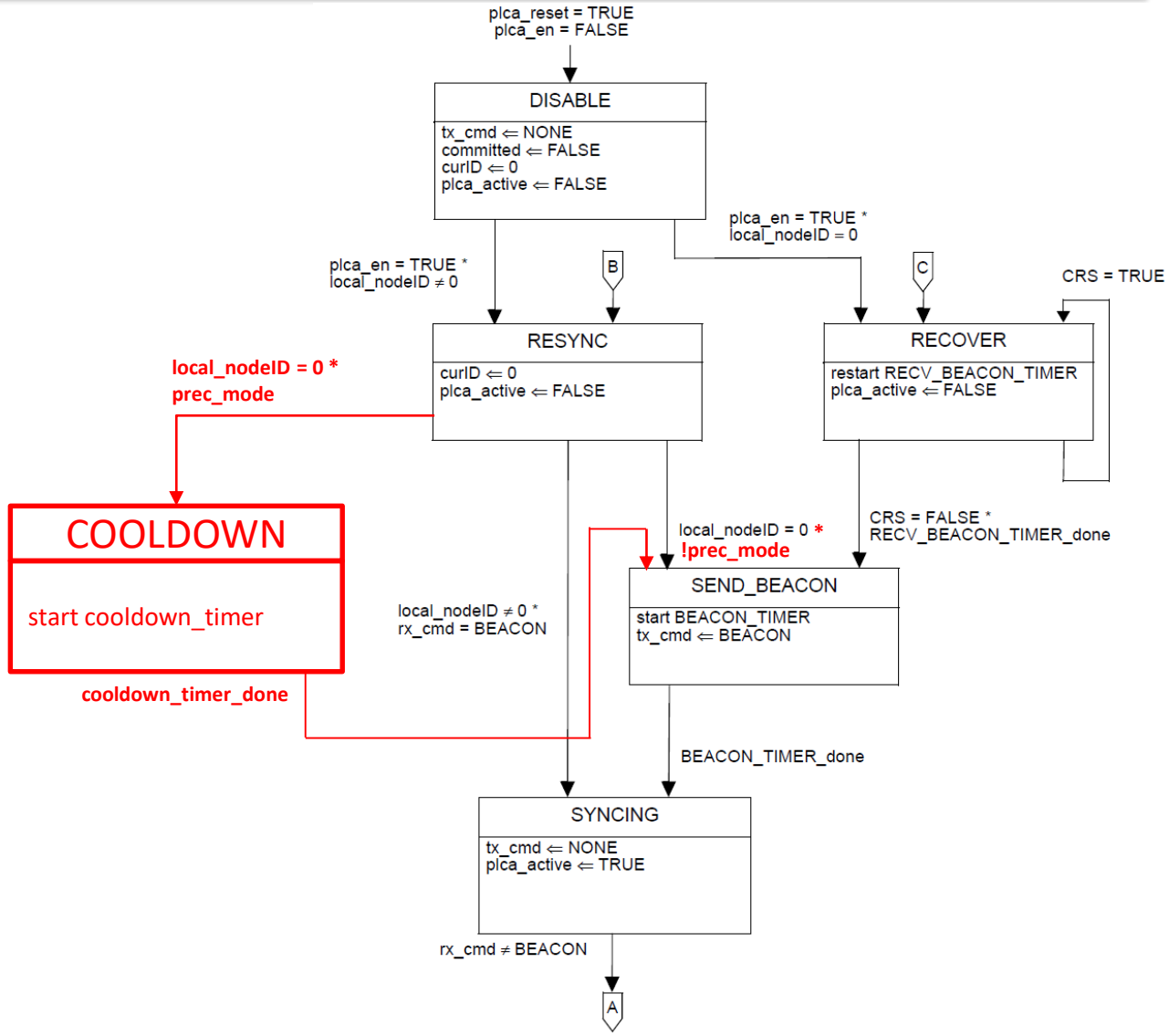


Figure 148–4—PLCA Control state diagram

Text Changes (C148)

148. Overview → add text marked in red

Transmit opportunities are generated in a round-robin fashion every time the PHY with node ID = 0 signals a BEACON on the medium, indicating the start of a new cycle. This happens after each node has had a transmission opportunity.

When the optional PLCA strict precedence mode is supported and enabled, instead, the PLCA cycle ends each time a packet is transmitted. As a result, nodes with higher ID will not get an opportunity to transmit until all lower ID nodes yield their transmit opportunity.

PLCA relies…

Text Changes (C148)

148.4.5.2 → add the following variable description

prec_mode

PLCA precedence mode enable. This signal maps to aPLCAPrecedenceMode attribute. When MDIO is present, prec_mode is configured to the content of bit 28.4.15. When MDIO is not present, the functionality of bits 28.4.15 can be provided by equivalent means.
Value: TRUE or FALSE

148.4.5.4 → add the following timer description

cooldown_timer

when precedence mode is enabled, counts the time to wait after any reception or transmission before sending a new BEACON. This signal maps to aPLCACooldownTimer attribute. When MDIO is present, cooldown_timer is configured to the content of bit 28.4.7:0. When MDIO is not present, the functionality of bits 28.4.7:0 can be provided by equivalent means. For PLCA precedence mode to work properly this timer should be set greater than one IPG.
Duration: integer number between 0 and 255, expressed in bit times

Text Changes (C30)

Add the following lines (marked in red) to table 30-1c under oPLCA managed object class (30.3.9) section:

	aPLCATransmitOpportunityTimer	ATTRIBUTE	GET-SET									X																			
	aPLCAPrecedenceMode	ATTRIBUTE	GET-SET									X																			
	aPLCACooldownTimer	ATTRIBUTE	GET-SET									X																			

Text Changes (C30)

Add the following subclauses in 30.3.9.2:

30.3.9.2.x aPLCAPrecedenceMode

ATTRIBUTE APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries: TRUE FALSE

BEHAVIOUR DEFINED AS:

When this value is set to TRUE the PLCA RS behaves in strict precedence mode as described in 148.2 and 148.4.5. This attribute is FALSE by default.;

30.3.9.2.y aPLCACooldownTimer

ATTRIBUTE APPROPRIATE SYNTAX:

INTEGER VALUE in the following range (inclusive): 0 to 255

BEHAVIOUR DEFINED AS:

This value is assigned to set the amount of time, expressed in bit times, the PLCA RS waits before sending a new BEACON when aPLCAPrecedenceMode is set to TRUE. The default value of aPLCACooldownTimer is 128.

Make the following changes to Table 45-351a:

28.2	PLCA TO Timer	45.2.13.3
28.3 ~~through 28.4~~	Reserved	
28.4	PLCA Precedence Mode Control	45.2.13.x
28.5, 28.6	PLCA devices in package	45.2.13.4

Append the following subclause to 45.2.13

45.2.13.x PLCA Precedence Mode Control register (Register 28.4)

The assignment of bits in the PLCA Precedence Mode Control register is shown in Table 45–351x.

Table 45-351x - PLCA Precedence Mode bit definitions

Bit(s)	Name	Description	R/W[25]
28.4.15	prec_mode	1 = PLCA behaves in strict precedence mode 0 = PLCA behaves in round-robin mode	R/W
28.4.7:0	cooldown_timer	8 bit field indicating the number of bit times PLCA wait before sending a new BEACON when prec_mode = 1	R/W

45.2.13.x.1 prec_mode (28.4.15)

PLCA precedence mode enable. When this bit is set to one, the PLCA RS behaves in strict precedence mode as described in 148.2 and 148.4.5. The default value of bit 28.4.15 is 0.

45.2.13.x.2 cooldown_timer (28.4.7:0)

Indicates the amount of time, expressed in bit times, the PLCA RS waits before sending a new BEACON when prec_mode = 1. The default value of cooldown_timer is 128.

THANK YOU!