TRUE	Transmission is enabled.
FALSE	Transmission is disabled.

Circular object in the margin denotes edit in the text in that area.

146.2.9.2 When generated

PCS Data Transmission Enable function generates PMA_TXEN.request messages to indicate a change in tx_enable_mii variable.

146.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 146–14 and Figure 146–15.

146.2.10 PMA_RX_LPI_STATUS.request (rx_lpi_active)

When the PHY supports the EEE capability, this primitive is generated by the PCS receive function to indicate the status of the receive link of the local PHY. The parameter PMA_RX_LPI_STATUS.request conveys to the PMA receive function and the PMA PHY control function information regarding whether the PCS receive function is in the LPI receive mode.

146.2.10.1 Semantics of the primitive

PMA_RX_LPI_STATUS.request (rx_lpi_active)

The rx_lpi_active parameter can take on one of two values of the following form:

TRUE	The PCS receive function is in the LPI receive mode.
FALSE	The PCS receive function is not in the LPI receive mode.

146.2.10.2 When generated

The PCS generates PMA_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as described in Figure 146–8 and Figure 146–9.

146.2.10.3 Effect of receipt

The receiver may adjust the link training and clock recovery while being in low power idle mode. Additionally, checking of the descrambler status in the PHY control state diagram is suppressed, as the receiver is disabled.

146.2.11 PMA_TX_LPI_STATUS.request (tx_lpi_active)

When the PHY supports the EEE capability, this primitive is generated by the PCS transmit function to indicate the status of "Assert Low Power Idle" on the MII. The parameter PMA_TX_LPI_STATUS.request conveys to the PMA control function information regarding whether the PCS transmit function is receiving "Assert Low Power Idle" on the MII.

146.2.11.1 Semantics of the primitive

PMA_TX_LPI_STATUS.request (tx_lpi_active)

The tx_lpi_active parameter can take on one of two values of the following form:

TRUE	The PCS transmit function is receiving "Assert Low Power Idle" on the MII.

FALSE	The PCS transmit function is not receiving “Assert Low Power Idle” on the MII.

146.2.11.2 When generated

The PCS generates PMA_TX_LPI_STATUS.request messages to indicate a change in the tx_lpi_active variable to the PMA PHY control function. Tx_lpi_active is set to true if “Assert Low Power Idle” is received from the MII, otherwise it is set to false.

unneeded comma

146.2.11.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 146–14 and Figure 146–15.

146.2.12 PMA_TX_LPI_STATUS.indication

When the PHY supports the EEE capability this primitive is generated by the PMA PHY control function to indicate a sleep or wake event. The parameter PMA_TX_LPI_STATUS.indication conveys to the PCS transmit function information regarding whether the PHY should indicate a sleep or a wake event to the remote PHY.

146.2.12.1 Semantics of the primitive

PMA_TX_LPI_STATUS.indication (loc_lpi_req)

The loc_lpi_req parameter can take on one of two values of the following form:

TRUE	Communicate to the remote PHY that LPI mode will be entered by the local PHY.
FALSE	Communicate to the remote PHY that normal IDLE mode will be entered by the local PHY.

146.2.12.2 When generated

The PMA generates PMA_TX_LPI_STATUS.indication messages to indicate a change in the loc_lpi_req variable as described in Figure 146–14 and Figure 146–15.

146.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in 146.3.3.2.4.

146.3 Physical Coding Sublayer (PCS) functions

The Physical Coding Sublayer (PCS) consists of PCS Reset, the PCS Data Transmission Enable, PCS Transmit, and PCS Receive functions as shown in Figure 146–3. The PCS Reset function is explained in 146.3.1, the PCS Data Transmission Enable function is explained in 146.3.2, the PCS Transmit function is explained in 146.3.3, the PCS Receive function is explained in 146.3.4, and the PCS Loopback function is explained in 146.3.5.

146.3.1 PCS Reset Function

PCS reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 36.2.5.1.3).

a) The receipt of a request for reset from the management entity.

TX_EN

The TX_EN signal of the MII as specified in 22.2.2.3.

TX_ER

The TX_ER signal of the MII as specified in 22.2.2.5.

tx_mode

The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

146.3.3 PCS Transmit

146.3.3.1 PCS Transmit State Diagram

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 146–5, and the associated state variables, functions, timers and messages.

In each symbol period PCS Transmit generates a symbol A_n provided to the PMA, operating in one of three different modes (tx_mode), where symbol A_n is a ternary code that can take values of {-1, 0, +1}. The PMA transmits symbol A_n over the wire pair BI_DA. The integer, n, is a time index, introduced to establish a temporal relationship between different symbol periods. The nominal symbol clock frequency is specified in 146.5.4.5.

Upon the assertion of TX_EN, the PCS Transmit function passes an SSD of 12 consecutive symbols to the PMA, which replaces the first 16 bits of the preamble. Following SSD, TXD[3:0] is encoded into ternary symbols using encoding rules specified in 146.3.3.2.5, until TX_EN is de-asserted.

Following the de-assertion of TX_EN, a special code ESD (or ERR_ESD when a transmit error is encountered, which means that TX_ER was high at any point during the transmission) of 12 consecutive symbols is generated, after which the transmission of idle mode according to 146.3.3.2.5 is resumed.

10BASE-T1L has one special symbol triplet (0, 0, 0) that is not used by Idle or Data symbols. Therefore this symbol triplet will be used for the COMMA symbols within the delimiters. See Figure 146–5 for more details.

The 10BASE-T1L PHY supports normal operation and link training operation. In training operation, the PCS ignores signals from the MII and sends only the idle signals to the PMA until the training process is complete.

If tx_mode has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA.

If tx_mode has the value SEND_I, PCS Transmit generates sequences of symbols according to the encoding rule in idle mode as described in 146.3.3.2.5.

If tx_mode has the value SEND_N, PCS Transmit generates symbols A_n at each symbol period representing data, special control symbols like SSD/ESD or IDLE symbols as defined in 146.3.3.2.5. The transition from idle to data is signaled by an SSD and the end of transmission of data is signaled by an ESD.

unneeded comma

During training operation (when tx_mode is SEND_I), knowledge of the transmitted symbols may be used at the receiver side to perform any signal conditioning necessary for meeting the required performance during normal operation. When the link is up, the PHY enters SEND_N mode and the transmitted PAM3 symbols are used at the receiver PHY for continued clock frequency/phase tracking.

146.3.3.2.4 Generation of scrambled bits $Sd_n[3:0]$

From scrambler bits $Sc_n[3:0]$ and $TXD_n[3:0]$, bits $Sd_n[3:0]$ shall be generated as follows:

$$Sd_n[3] = \begin{cases} Sc_n[3] \wedge TXD_n[3] & \text{if (tx\_enable\_mii = TRUE)} \\ Sc_n[3] \wedge 1 & \text{else if (loc\_rcvr\_status = OK)} \\ Sc_n[3] & \text{else} \end{cases}$$

$$Sd_n[2] = \begin{cases} Sc_n[2] \wedge TXD_n[2] & \text{if (tx\_enable\_mii = TRUE)} \\ Sc_n[1] \wedge 1 & \text{else if (loc\_lpi\_req = TRUE)} \\ Sc_n[1] & \text{else} \end{cases}$$

$$Sd_n[1:0] = \begin{cases} Sc_n[1:0] \wedge TXD_n[1:0] & \text{if (tx\_enable\_mii = TRUE)} \\ (Sc_n[2], Sc_n[0]) & \text{else} \end{cases}$$

Note that during transmission of idles, bits $Sc_n[1]$ and $Sc_n[2]$ shall be swapped compared to data transmission which can be used to reliably distinguish idle data transmission from data transmission at the receiver side.

146.3.3.2.5 Generation of ternary triplet in mode SEND_N and SEND_I

The scrambled bits $Sd_n[3:0]$ shall be converted to a ternary triplet (TAn, TBn, TCn) using the 4B3T algorithm in conjunction with a running disparity value, shown in Table 146–1. The 4B3T coding is DC-free. To achieve this, the difference between the number of transmitted "+1" and "-1" symbols is limited. The running disparity is reflecting this actual difference and depending on the running disparity the next symbol coding is chosen. The same ternary symbol encoding is used while in SEND_I and SEND_N.

unneeded comma

The ternary symbol triplet (0, 0, 0) is used as the COMMA value and never occurs during normal 4B3T mapping. This can also be used to synchronize the receiver's demultiplexer triplet boundary during training.

The DISPRESET3 triplet, together with the following fourth symbol group (which always has a disparity of 1), shall be used to bring back the running disparity to a defined value of 2. The coding shown in Table 146–2 shall be used for the DISPRESET3 symbol triplet:

supposed to be a period?

The fourth symbol group (SSD4/ESD4/ESD_ERR4) shall be encoded as shown in Table 146–3 (all have disparity of +1):

146.3.3.2.6 Generation of ternary triplet in mode SEND_Z

The ternary triplet (TA_n, TB_n, TC_n) shall be a zero vector (0, 0, 0) when tx_mode = SEND_Z.

146.3.3.2.7 Generation of symbol sequence

A ternary triplet (TA_n, TB_n, TC_n) shall be a sent in the following order: TA_n, TB_n, TC_n, TA_{n+1}, TB_{n+1}, TC_{n+1}, ...

146.3.4 PCS Receive

146.3.4.1 PCS Receive overview

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 146–8, and associated state variables.

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The PCS Receive function shall conform to the JAB state diagram in Figure 146–10. This prevents the possible lock-up of the PCS Receive state diagram in the DATA state due to mis-detection of an ESD. The maximum dwelling time in DATA state shall be less than the period specified for rcv_max_timer. When rcv_max_timer expires, the PCS Receive state machine is reset and transition to IDLE state is forced.

In Figure 146–8, there are a total of five states after SSD4 detection before the DATA state; meanwhile, there are also five states before the IDLE state (including the DATA state) that perform data decoding. As a result, the depth of the data flush-in delay line is the same as the flush-out delay line ensuring correct packet reception at the MII.

The variables, functions, and timers used in Figure 146–8, Figure 146–9, and Figure 146–10 are defined as below. For the definition of IDLE, COMMA, DISPRESET3, SSD4, ESD4 and ERR_ESD4, see 146.3.3.2.5.

146.3.4.3 PCS Receive descrambler polynomial

The PHY shall descramble the data stream and return the proper sequence of code-groups to the decoding process for generation of RXD<3:0> to the MII. For side-stream descrambling, the MASTER PHY shall employ the following receiver descrambler generator polynomial:

$$g'_M(x) = 1 + x^{20} + x^{33} \quad (146–4)$$

and the SLAVE PHY shall employ the following receiver descrambler generator polynomial:

$$g'_S(x) = 1 + x^{13} + x^{33}. \quad (146–5)$$

146.3.4.4 PCS Receive automatic polarity detection

An automatic polarity detection and correction shall be implemented on the receive side of both master and slave PHY.

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Polarity can be automatically detected in a recursive process: one assumption of polarity is made first and the descrambler synchronization is monitored within a certain period to determine whether such an assumption is correct; if not, the same procedure is repeated with a different polarity assumption and vice versa.

Receive polarity detection and correction can be done simultaneously at the earliest link up stages. Link up starts with the MASTER PHY sending symbols to the SLAVE PHY. If a polarity flip is detected, the SLAVE changes the sign of its received signals (RA_n, RB_n, RC_n) to correct the polarity. There is no change in the polarity of the transmit signal. After the SLAVE PHY has started transmission, the MASTER PHY can use the same method for determining its receive polarity.

146.3.5 PCS Loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, or the loopback bit in MDIO register 3.2278.14, defined in 45.2.3.58a.2, is set to a one (or PCS loopback mode is enabled by a similar functionality if MDIO is not implemented). In this mode, the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium.

146.4 Physical Medium Attachment (PMA) Sublayer

The PMA couples messages from the PMA service interface specified in 146.3 onto the 10BASE-T1L physical medium, and provides the link management and PHY Control functions. The PMA provides full duplex communications to and from medium employing 3-level Pulse Amplitude Modulation (PAM3). The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 146.8.

PMA Reset shall set pma_reset = ON while any of the above reset conditions hold true. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

146.4.2 PMA Transmit function

Figure 146–12 illustrates the signal flow of the 10BASE-T1L PMA Transmit function. During transmission, PMA_UNITDATA.request conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over the single transmit pair.

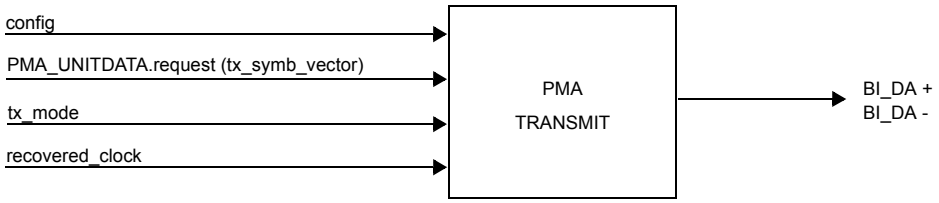

Figure 146–12—PMA Transmit

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A single transmitter is used to generate the PAM3 signal BI_DA on the wire, using the transmit clock, TX_TCLK (see 146.5.4.5). When the config parameter is set to MASTER, the PMA Transmit function derives the TX_TCLK from a local clock source. When the config parameter is set to SLAVE, the PMA Transmit function derives the TX_TCLK from the recovered clock.

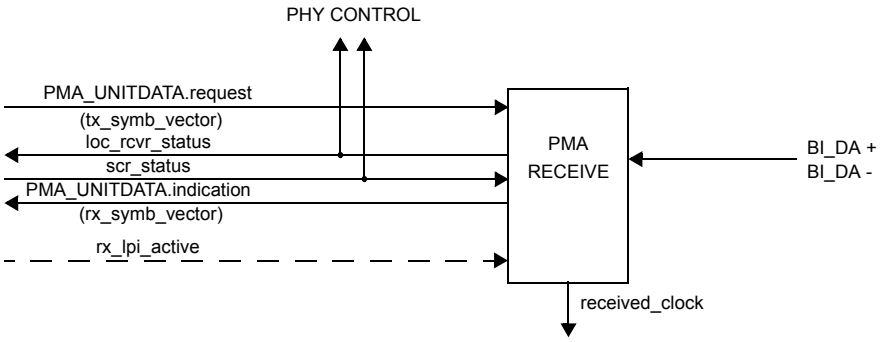
The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

146.4.3 PMA Receive function

Figure 146–13 illustrates the signal flow of the 10BASE-T1L PMA Receive function.

The 10BASE-T1L PMA Receive function comprises a single receiver (PMA Receive) for PAM3 modulated signals on a single balanced pair, BI_DA. PMA Receive has the ability to translate the received signals on at the MDI into the PMA_UNITDATA.indication parameter rx_symb_vector. It detects ternary symbol sequences from the signals received at the MDI and presents these sequences to the PCS Receive function. The parameter loc_rcvr_status is generated by PMA Receive to indicate the status of the receive link at the local PHY. This variable indicates to the PCS Transmitter, PCS Receiver, and PMA PHY Control function whether the status of the overall received link is ok or not. Signal scr_status is generated by the PCS

Receiver to indicate the status of the descrambler to the local PHY. It conveys the information on whether the scrambler has achieved synchronization or not to the PMA receive function.



NOTE—Signals shown with dashed lines are required only for EEE functionality.

Figure 146–13—PMA Receive

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, ~~then~~ this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.174b.7.

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146.4.4 PHY Control function

For the 10BASE-T1L PHY, FORCE mode or Auto-Negotiation can be used to achieve link acquisition between two 10BASE-T1L link partners. Using FORCE mode, the configuration of the PMA is pre-determined to be MASTER or SLAVE via management control during initialization or via default hardware set-up. Using Auto-Negotiation, the configuration of the PMA is determined during the auto-negotiation process.

The PHY Control functions block governs the control actions needed to bring the PHY into the 10BASE-T1L mode of operation so that frames can be exchanged with the link partner. PMA PHY Control also generates the signals that control PCS and PMA sublayer operations. It determines whether the PHY operates in the normal mode, enabling data transmission over the link segment, or whether the PHY sends idle data. PHY Control shall comply with the state diagram shown in Figure 146–14 and Figure 146–15. PHY Control sets tx_mode to SEND_N (transmission of normal MII Data Stream, Control Information, or Idle Data), SEND_I (transmission of Idle Data), or SEND_Z (transmission of zero symbol vectors)

There shall be two startup sequences, depending on which training time is needed during the startup. If there is no predetermined configuration available, the maximum time, until link_status = OK is reached, shall be less than 3000 ± 30 ms. If there is a predetermined configuration available (a set of valid filter coefficients is available), the maximum time from power_on = FALSE to link_status = OK shall be less than 100 ms.

NOTE - Fast startup is expected to be limited to very short link segment length only, where a predetermined configuration is available and where the change in ambient conditions has no significant influence on the available predetermined configuration or filter coefficient set.

146.4.4.1 Variables

pma_reset
: Allows reset of all PMA functions.
Values: ON or OFF
Set by: PMA Reset

link_control

This variable is generated by management or set by default.
Values: ENABLE or DISABLE

config

The config parameter is set by management, set by default or set by auto-negotiation and passed to the PMA and PCS.
Values: MASTER or SLAVE

loc_lpi_req:

The variable loc_lpi_req is set TRUE if low power idle mode is requested by the PMA PHY control function.
unneeded comma
Values: TRUE or FALSE

loc_rcvr_status

Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive function for the local PHY.
Values: OK: The receive function for the local PHY is operating reliably.
NOT_OK: Operation of the receive function for the local PHY is unreliable.

lpi_enabled

This variable indicates whether Energy Efficient Ethernet is enabled for the PHY or not. If MDIO is implemented, it reflects bit 1.2294.10 as described in 45.2.1.174a.

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive function for the remote PHY is detected or not.
Values: TRUE: The receive function for the remote PHY is operating reliably.
FALSE: Reliable operation of the receive function for the remote PHY is not detected.

rx_lpi_active

This variable indicates to the PMA receive function if the receive state machine is in low power idle state.
unneeded comma
Values: TRUE or FALSE

scr_status

The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.
Values: OK: The descrambler has achieved synchronization.
NOT_OK: The descrambler is not synchronized.

tx_enable_mii

The tx_enable_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 146–4. When set to FALSE transmission is disabled; when set to TRUE transmission is enabled.
semicolon
Values: TRUE or FALSE

tx_lpi_active

This variable indicates to the PMA PHY control function whether the “Assert Low Power Idle” condition on the MII is active.
Values: TRUE or FALSE

tx_mode

PCS Transmit sends code-groups according to the value of this variable.
Values: SEND_N: This value is continuously asserted when transmitting data, control information or idle during normal operation.
SEND_I: This value is continuously asserted when transmitting idle data during training.
SEND_Z: This value is asserted when transmitting zero code-groups.

146.4.5 Link Monitor function

Link Monitor operation, as shown in state diagram of Figure 146–16, shall be provided to support PHY Control. Variable link_control is set to ENABLE through management control during the PHY initialization or via default hardware set-upVariables

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tx_mode

The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

146.4.5.1 State diagram

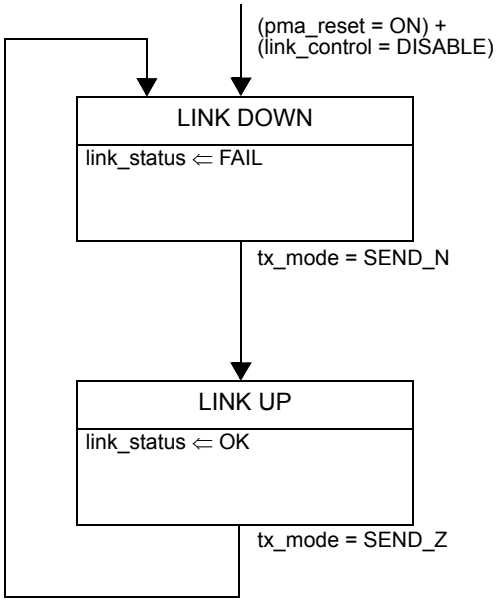

Figure 146–16—PHY Link Monitor state diagram

146.4.6 PMA clock recovery

This PMA function recovers the clock from the received stream. It is coupled to the receiver in order to provide for the SLAVE PHY a clock synchronous to the transmit clock of the MASTER PHY.

146.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA for a 10BASE-T1L Ethernet PHY.

146.5.1 EMC tests

Direct Power Injection (DPI) and 150 Ω emission tests for noise immunity and emission as per 146.5.1.1 and 146.5.1.2 may be used to establish a baseline for PHY EMC performance. These tests provide a high

degree of repeatability and a good correlation to immunity and emission measurements. Additional tests may be needed to verify EMC performance in various configurations, applications, and conditions.

146.5.1.1 Immunity - DPI test

In a real application radio frequency (RF) common mode (CM) noise at the PHY is the result of electromagnetic interference coupling to the cabling system. Additional differential mode (DM) noise at the PHY is generated from the CM noise by mode conversion of all parts of the cabling system and the MDI. The sensitivity of the PMA's receiver to RF CM noise may be tested according to the DPI method of IEC 62132-4, and may need to comply with more stringent requirements as agreed upon between customer and supplier.

146.5.1.2 Emission - Conducted emission test

The emission of the PMA transmitter to its electrical environment may be tested according to the 150 Ω direct coupling method of IEC 61967-4, and may need to comply with more stringent requirements as agreed upon between customer and supplier.

146.5.2 Test modes

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The test modes described in this sub clause shall be provided to allow testing of the transmitter waveform, transmitter distortion, transmitter jitter, and transmitter droop. The test modes can be enabled by setting bits 1.2298.15:13 (10BASE-T1L PMA/PMD Test Control Register) of the PHY Management register set as described in 45.2.1.174c.1. If MDIO is not implemented a similar functionality shall be provided by another interface. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

a) Test mode 1 - Transmitter output voltage and timing jitter test mode
b) Test mode 2 - Transmitter output droop test mode
c) Test mode 3 - Normal operation in Idle mode. This is for the PSD Mask test.

When test mode 1 is enabled, the PHY shall repeatedly transmit the data symbol sequence (+1, -1). See 146.5.4.5 for transmit clock requirements.

When test mode 2 is enabled, the PHY shall transmit ten "+1" symbols followed by ten "-1" symbols. This sequence is repeated continually.

146.5.3 Test fixture

The test fixture shown in Figure 146–17, or its equivalent, is being used in the stated respective tests for measuring the transmitter specifications. The tolerance of the termination resistor shall be ± 0.1 %. All the transmitter tests are defined at the MDI.

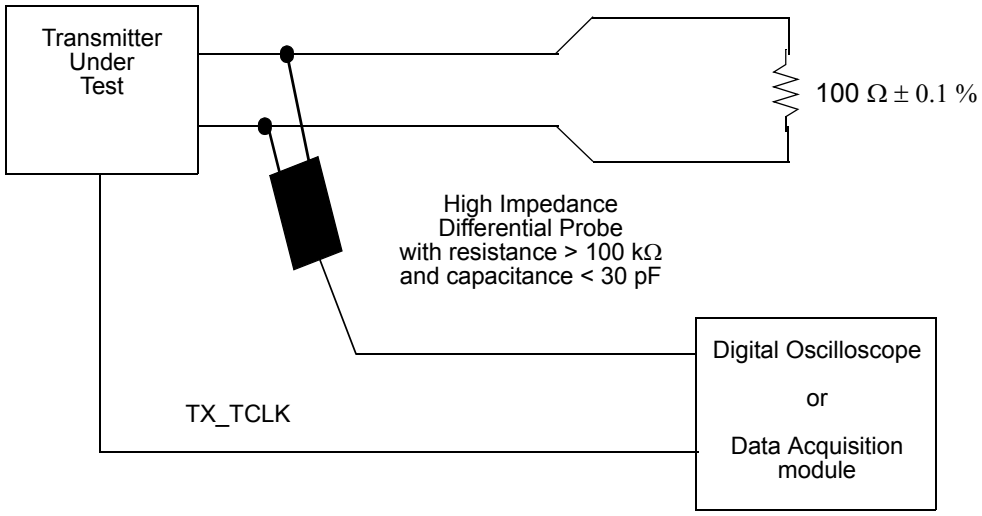

Figure 146–17—Test fixture

To allow an easy synchronization of the measurement equipment, the PHY shall provide access to the symbol rate clock TX_TCLK, which times the transmitted symbols. For a MASTER PHY this is the output of the (divided) clock oscillator, for the SLAVE PHY this is the recovered clock.

146.5.4 Transmitter electrical specifications

The PMA shall operate with AC coupling to the MDI. Where a load is not specified, the transmitter shall meet the requirements of this section with a 100 Ω ± 0.1 % resistive differential load connected to the transmitter output.

146.5.4.1 Transmitter output voltage

Transmitter output voltage shall be tested using test mode 1 in combination with the test fixture shown in Figure 146–17. The transmitter output voltage shall be 2.4 V ± 5 % peak-to-peak (for the 2.4 Vpp operating mode) and 1.0 V ± 5 % peak-to-peak (for the 1.0 Vpp operating mode). Transmitter output voltage can be set using the management interface or by hardware default set-up. Additionally, Auto-Negotiation can be used to find a common transmitter output voltage for the two PHYs.

The transmitter driving level can be selected by setting bit 1.2294.12 (10BASE-T1L PMA control register) of the PHY Management register set as described in 45.2.1.174a.4. If MDIO is not implemented, a similar functionality shall be provided by another interface. The default setting is to use Auto-Negotiation, if available.

146.5.4.2 Transmitter output droop

Transmitter output droop shall be tested using test mode 2 in combination with the test fixture shown in Figure 146–17. The transmitter output droop shall be less than 20 %, taking the inner 9 bit times of the 10 bit times pulse duration.

146.5.4.3 Transmitter timing jitter

The transmitter symbol-to-symbol jitter shall be tested using test mode 1 in combination with the test fixture shown in Figure 146–17. The maximum jitter at the transmitter side shall be less than ± 10 ns symbol-to-symbol jitter.

146.5.4.4 Transmitter Power Spectral Density (PSD) and power level

In test mode 3 (reflecting normal operation), the transmit power shall be 8.8 ± 1.0 dBm for the 2.4 Vpp operating mode and 1.2 ± 1.0 dBm for the 1.0 Vpp operating mode. The power spectral density of the transmitter, measured into a 100 Ω load using the test fixture shown in Figure 146–18, shall be between the upper and lower masks specified in Equation (146–6) and Equation (146–7) for the 2.4 Vpp transmit amplitude, and by Equation (146–8) and Equation (146–9) for the 1.0 Vpp transmit amplitude. The masks are shown in Figure 146–19. The measurements need to be calibrated for insertion loss of the differential Balun used in the test. The resolution bandwidth of 10 kHz and sweep time of larger than 1 second are considered in the PSD measurement.

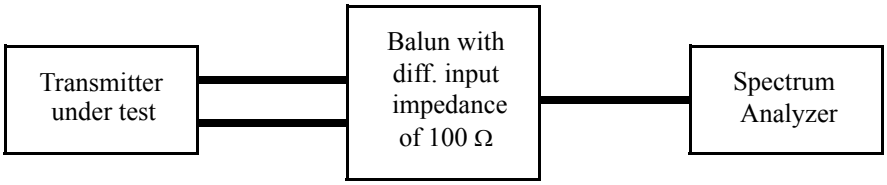

Figure 146–18—Transmitter test fixture for power spectral density measurement and transmit power level measurement

For the 2.4 Vpp transmit signal amplitude:

$$\text{Upper PSD Limit } (f) \geq \begin{cases} -55\,\text{dBm/Hz} & 0 \leq f \leq 2.5 \\ -55 - 1.5 \times (f - 2.5)\,\text{dBm/Hz} & 2.5 < f < 12.5 \\ -70\,\text{dBm/Hz} & 12.5 \leq f \leq 20 \end{cases} \quad (146\text{–}6)$$

$$\text{Lower PSD Limit } (f) \geq \begin{cases} -60\,\text{dBm/Hz} & 0.625 \leq f \leq 2.5 \\ -60 - 4 \times (f - 2.5)\,\text{dBm/Hz} & 2.5 < f \leq 5 \end{cases} \quad (146\text{–}7)$$

where f is the frequency in MHz, and for the 1.0 Vpp transmit signal amplitude:

$$\text{Upper PSD Limit } (f) \geq \begin{cases} -62.6\,\text{dBm/Hz} & 0 \leq f \leq 2.5 \\ -62.6 - 1.5 \times (f - 2.5)\,\text{dBm/Hz} & 2.5 < f < 12.5 \\ -77.6\,\text{dBm/Hz} & 12.5 \leq f \leq 20 \end{cases} \quad (146\text{–}8)$$

$$\text{Lower PSD Limit } (f) \geq \begin{cases} -67.6\,\text{dBm/Hz} & 0.625 \leq f \leq 2.5 \\ -67.6 - 4 \times (f - 2.5)\,\text{dBm/Hz} & 2.5 < f \leq 5 \end{cases} \quad (146\text{–}9)$$

where f is the frequency in MHz.

.

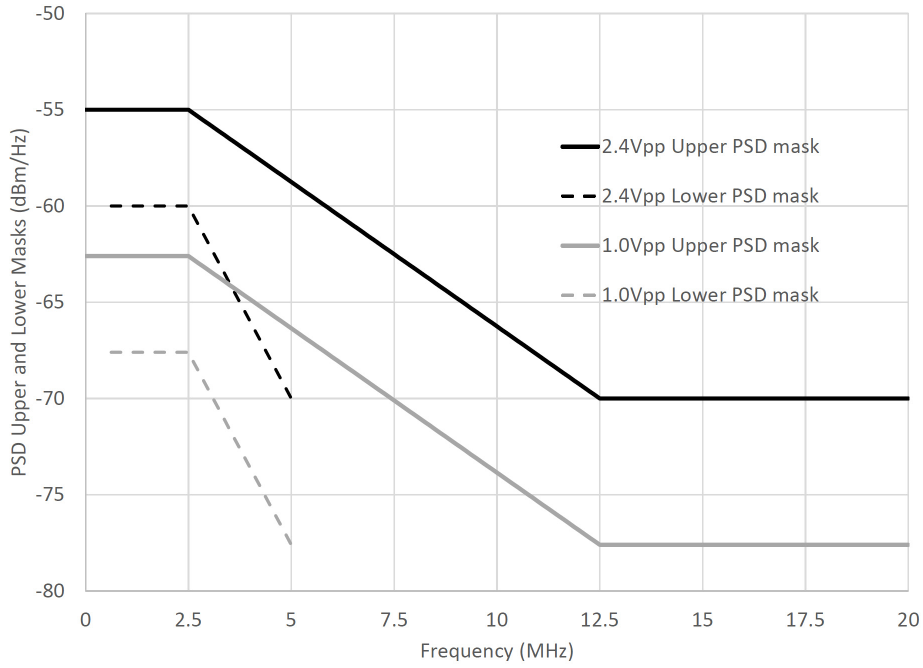

Figure 146–19—Transmitter Power Spectral Density, Upper and Lower Masks

146.5.4.5 Transmit clock frequency

The symbol transmission rate of the MASTER PHY shall be within the range 7.5 MBd ± 50 ppm.

146.5.5 Receiver electrical specifications

The PMA shall meet the requirements specified in PMA Receive function and the electrical specifications of this section. The link segment used in the test configurations shall be within the limits specified in 146.7.

146.5.5.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of Transmitter Electrical Specifications and have passed through a link segment specified in 146.7, shall be received with a bit error ratio less than 10^{-9}.

146.5.5.2 Receiver frequency tolerance

The receiver shall properly receive incoming data with a symbol rate within the range 7.5 MBd ± 50 ppm.

146.5.5.3 Alien crosstalk noise rejection

This specification is provided to verify the receiver's tolerance to alien crosstalk noise. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidth of 10 MHz and magnitude of –106 dBm/Hz. The receive DUT is connected to these noise sources through a resistive network, as shown in Figure 146–20, with a link segment as defined in 146.7. The noise is added at the MDI of the DUT. The BER is expected to be less than 10^{-9} and to satisfy this specification the frame loss ratio is less than 10^{-6} for 125 octet packets measured at MAC/PLS service interface.

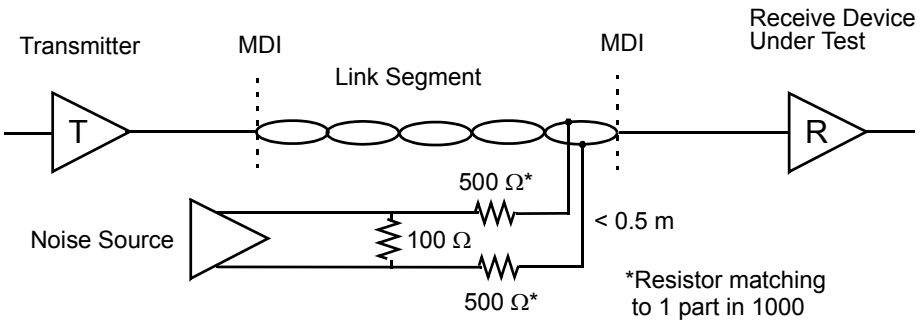

Figure 146–20—Alien crosstalk noise rejection test set-up

Note: If the output level is too high for the noise generator, the resistor divider network may be adopted to allow for a lower noise generator output level. The noise signal fed into the receiver shall have a magnitude of -106 dBm/Hz with a bandwidth of 10 MHz, taking the 100 ohm termination within the PHY into account.

146.5.6 Transmitter peak differential output

When measured with 100 Ω ± 0.1 % termination, the transmit differential signal at the MDI shall be less than 2.64 Vpp for the 2.4 Vpp operating mode and 1.10 Vpp for the 1.0 Vpp operating mode, including the signal droop. This limit applies to all transmit modes, including SEND_I and SEND_N modes.

146.5.7 PMA Local Loopback

The PMA local loopback function is optional. If supported, the PMA shall be placed in local loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, or the PMA loopback bit in MDIO register 1.2294.13, defined in 45.2.1.174a.3, is set to a one (or PMA loopback mode is enabled by a similar functionality if MDIO is not implemented). When the PHY is in the PMA local loopback mode, the PMA Receive function utilizes the echo signals from the unterminated MDI and decodes these signals to pass the data back to the MII Receive interface. The data flow of the external loopback is shown in Figure 146–21.

where

f is the frequency in MHz; $0.1 \le f \le 20$

The insertion loss is illustrated in Figure 146–23.

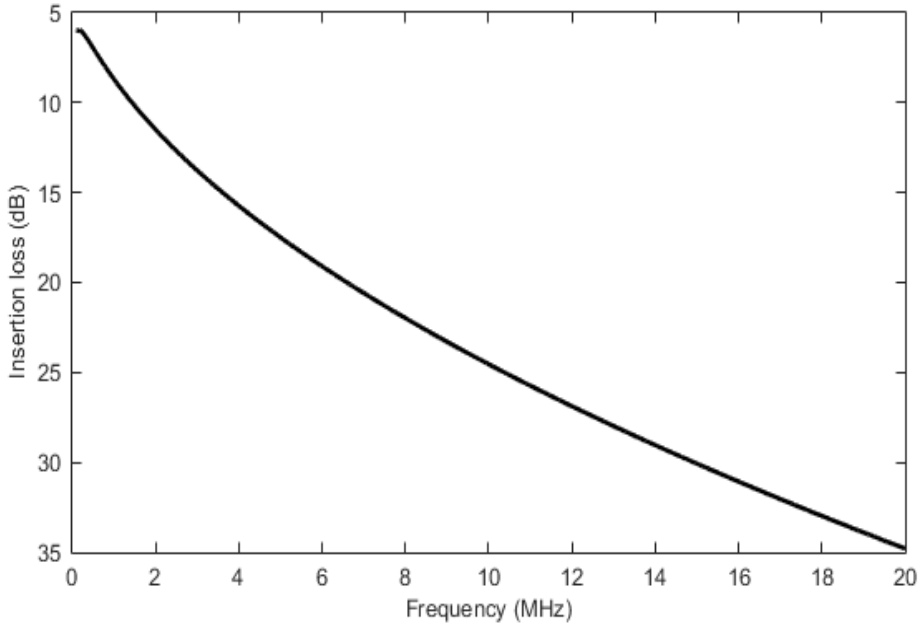

Figure 146–23—Insertion loss calculated using Equation (146–11)

146.7.1.2 Return loss

In order to limit the noise at the receiver due to impedance mismatches, each 10BASE-T1L link segment shall meet the values determined using Equation (146–12) at all frequencies from 0.1 MHz to 20 MHz. The reference impedance for the return loss specification is 100 Ω.

$$\text{Return Loss} \ge \begin{cases} 9 + 9 \times f \text{ dB} & 0.1 \le f < 0.5 \text{ MHz} \\ 13.5 \text{ dB} & 0.5 \le f \le 20 \text{ MHz} \end{cases} \text{ dB} \qquad (146\text{–}12)$$

where

f is the frequency in MHz; $0.1 \le f \le 20$

The return loss is illustrated in Figure 146–24.

146.8 MDI specification

This section defines the MDI for 10BASE-T1L.

146.8.1 MDI connectors

The mechanical interface to the balanced cabling is a 3-pin connector (BI_DA+, BI_DA-, and optional SHIELD) or alternatively a 2-pin connector with an optional additional mechanical shield connection which conforms to the link segment specification defined in 146.7.

146.8.2 MDI electrical specification

The MDI connector mated with a specified single balanced-pair connector shall meet the electrical requirements specified in 146.7.

146.8.3 MDI return loss

The MDI return loss (RL) shall meet or exceed Equation (146–17) for all frequencies from 100 kHz to 20 MHz (with 100 Ω ± 0.1 % reference impedance) at all times when the PHY is transmitting data or idle symbols.

$$\text{Return Loss}\,(f) \geq \begin{cases} 20 - 18 \times \log_{10}\left(\frac{0.2}{f}\right)\ \text{dB} & 0.1 \leq f < 0.2\ \text{MHz} \\ 20\ \text{dB} & 0.2 \leq f \leq 1\ \text{MHz} \\ 20 - 16.7 \times \log_{10}(f)\ \text{dB} & 1 < f \leq 10\ \text{MHz} \\ 3.3 - 7.6 \times \log_{10}\left(\frac{f}{10}\right)\ \text{dB} & 10 < f \leq 20\ \text{MHz} \end{cases}$$

where f is the frequency in MHz. (146–17)

146.8.4 MDI fault tolerance

For industrial applications, the wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential, or positive voltages of up to 60 V dc with the source current limited to 1200 mA, as per Table 146–8, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is/are removed.

The wire pair of the MDI shall also withstand, without damage, high-voltage transient noises and ESD per application requirements. The following table gives an overview about possible connection faults for the wire pair (BI_DA+ and BI_DA-):

Note: Typically industrial control circuits are SELV/PELV limited to a maximum voltage of 60 V. The maximum current is limited by the 50 ohm termination resistors in each signal line. Depending on the internal structure of the PHY IC, additional external clamping diodes could be necessary. Due to the AC signal coupling, the maximum current is only applied while charging the signal coupling capacitors.

146.9 Environmental specifications

146.9.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1 or IEC 62368-1 (for IT and industrial applications), to IEC 61010-1 (for industrial applications only, if required by the given application). All

Table 146–8—Fault conditions

BI_DA+	BI_DA-
BI_DA-	BI_DA+
Ground	No fault
No fault	Ground
Ground	Ground
+60 V dc	No fault
No fault	+60 V dc
+60 V dc	+60 V dc
Ground	+60 V dc
+60 V dc	Ground

equipment subject to this clause may be additionally required to conform to any applicable local, state, or national standards or as agreed to between the customer and supplier.

146.9.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner. In industrial applications, all 10BASE-T1L cabling shall be routed according to any applicable local, state or national standards considering all relevant safety requirements.

146.9.2.1 Environmental safety

In industrial applications, all equipment subject to this clause shall conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications, where applicable:

a) Environmental loads: IEC 60529 and ISO 4892
b) Mechanical loads: IEC 60068-2-6/31
c) Climatic loads: IEC 60068-2-1/2/14/27/30/38/52/78

Industrial environmental conditions are generally more severe than those found in many commercial environments. The targeted application environment(s) require careful analysis prior to implementation.

146.9.2.2 Electromagnetic compatibility

A system integrating the 10BASE-T1L PHY shall comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements as agreed upon between customer and supplier, for the limitation of electromagnetic interference.

In industrial applications a 10BASE-T1L PHY shall be tested according to the MICE classification depending on the intended electromagnetic classification (MICE E1 to MICE E3). Where applicable, also testing according to IEC 61326 and NE21 test methods, which are similar or even more severe than a MICE E3 environment shall be done and the following industrial EMC requirements shall be met:

a) Radiated/Conducted Emissions: IEC 61000-6-4
b) Radiated/Conducted Immunity: IEC 61000-4-3 and IEC 61000-4-6
c) Electrical Fast Transients: IEC 61000-4-4

147. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S

147.1 Overview

This clause defines the type 10BASE-T1S Physical Coding Sublayer (PCS) and type 10BASE-T1S Physical Medium Attachment (PMA) sublayer. Together, the PCS and PMA sublayers comprise a 10BASE-T1S Physical Layer (PHY). Provided in this clause are full functional and electrical specifications for the type 10BASE-T1S PCS and PMA.

The 10BASE-T1S PHY is a full/half-duplex point-to-point and half-duplex multidrop PHY specification, capable of operating at 10 Mb/s. The 10BASE-T1S PHY is intended to be operated over the point-to-point link segment defined in 147.7 and the mixing segment defined in 147.8. The cabling supporting the operation of the 10BASE-T1S PHY is defined in terms of performance requirements between the attachment points (Medium Dependent Interface (MDI)), allowing implementers to provide their own cabling to operate the 10BASE-T1S PHY as long as the normative requirements included in this clause are met.

DME-based 10BASE-T1S is silent during idle symbols making it inherently energy efficient and without the need for a separate low-power-idle (LPI) mode, as is defined in Clause 78.

Optional support for PHY Level Collision Avoidance (PLCA) is described in 147.3.7 and Clause 148. PLCA provides improved performance in terms of effective throughput and maximum transmission latency when operating in half-duplex mode over a multi-drop mixing segment network.

147.1.1 Relationship of 10BASE-T1S to other standards

The relationship between the 10BASE-T1S, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model are shown in Figure 147–1. The PHY sublayers (shown shaded) in Figure 147–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 10BASE-T1S is defined in Clause 98. MII is defined in Clause 22. Auto negotiation is not defined for 10BASE-T1S PHY operating in half-duplex multidrop mode.

147.1.2 Operation of 10BASE-T1S

The 10BASE-T1S PHY may operate using full-duplex or half-duplex point-to-point communications on a link segment using a single balanced pair of conductors and supporting up to four in-line connectors and up to at least 15 meters with an effective rate of 10 Mb/s in each direction simultaneously.

Additionally, the 10BASE-T1S PHY may operate using half-duplex multidrop communications on a mixing segment using a single twisted-pair copper cable, interconnecting up to at least 8 PHYs, to a trunk up to at least 25 m. PHYs may be attached in-line with the trunk or at the end of stubs up to 10 cm. An overall effective rate of 10 Mb/s is shared among the nodes. Larger PHY count and reach may be achieved provided the mixing segment specifications in 147.8 are met.

In any operating mode the 10BASE-T1S PHY supports low cost applications requiring short physical reach, such as industrial, automotive and automation controls.

The 10BASE-T1S PHY utilizes two level Differential Manchester Encoding (DME) modulation. A 17-bit self-synchronizing scrambler is used to improve the EMC performance. 4B/5B encoding is used to further improve EMC performance and to perform out-of-band signaling among the connected PHYs. DME is a self-clocked and intrinsically balanced line coding which guarantees very low DC baseline wander and

- tx_cmd <= 'J' when a COMMIT request is asserted
- tx_cmd <= 'I' otherwise.

When PLCA capabilities are not supported or disabled, tx_cmd shall be set to the special 5B symbol ‘I’ (binary vector of 1,1,1,1,1) representing SILENCE.

tx_sym

5B symbol to transmit, generated from the MII data or directly passed from tx_cmd in SILENT state when optional PLCA reconciliation sublayer is implemented.

transmitting

This variable is set in the PCS Transmit state, as described in Figure 147–4.
When this variable is set to TRUE it indicates a transmission is ongoing.
Values: TRUE or FALSE

err

This variable is set in the PCS Transmit state, as described in Figure 147–4 and Figure 147–5.
This variable is used to detect and latch a pcs_txer = TRUE condition during data transmission; if such error is detected, an ESDERR symbol is sent at the end of transmission.
Values: TRUE or FALSE

link_control

This variable is generated by management or set by default. When set to FALSE all PCS functions are switched off and no data can be sent or received.
Values: TRUE or FALSE

txcnt

General purpose counter for PCS transmit function.

SYNC

5B symbol defined as ‘J’ in 4B/5B encoding.

SSD

5B symbol defined as ‘H’ in 4B/5B encoding.

ESD

5B symbol defined as ‘T’ in 4B/5B encoding.

ESDERR

5B symbol defined as ‘K’ in 4B/5B encoding.

ESDOK

5B symbol defined as ‘R’ in 4B/5B encoding.

SILENCE

5B symbol defined as ‘I’ in 4B/5B encoding.

147.3.2.3 Function

ENCODE

In the PCS transmit process, this function takes as its arguments four bits of input data, scrambles it as defined in 147.3.2.5 and returns the corresponding 5B symbol as defined in Table 147–1.

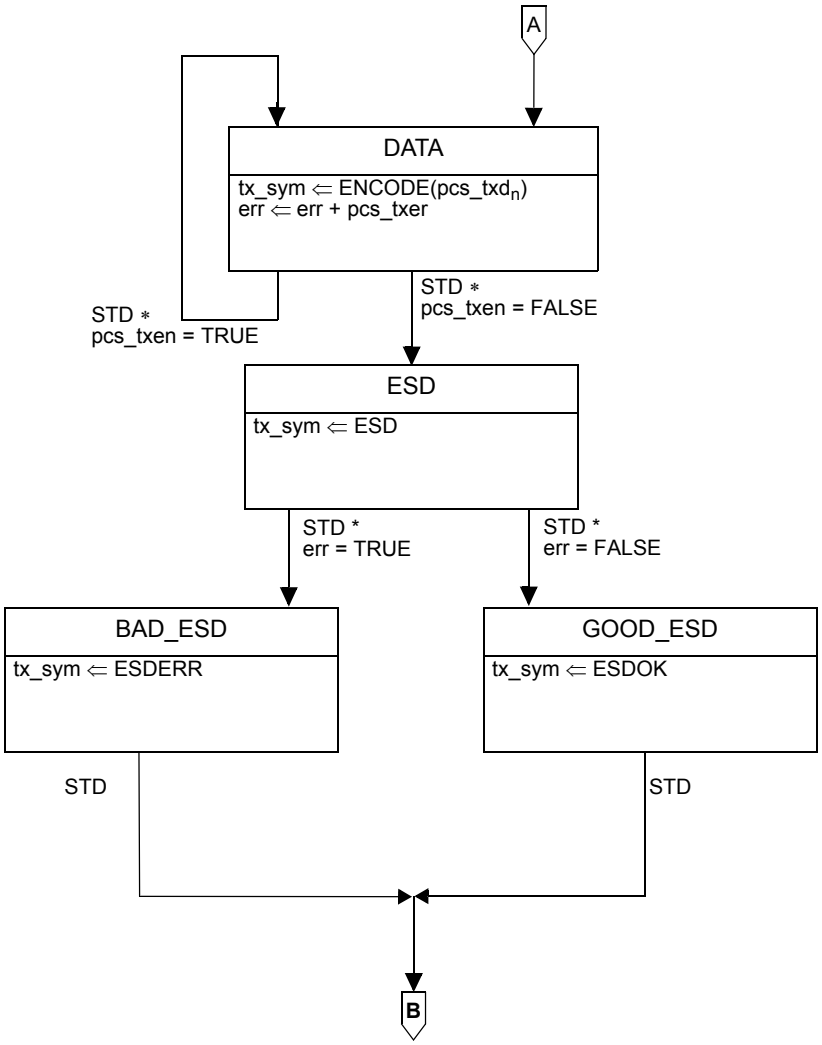

Figure 147–5—PCS Transmit state diagram (2 of 2)

147.3.2.4 Abbreviations

STD

Alias for 5B symbol timer done, synchronous to PCS TX clock.

147.3.2.5 Self-synchronizing scrambler

The PCS Transmit function shall implement multiplicative scrambling using the following generator polynomial: $g(x) = x^{17} + x^{14} + 1$.

need a colon here.

An implementation of self-synchronizing scrambler by linear-feedback shift register is shown in figure Figure 147–6. The bits stored in the shift register delay line at time n are denoted by $Scr_n[16:0]$. At every MII clock cycle, for each bit of TXD[3:0], the scrambler is advanced by one bit, and the output bit $Sd_n[i]$, represented by the exclusive-OR of $Scr_n[13]$, $Scr_n[16]$, and TXD[i], is shifted in as a new $Scr_n[0]$, with i ranging from 0 to 3 (i.e. LSB first). The scrambler is reset upon execution of the PCS Reset function. If the PCS

Reset is executed, all bits of the 17-bit vector representing the self-synchronizing scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeroes.

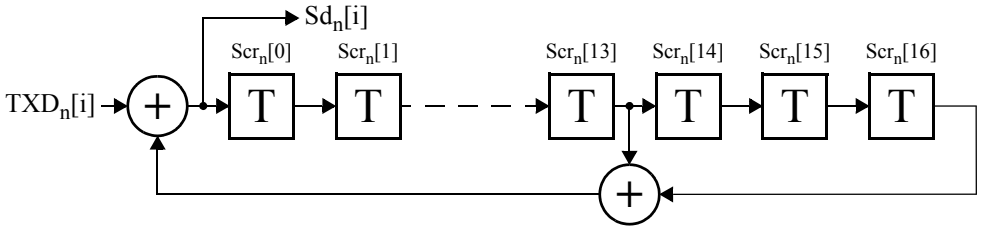

Figure 147–6—Self-synchronizing scrambler

147.3.3 PCS Receive

147.3.3.1 PCS Receive overview

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 147–8 and Figure 147–9, and associated state variables.

Note: A JAB state machine as the one defined for the 10BASE-T1L PHY in Clause 146 is not required for the 10BASE-T1S PHY because even in case of mis-detection of the ESD special symbol, the actual end of a transmission can still be detected by the PMA exploiting the absence of DME activity on the line. In fact, during idle period (i.e. when no data is being transmitted), the PMD is either driving a constant zero voltage level or put into high impedance state, depending on the operating mode (see 147.5.2).

The finite state machine defined in Figure 147–8 is triggered by the reception of a SYNC symbol from the PMA Receive function and waits for two SSD symbols to start regenerating the packet preamble whose start has been replaced with the SYNC, SYNC, SSD, SSD sequence by the PCS Transmit functions as described in Figure 147–4. After the second SSD is received, the PCS Receive function discards the next nine symbols which shall instead be used to achieve lock of the self-synchronizing descrambler.

During the descrambler locking time, the special value 5 is conveyed to the MII via the pcs_rxd variable in order to rebuild the original preamble transmitted by the MAC.

The DATA state, in which 5B symbols are decoded into MII data, is left when ESD followed by either ESDOK or ESDERR symbol is encountered or when the PMA detects SILENCE on the media (e.g. the transmitter prematurely stops data transmission).

The variables, functions, and timers used in Figure 147–8 are defined as below. For the definition of pcs_reset, SILENCE, SYNC, SSD, ESD, ESDOK and ESDERR see 147.3.2.2.

147.3.3.2 Variables

receiving

This variable is set in the PCS Receive state, as described in Figure 147–8 and Figure 147–9.
When it is set to TRUE it indicates that a data reception is ongoing.
Values: TRUE or FALSE

duplex_mode

This variable indicates whether the PHY is configured for full-duplex operation (DUPLEX_FULL) or half-duplex operation (DUPLEX_HALF). This variable is set after bit 8 in MDIO register 0 defined in Table 22-7.

precnt
: Counter for preamble regeneration.

pcs_rxdv
: The RX_DV signal of the MII as specified in 22.2.2.7.

pcs_rxer
: The RX_ER signal of the MII as specified 22.2.2.10.

pcs_rxd
: PCS decoded data synchronous to RX_CLK.

RXn
: Received 5b symbol generated by PMA receive at time n.

SILENCE
: The 5B symbol defined as 'I' in 4B/5B encoding.

147.3.3.3 Functions

DECODE
: In the PCS Receive process, this function takes as its arguments one 5B symbol, decodes the corresponding nibble as defined in Table 147–1, descrambles it as defined in 147.3.3.5 and returns the descrambled result as defined in 147.3.3.5. If a violation of the encoding rules is detected, PCS Receive asserts the signal RX_ER for at least one symbol period.

147.3.3.4 Abbreviations

RSCD — Alias for Receive Symbol Conversion Done, synchronous to PCS RX clock

147.3.3.5 Self-synchronizing descrambler

The PCS Receive function shall descramble the 5B/4B decoded data stream and return the proper nibble for generation of RXD[3:0] to the MII. The descrambler shall employ the polynomial $g(x)$ defined in 147.3.2.5. The implementation of the self-synchronizing descrambler by linear-feedback shift register is shown in Figure 147–7. The bits stored in the shift register delay line at time n are denoted by $Dcr_n[16:0]$. At every MII clock cycle, each bit of $Dr_n[3:0]$ is shifted in as new $Dcr_n[0]$ and the descrambler is advanced by one bit. The output bit RXD[i], represented by the exclusive OR of $Dcr_n[13]$, $Dcr_n[16]$ and $Dr_n[i]$, is generated, with i ranging from 0 to 3 (i.e. LSB first). The descrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all the bits of the 17-bit vector representing the self-synchronizing descrambler state are arbitrarily set. The initialization of the descrambler state is left to the implementer.

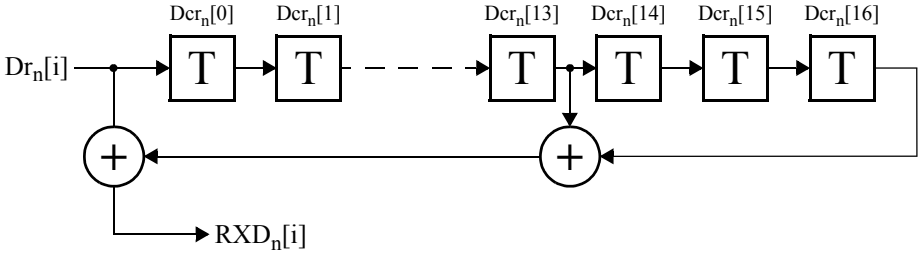

Figure 147–7—Self-synchronizing descrambler

147.3.4 PCS Loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to a one (or PCS loopback mode is enabled by a similar functionality if MDIO is not implemented). In this mode, the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium.

147.3.5 Collision detection

When operating in half-duplex mode, the 10BASE-T1S PHY shall detect physical collisions on the media during data transmission. When collisions are detected, the PHY shall assert the signal COL on the MII for the duration of the collision or until TX_EN signal is FALSE.

A collision can be detected by monitoring the rx_sym parameter conveyed through the PMA_UNITDATA.indication primitive for a SYNC, SSD symbol sequence and verify matching against the transmitted symbol sequence after the SSD symbol. A collision results in a mismatch in the symbol sequence.

147.3.6 Carrier sense

When operating in half-duplex mode, the 10BASE-T1S PHY shall sense when the media is busy and convey this information to the MAC, asserting the signal CRS on the MII as specified in 22.2.2.11.

CRS is generated by PCS Receive as the logical OR of the “transmitting” and “receiving” variables.

147.3.7 Optional support for PLCA Reconciliation Sublayer

When PLCA capabilities defined in Clause 148 are supported, the following applies.

147.3.7.1 Generation of BEACON indication

In compliance to 148.4.4.2.1, when PLCA RS operations are supported and enabled, the PHY shall notify the RS of a received BEACON indication by the means of MII interface as specified in 22.2.2.8.

When a sequence of at least two consecutive 'N' symbols is received, the MII signals RX_DV, RX_ER and RXD shall be set to the BEACON indication as shown in Table 22–2, overriding the current state. Override shall cease as soon as the currently received symbol is anything other than a 'N' code.

147.3.7.2 Generation of COMMIT indication

In compliance to 148.4.4.2.2, when PLCA RS operations are supported and enabled, the PHY shall notify the RS of a received COMMIT indication by the means of MII interface as specified in 22.2.2.8.

When a sequence of at least two consecutive 'J' symbols is received, the MII signals RX_DV, RX_ER, and RXD shall be set to the COMMIT indication as shown in Table 22–2, overriding the current state. Override shall cease as soon as the currently received symbol is anything other than a 'J' code.

147.3.7.3 Optional generation of early receive indication

In compliance to 148.4.4.2.4, when PLCA RS operations are supported and enabled, the PHY may notify the RS of an early receive indication by the means of MII interface as specified in 22.2.2.11 and 22.2.2.12.

The generation of the early receive indication is optional and left to the implementer as long as the requirements defined in the mentioned clauses are met.

147.4 Physical Medium Attachment (PMA) Sublayer

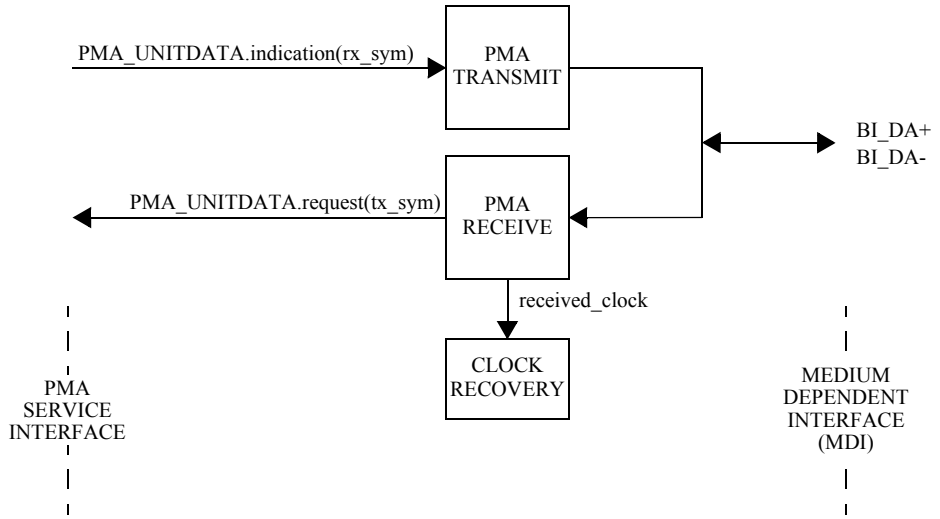

Figure 147–10—PMA functional block diagram

The reference diagrams do not explicitly show the PMA Reset function.

The PMA couples messages from the PMA service interface specified in 147.3.1 onto the 10BASE-T1S physical medium. The PMA provides both full duplex and half duplex communications to and from medium employing Differential Manchester Encoding. The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 147.9.

147.4.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see 36.2.5.1.3).

b) The receipt of a request for reset from the management entity.

147.4.2 PMA Transmit function

During transmission, PMA_UNITDATA.request conveys to the PMA using tx_sym the value of the symbols to be sent over the single transmit pair.

DME uses the presence or absence of transitions between these two voltage levels to encode data, thus the polarity is irrelevant.

The tx_sym variable is a vector of 5 bits to be encoded, LSB first, using Differential Manchester Encoding (DME) rules defined below:

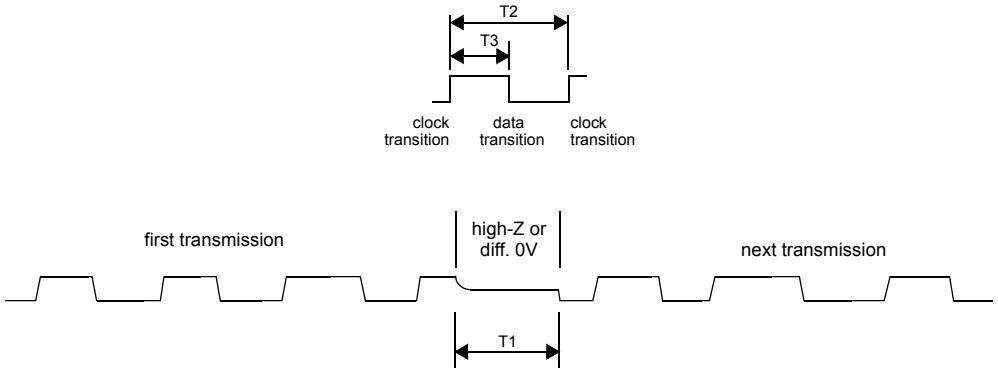

Figure 147–11—DME Encoding Scheme

Table 147–2—DME Timings

	Parameters	Min	Typ	Max	Units
T1	Delay between transmissions	200	—	—	ns
T2	Clock transition to clock transition	—	80	—	ns
T3	Clock transition to data transition (data = 1)	38	40	42	ns

The minimum and maximum values for parameter T2 are related to the transmit clock specification in 147.5.4.5.

If the tx_sym parameter value is the special 5B symbol 'I', the PMA shall, in order:

a) Transmit an additional DME encoded 0 if the previous value of the tx_sym parameter was anything but the 5B symbol 'I',

b) When operating in multidrop mode, put the PMD into high-impedance state.

c) When operating in point-to-point mode, have the PMD drive a differential voltage of 0 V (BI_DA+ = BI_DA-).

If tx_sym value is anything other than 'I' the following rules apply:

a) A "clock transition" shall always be generated at the start of each bit.

b) A "data transition" in the middle of a nominal bit period shall be generated if the bit to be transmitted is a logical '1'. Otherwise no transition shall be generated until next bit.

147.4.3 PMA Receive function

The 10BASE-T1S PMA Receive function comprises a single receiver (PMA Receive) for DME modulated signals on a single balanced pair, BI_DA. PMA Receive has the ability to translate the received signals on the single balanced pair into the PMA_UNITDATA.indication parameter rx_sym. It detects 5B symbols from the signals received at the MDI and presents these sequences to the PCS Receive function.

The PMA receive function shall recover encoded clock and data information from the DME encoded stream received at the MDI. In order to accomplish this task, the PMA Receive shall achieve proper synchronization on both the DME stream and the 5B boundary within 1.2 μs.

147.4.4 PMA Clock recovery

This PMA function recovers the clock from the received stream. PMA clock recovery outputs are used as input variables for other PMA functions.

147.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA for a 10BASE-T1S PHY.

147.5.1 EMC tests

Direct Power Injection (DPI) and 150 Ω emission tests for noise immunity and emission as per 147.5.1.1 and 147.5.1.2 may be used to establish a baseline for PHY EMC performance. These tests provide a high degree of repeatability and a good correlation to immunity and emission measurements. Additional tests may be needed to verify EMC performance in various configurations, applications, and conditions.

147.5.1.1 Immunity - DPI test

In a real application radio frequency (RF) common mode (CM) noise at the PHY is the result of electromagnetic interference coupling to the cabling system. Additional differential mode (DM) noise at the PHY is generated from the CM noise by mode conversion of all parts of the cabling system and the MDI. The sensitivity of the PMA's receiver to RF CM noise may be tested according to the DPI method of IEC 62132-4, and may need to comply with more stringent requirements as agreed upon between customer and supplier.

147.5.1.2 Emission - Conducted emission test

The emission of the PMA transmitter to its electrical environment may be tested according to the 150 Ω direct coupling method of IEC 61967-4, and may need to comply with more stringent requirements as agreed upon between customer and supplier.

147.5.2 Test modes

The test modes described in this subclause shall be provided to allow testing of the transmitter waveform, transmitter distortion, transmitter jitter, and transmitter droop. The test modes can be enabled by setting bits 1.2303.15:13 (10BASE-T1S PMA/PMD Test Control Register) of the PHY Management register set as described in 45.2.1.174c.1. If MDIO is not implemented a similar functionality shall be provided by another interface. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

a) Test mode 1 – Transmitter output voltage, timing jitter
b) Test mode 2 – Transmitter output droop test mode
c) Test mode 3 – Transmitter distortion test and PSD mask
d) Test mode 4 – Transmitter high impedance mode

When test mode 1 is enabled, the PHY shall repeatedly transmit DME encoded ones. See 147.5.4.5 for transmit clock requirements.

When test mode 2 is enabled, the PHY shall transmit a positive differential voltage for twenty nominal bit periods followed by a negative differential voltage for twenty nominal bit periods at 1 Vpp ± 30% amplitude. This sequence is repeated continually.

When test mode 3 is enabled, the PHY shall transmit continually a pseudo-random sequence of +1 and -1 symbols generated by PRBS7 with the generating polynomial of $x^7 + x^6 + 1$ encoded using Differential Manchester Encoding (DME) as in 147.4.2.

When the multidrop option is supported and test mode 4 is enabled, the transmitter presents a high impedance to the line as specified in 147.4.2 for the 'I' symbol in multidrop mode.

147.5.3 Test fixtures

The tolerance of the termination resistor shall be ± 0.1 %. All the transmitter tests are defined at the MDI.

To allow an easy synchronization of the measurement equipment, the PHY shall provide access to the symbol rate clock TX_TCLK, which times the transmitted symbols. For a MASTER PHY this is the output of the (divided) clock oscillator, for the SLAVE PHY this is the recovered clock.

147.5.4 Transmitter electrical specification

The PMA shall operate with AC coupling to the MDI. Where a load is not specified, the transmitter shall meet the requirements of this section with a 100 Ω ± 0.1 % resistive differential load connected to the transmitter output.

147.5.4.1 Transmitter output voltage

Transmitter output voltage shall be tested using test mode 1 in combination with the test fixture shown in Figure 147–12. The transmitter output voltage shall be 1 V ± 20 % peak-to-peak differential.

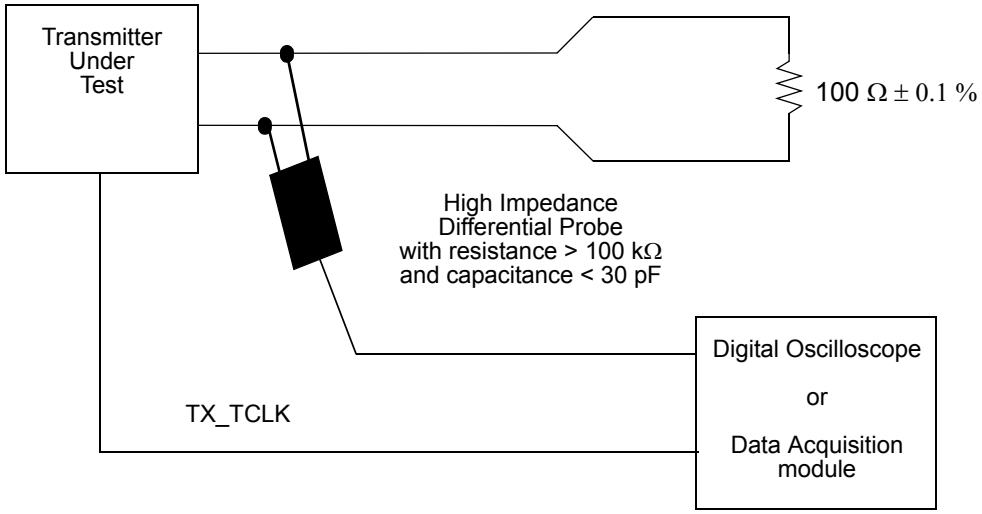

Figure 147–12—Test fixture

147.5.4.2 Transmitter output droop

Transmitter output droop shall be measured using test mode 2 and with the test fixture shown in Figure 147–12. The magnitude of both the positive and negative droop measured with respect to the initial peak value after the zero crossing and the value 800 ns after the initial peak, depicted by Figure 147–13, shall be less than 30 %.

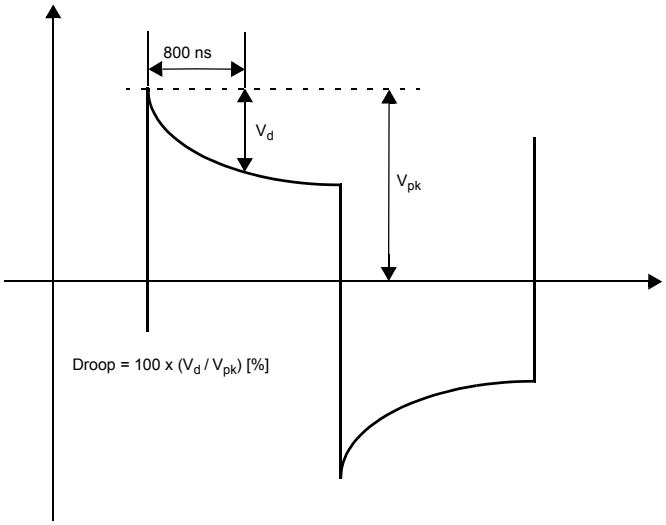

Figure 147–13—Transmitter output droop

147.5.4.4.3 PSD Mask

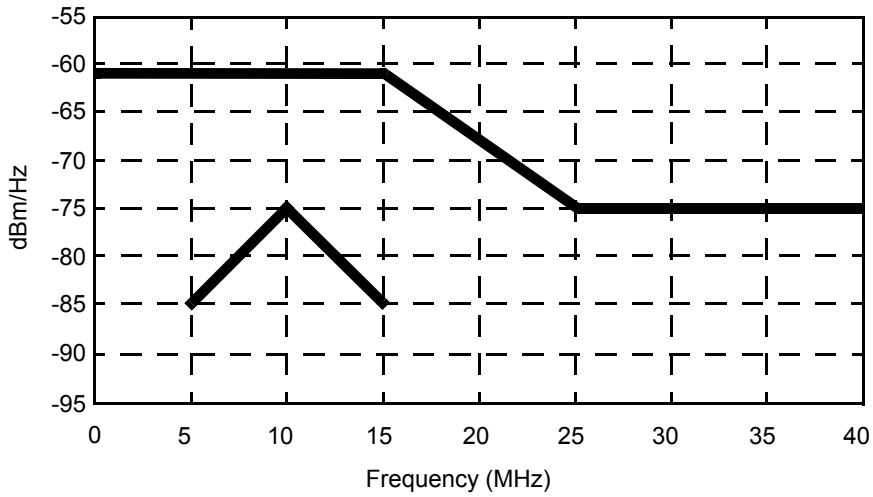

Figure 147–15—PSD upper and lower limits

147.5.4.5 Transmit clock frequency

The transmit clock frequency shall be 25 MHz with a tolerance of ± 100 ppm.

147.5.4.6 Alien crosstalk noise rejection

This specification is provided to verify the receiver's tolerance to alien crosstalk noise. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidth of 20 MHz and magnitude of -106 dBm/Hz. The receive DUT is connected to these noise sources through a resistive network, as shown in Figure 147–16, with link segments as defined in 147.7 and 147.8. The noise is added at the MDI of the DUT. The BER is expected to be less than 10^{-10} and to satisfy this specification the frame loss ratio is less than 10^{-7} for 125 octet packets measured at MAC/PLS service interface.

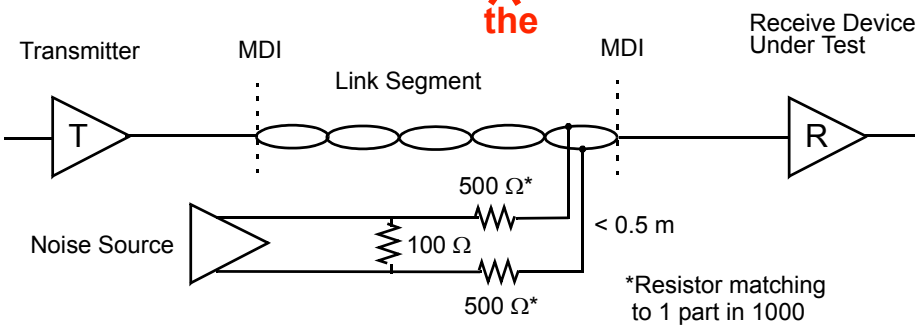

Figure 147–16—Alien crosstalk noise rejection test set-up

The PMA local loopback function is optional. If supported, the PMA shall be placed in local loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, or the PMA loopback bit in MDIO register 1.2299.13, defined in 45.2.1.174d.3, is set to a one (or PMA loopback mode is enabled by a similar functionality if MDIO is not implemented).

When the PHY is in the PMA local loopback mode, if the PHY supports full-duplex mode of operation, the PMA Receive function utilizes the echo signals from the unterminated MDI and decodes these signals to pass the data back to the MII Receive interface.

If the PHY supports half-duplex mode of operation, the PMA and PCS Receive functions shall pass to the MII RX the data decoded from the signal which is normally received during a transmission for the purpose of detecting collisions.

A MAC client can compare the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the 10BASE-T1S PCS and PMA functions.

147.5.4.7 Transmitter high impedance mode

In test mode 4, a transmitter supporting the multidrop mode presents a minimum of 10 kΩ impedance to the line from DC to 25 MHz.

147.6 Management interface

10BASE-T1S uses the management interface as specified in Clause 45. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

147.7 Point-to-point link segment characteristics

The transmission characteristics for the 10BASE-T1S point-to-point link segment are specified to support applications requiring short physical reach, such as industrial, automotive and automation controls, for up to at least 15 m.

147.7.1 Insertion loss

The insertion loss of each 10BASE-T1S point-to-point link segment shall meet the values determined using Equation (147–3).

$$\text{InsertionLoss}(f) < \begin{cases} 1.0 + \dfrac{1.6\,(f-1)}{9} & 0.3 \le f < 10 \\ 2.6 + \dfrac{2.3\,(f-10)}{23} & 10 \le f < 33 \\ 4.9 + \dfrac{2.3\,(f-33)}{33} & 33 \le f \le 40 \end{cases} \text{ dB} \qquad (147\text{–}3)$$

where

f is the frequency in MHz; $0.3 \le f \le 40$

147.7.2 Return loss

In order to limit the noise at the receiver due to impedance mismatches each 10BASE-T1S point-to-point link segment shall meet the values determined using Equation (147–4) at all frequencies from 0.1 MHz to 20 MHz. The reference impedance for the return loss specification is 100 Ω.

147.8.1 Return loss

The mixing segment shall meet the return loss characteristics specified for link segments in 147.7.2 at any MDI attachment point and with any combinations of up to at least seven other MDIs presenting minimum parallel load attached at any combination of permissible MDI attachment points.

147.8.2 Insertion loss

The mixing segment shall meet the insertion loss characteristics specified for link segments in 147.7.1 between any two MDI attachment and at the end of stubs of length up to 10 cm, and with any combinations of up to at least seven other MDIs presenting minimum parallel load attached at any combination of permissible MDI attachment points.

147.8.3 Mode conversion loss

The mixing segment shall meet the mode conversion loss characteristics specified for link segments in 147.7.3 at any MDI attachment points and with any combinations of up to at least seven other MDIs presenting minimum parallel load attached at any combination of permissible MDI attachment points.

147.9 MDI specification

147.9.1 MDI connectors

The mechanical interface to the balanced cabling is a 3-pin connector (BI_DA+, BI_DA-, and optional SHIELD) or alternatively a 2-pin connector with an optional additional mechanical shield connection which conforms to the link segment specification defined in 147.7 or to the mixing segment specification defined in 147.8.

147.9.2 MDI electrical specification

The MDI shall present a minimum parallel impedance across the MDI attachment points based on impedance Equation (147–6) and limits for R, L, C_{tot} and C_{node} over the stated frequency range, where C_{tot} is the maximum total capacitance across all attachment points, while C_{node} is the maximum capacitance for each attachment point.

$$|Z| = \frac{1}{\sqrt{\frac{1}{R^2} + \left(\frac{1}{2\pi \cdot f \cdot L} - 2\pi \cdot f \cdot C_{node}\right)^2}} \qquad (147\text{–}6)$$

where

f is the frequency in MHz; $0.3 \le f \le 40$.

147.9.3 MDI fault tolerance

The wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential or positive voltages of up to 60 V dc with the source current limited to 1200 mA, as per Table 147–4, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is/are removed.

148. PLCA Reconciliation Sublayer (RS)

148.1 Introduction

This clause specifies the optional PHY Level Collision Avoidance (PLCA) capabilities. PLCA provides improved performance over standard CSMA/CD method in terms of throughput and latency for small multi-drop networks having a limited number of nodes and high utilization.

PLCA is defined for half-duplex mode of operation only. MII (Clause 22) specifications are compatible with the gRS sublayer defined in 148.4.2. The PLCA sublayer is specified for operation with the PHY defined in Clause 147 (10BASE-T1S).

PLCA is designed to work on top of CSMA/CD and can be dynamically enabled or disabled via management interface. When disabled, the system operates as specified in Clause 22.

148.2 Overview

The working principle of PLCA is that each PHY on a multidrop network is granted, in turn, a single transmit opportunity based on its assigned unique node ID.

At any time, only the PHY owning a transmit opportunity is allowed to send data over the medium, therefore avoiding physical collisions.

Transmit opportunities are generated in a round-robin fashion every time the PHY with node ID = 0 signals a BEACON on the medium, indicating the start of a new cycle. This can only happen after each PHY has been given exactly one transmit opportunity, thus ensuring media access fairness.

PLCA relies on CSMA/CD functions to have the MAC delay a transmission until a transmit opportunity is met.

148.3 Relationship with other IEEE standards

The relationship between the PLCA generic Reconciliation Sublayer, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model is shown in Figure 148–1. The reconciliation sublayer (shown shaded) in Figure 148–1 connects one Clause 4 Media Access Control (MAC) layer to the PHY. Ethernet support for time synchronization protocols is defined in Clause 90. MII is defined in Clause 22.

When PLCA functions are not supported or are disabled by the management interface (plca_en = OFF), RS operation shall conform to the MII RS definition in Clause 22.

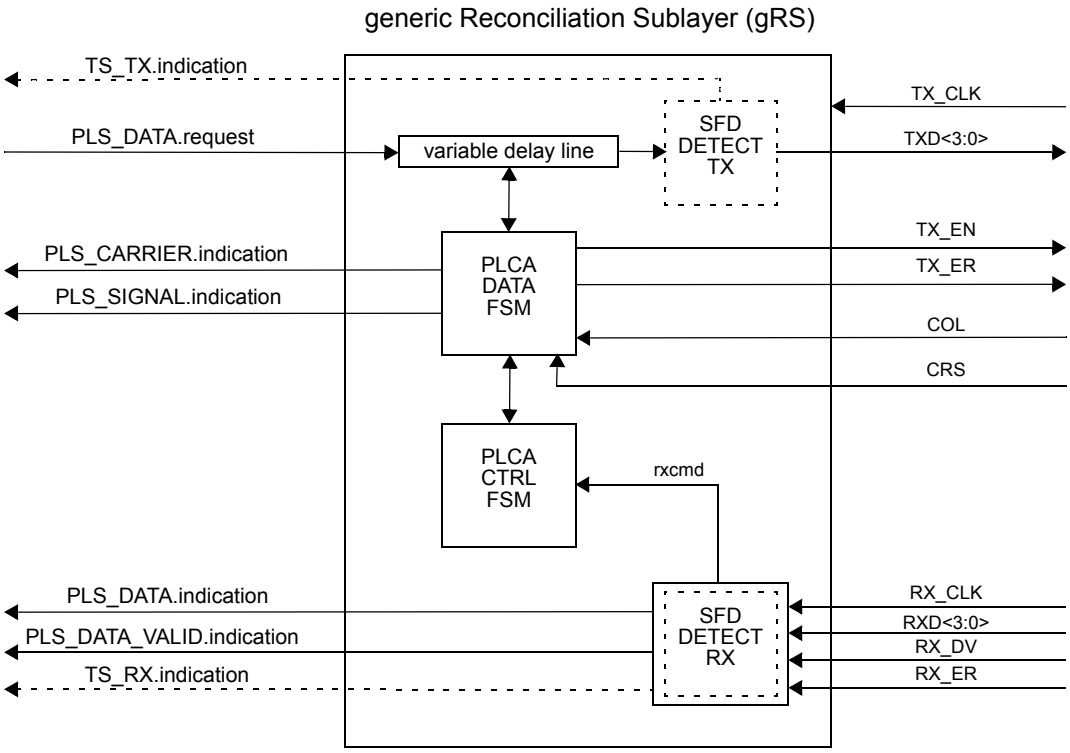

Figure 148–3—PLCA functions within the generic Reconciliation Sublayer (gRS)

148.4.2.1 Operation with TSSI

When TSSI support is also specified in the actual RS, the SFD detection of transmitted frames shall be detected after the PLCA variable delay line, as shown in Figure 148–3. This ensures the network latency measurement is not affected by the synchronization latency added by PLCA. No special attention is required for SFD detection of received frames.

148.4.3 Mapping of MII signals to PLS service primitives and PLCA functions

The RS maps the signals provided at the MII to the PLS service primitives defined in Clause 6 via the PLCA state machines, variables and functions (see 148.4.5 and 148.4.6). The PLS service primitives provided by the RS behave in exactly the same manner as defined in Clause 6.

148.4.3.1 Mapping of PLS_DATA.request

When PLCA is disabled (plca_en = OFF), the mapping of the PLS_DATA.request primitive shall be the one specified in 22.2.1.1. Otherwise, the following applies.

148.4.3.1.1 Function

Maps the primitive PLS_DATA.request to PLCA state machines variables which in turn generate the MII signals TXD<3:0>, TX_EN and TX_CLK.

148.4.3.1.2 Semantic of the service primitive

PLS_DATA.request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. It represents a single data bit. The values ONE and ZERO are conveyed by the PLCA variables plca_txd<3>, plca_txd<2>, plca_txd<1> and plca_txd<0>, each of which conveys one bit of data while plca_txen is set to TRUE. The value DATA_COMPLETE is conveyed by setting the variable plca_txen to FALSE. MII signals TXD<3:0> and TX_EN are generated by way of the PLCA DATA State Machine specified in 148.4.6. Synchronization between the RS and the PHY is achieved by way of the TX_CLK signal.

148.4.3.1.3 When generated

The plca_txd<3:0> and plca_txen variables are assigned after every group of four PLS_DATA.request transactions from the MAC sublayer to request the PLCA functions to transmit a nibble of data when PHY transmit opportunity is met, or to signal the end of the transmission. The TX_CLK signal is generated by the PHY. The TXD<3:0> and TX_EN signals are generated by the RS according to PLCA DATA State Machine (see 148.4.6).

148.4.3.2 Mapping of PLS_DATA.indication

Map of the primitive PLS_DATA.indication shall comply with 22.2.1.2.

148.4.3.3 Mapping of PLS_CARRIER.indication

When PLCA is disabled (plca_en = OFF) the mapping of the PLS_CARRIER.indication primitive shall be the one specified in 22.2.1.3. Otherwise, the following applies

148.4.3.3.1 Function

Maps the primitive PLS_CARRIER.indication to the PLCA DATA State Machine.

148.4.3.3.2 Semantic of the service primitive

PLS_CARRIER.indication (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. For EEE capability, CARRIER_STATUS is overridden as specified in 22.2.1.3.3.

148.4.3.3.3 When generated

The PLS_CARRIER.indication service primitive is generated by the RS according to the PLCA DATA State Machine specified in 148.4.6.

148.4.3.4 Mapping of PLS_SIGNAL.indication

When PLCA is disabled (plca_en = OFF) the mapping of the PLS_SIGNAL.indication primitive shall be the one specified in clause 22.2.1.4. Otherwise, the following applies.

148.4.3.4.1 Function

Map the primitive PLS_SIGNAL.indication to the PLCA DATA State Machine.

PHY specifications are free to map the COMMIT request to any suitable line coding as long as the requirement defined herein are met.

148.4.4.1.3 Early receive indication (optional)

In order to minimize TO_TIMER skew across the multidrop network and improve PLCA performance, a PHY may optionally notify the RS of an early receive condition. Early receive indication is conveyed to the RS by the means of MII interface as specified in 22.2.2.8.

If supported, this notification shall occur before CRS is asserted, as soon as the PHY detects anything on the medium that might be a BEACON, COMMIT or normal data.

Notification shall terminate when either a valid BEACON, COMMIT or normal data is being received or if the condition that triggered the notifications ceases.

148.4.4.2 Mapping of MII signals to PLCA variables

The PLCA RS is required to decode PLCA specific signaling out of MII interface.

148.4.4.2.1 BEACON indication

When the PHY receives a BEACON, it shall indicate this information to the RS by asserting MII signals.

The RS shall react to such indication by setting the PLCA variable rx_cmd to the value BEACON. The RS shall also reset the rx_cmd variable to NONE when the BEACON indication on the MII ceases, unless a COMMIT indication is signaled in which case rx_cmd shall be set as specified in 148.4.4.2.2.

148.4.4.2.2 COMMIT indication

When the PHY receives a COMMIT from the line, it shall indicate this information to the RS by asserting MII signals.

The RS shall react to such indication by setting the PLCA variable rx_cmd to the value COMMIT. The RS shall also reset the rx_cmd variable to NONE when the COMMIT indication on the MII ceases, unless a BEACON indication is signaled in which case rx_cmd shall be set as specified in 148.4.4.2.1.

148.4.4.2.3 CARRIER indication

Since the PHY may optionally provide early receive indication by the means of CRS and COL MII signals, the plca_crs variable shall be set accordingly as follows:

$$plca\_crs \Leftarrow \begin{cases} \text{TRUE} & \text{if TX\_EN = TRUE or RX\_DV = TRUE} \\ \text{FALSE} & \text{else if COL= TRUE} \\ \text{CRS} & \text{else} \end{cases} \quad (148\text{–}1)$$

148.4.4.2.4 Early receive indication

The MII signal CRS shall map to the plca_eri variable directly, as shown in Equation (148–2), despite the PHY supporting the early receive indication feature or not.

$$plca\_eri \Leftarrow \text{CRS} \quad (148\text{–}2)$$

148.4.5 PLCA Control

148.4.5.1 PLCA Control State Diagram

PLCA Control state machine is responsible for synchronizing transmit opportunities across the multidrop network to avoid physical collisions.

The PLCA Control function shall conform to the PLCA Control state diagram in Figure 148–4 and Figure 148–5 and associated state variables, functions, timers and messages.

When PLCA functions are disabled (plca_en = OFF), the PLCA control variables are reset to their default values and no special signaling is conveyed to the MII through the tx_cmd variable.

When PLCA functions are enabled, the PHY with local_nodeID variable set to 0, immediately switches to RECOVER state and waits for all other PHYs to be silent for at least RECV_BEACON_TIMER. Then it switches to SEND_BEACON state to have all other PHYs synchronize their own transmit opportunity counter and related timer. PHYs with nonzero local_nodeID wait in RESYNC state until a BEACON is received.

All PHYs detect the end of the BEACON condition before resetting the transmit opportunity timer, in order to minimize latency differences across the network.

After syncing is done, all PHYs have their own transmit opportunity counters (curID) reset and the TO_TIMER started. At this point, the TO_TIMER maximum skew across all PHYs is $\Delta RX_{lat} + T_{PD}$, where ΔRX_{lat} is the worst case receive latency difference among all the PHYs, while T_{PD} is the worst-case propagation delay time from end-to-end on the mixing segment.

In WAIT_TO state, the PHY waits for one of these possible conditions:

1) An early receive indication (plca_eri = TRUE) is signaled by the PHY through MII (see 148.4.4.1.3).
2) The PHY asserts the CRS signal (plca_eri = TRUE), indicating a data reception is about to occur.
3) Transmit opportunity counter "curID" is equal to "local_nodeID"
4) TO_TIMER elapses indicating the current transmit opportunity is yielded

Condition (1) may only occur if the PHY supports the optional early receive indication as specified in 22.2.2.11 and 22.2.2.12. When this happens, it's very likely that a BEACON or a valid packet (see 1.4.312) is about to be received. However, it's also possible for the PHY to indicate a false early receive condition due to glitches and other unlikely external events. To handle such case, an optimistic scheme is used: PLCA control state machine assumes the early receive indication of the PHY to be reliable and switches to EARLY_RECEIVE state arming the RECV_TIMER and stopping the TO_TIMER (i.e. assuming BEACON or valid data to be received shortly).

At this point, if the plca_crs variable is set to TRUE, the control state machine goes to RECEIVE state for actually receiving the packet. If a BEACON is detected instead, it switches to RESYNC state. In case the RECV_TIMER expires, a recovery procedure is initiated to resynchronize the (possibly) misaligned TO_TIMER and curID counter.

The recovery procedure forces the PHY with local_nodeID=0 to wait for all other PHYs to be silent for at least RECV_BEACON_TIMER before sending a new BEACON, and all other PHYs to wait for the next BEACON to be received.

When condition (2) occurs, the state machine immediately switches to RECEIVE state, stopping the TO_TIMER. This is the usual case when the early receive indication is not supported by the PHY and a packet is being received.

When condition (3) occurs, PLCA Control samples the packetPending variable to detect whether the MAC is ready to send out a packet. If not, the transmit opportunity is yielded by waiting for the TO_TIMER to expire. Otherwise, the transmit opportunity is committed by having the PHY issue a COMMIT request and have other PHYs stop their own TO_TIMER. This is achieved by the means of special MII signaling as specified in Table 22-1 (PLCA COMMIT request).

When condition (4) is met, another PHY has yielded its transmit opportunity, causing the transmit opportunity counter to be incremented and TO_TIMER to be reset.

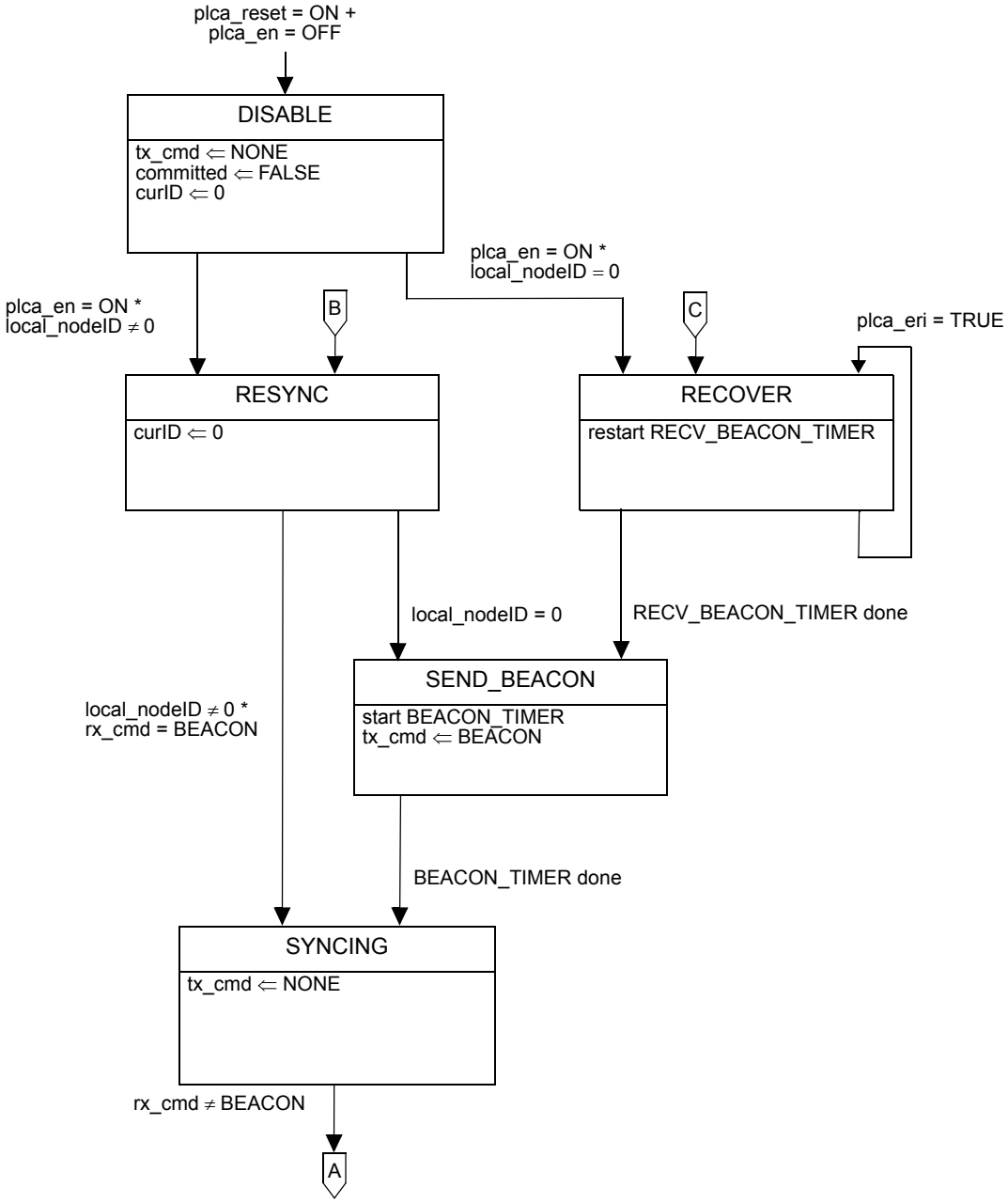

Figure 148–4—PLCA Control state diagram (1 of 2)

The PLCA Data function shall conform to the PLCA Data state diagram in Figure 148–6 and Figure 148–7 and associated state variables, functions, timers and messages.

When PLCA functions are enabled, the PLCA Data state machine waits for the MAC to start a transmission or the PHY to signal either an early receive indication or a carrier sense.

In the former case, the data conveyed by the MAC through the PLS_DATA.request primitive is delayed by switching to HOLD state. In the latter case, CARRIER_ON is signaled through the PLS_CARRIER.indication to have the MAC defer any new transmission, then the RECEIVE state is entered.

The MAC however, might have started a transmission right before a carrier is detected, which would normally result in a physical collision. In this case the Data state machine switches to the COLLIDE state asserting SIGNAL_STATUS = SIGNAL_ERROR via PLS_SIGNAL.indication primitive to have the MAC perform a backoff and send the packet again later, without actually forwarding any data for the PHY to transmit on the medium. This is called a logical collision.

During the HOLD state the PLCA Control state machine is notified via the packetPending variable that data is available to be transmitted and the beginning of the transmission is held in the variable delay line. At next transmit opportunity the PLCA Control state machine allows transmitting the delayed data by setting the "committed" variable to TRUE. In such case the PLCA Data state machine switches to TRANSMIT state to ~~actually~~ deliver the data for the PHY to encode and transmit on the medium.

The variable delay line is a small buffer that is necessary in order to avoid physical collisions by delaying transmission to the MII interface until the exclusive transmit opportunity for the node arrives. The variable delay line length is no greater than TO_TIMER * MAX_ID + BEACON_TIMER.

If TX_ER is asserted during the HOLD state, the PLCA Data state machine switches to ABORT state to assert packetPending = FALSE and to wait until the MAC stops sending data. The aborted packet will not be transmitted on the medium.

If another PHY starts a transmission after meeting its own transmit opportunity, delayed data cannot be held anymore and a logical collision is triggered by switching to COLLIDE state.

During the COLLIDE state, the PLCA Data state machine asserts packetPending = FALSE and CARRIER_STATUS = CARRIER_ON via the PLS_CARRIER.indication primitive. When the MAC is done sending the jam bits as described in Clause 4, it waits for the next transmit opportunity by switching to PENDING state.

During the PENDING state, the PLCA Data state machine asserts packetPending = TRUE and keeps CARRIER_STATUS = CARRIER_ON via the PLS_CARRIER.indication primitive to prevent the MAC to make new transmit attempts until PLCA Control state machine signals that a new transmit opportunity is met. At that point CARRIER_STATUS is set to CARRIER_OFF to have the MAC ~~actually~~ resend data after waiting one IPG period as described in Clause 4.

Annex 146A

(informative)

Intrinsically safe applications

146A.1 Guidelines for implementation of the 10BASE-T1L PHY in an intrinsically safe application

The principle of intrinsic safety is based on the limitation of voltage, current, power, capacitance, and inductance of electrical circuits. Within hazardous locations a circuit following the limits of the intrinsic safety standards will not be able to ignite gas or dust atmospheres in case of a short circuit or any other kind of failure.

Defining the limits of intrinsic safety is not the intention of this communication standard. Nevertheless, the specification of 10BASE-T1L in Clause 146 is intended to be compatible with implementation of intrinsically safe systems.

In addition, the realization of the PHY IC has a strong impact on the possible intrinsic safety concepts, while using external and discrete components for intrinsic safety related aspects simplifies the certification process. The following implementation choices can simplify the process for certifying 10BASE-T1L PHYs in intrinsically safe systems:

External termination resistors: These can be used to limit the energy and current to or from the intrinsically safe link segment;

Providing separate high impedance receive pins: External resistors for current and energy limitation can also be added to the receive path.

Figure 146A–1 and Figure 146A–2 show in principle two possible implementations on how to feed power onto an intrinsically safe link segment. The circuits should only be seen as examples. It is in the responsibility of the hardware designer to fulfill all relevant standards (especially IEC 60079-0 and 60079-11, but also others), when implementing devices for the use within intrinsically safe applications.

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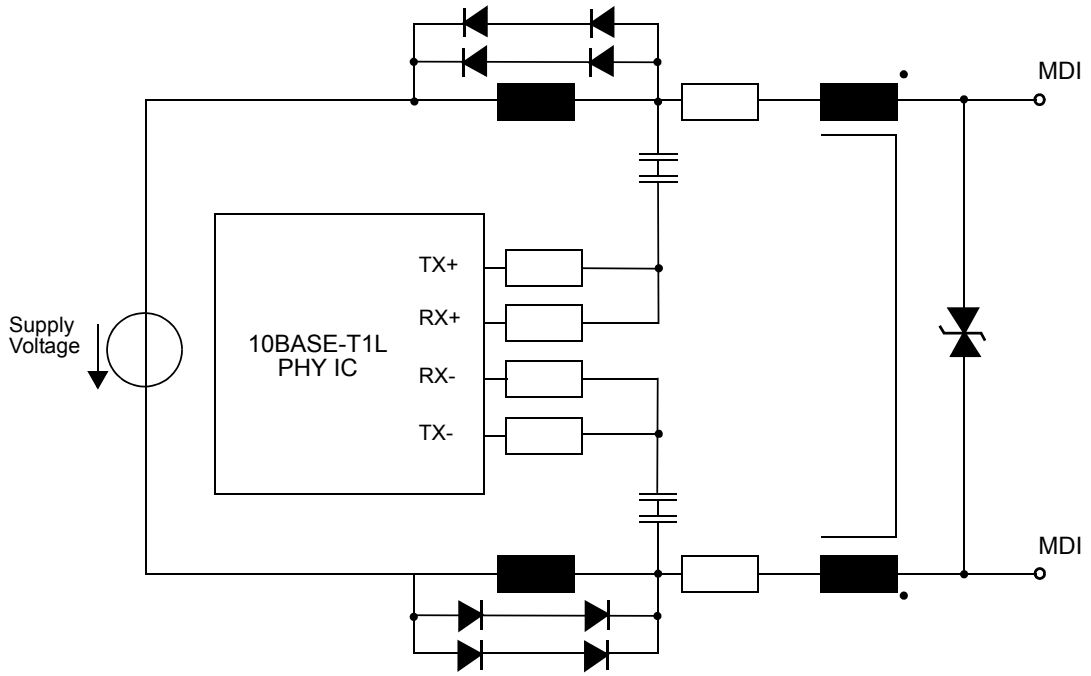

Figure 146A–1—First possible implementation on intrinsically safe power feeding side

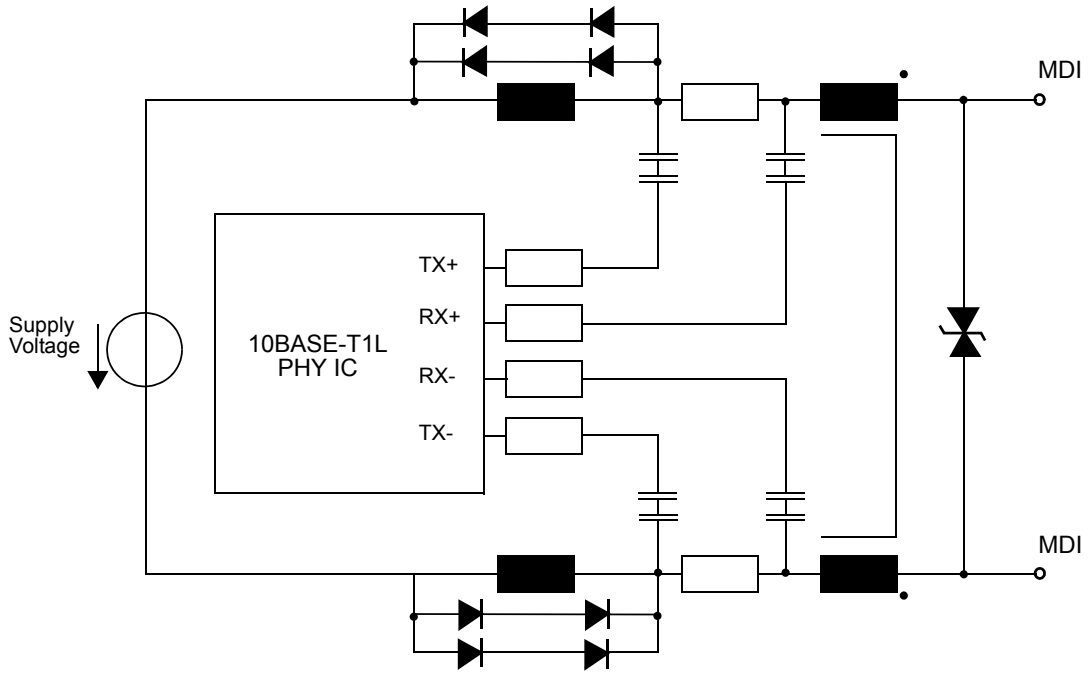

Figure 146A–2—Second possible implementation on intrinsically safe power feeding

Note: Likely the second version is easier to implement within a PHY IC as the hybrid within the PHY IC needs not to be adopted to different external resistor values.

Figure 146A–3 shows in principle a possible implementation on how to decouple the power from an intrinsically safe link segment. The circuit should only be seen as example. It is in the responsibility of the hardware

Annex 146B

(informative)

Optional power distribution

146B.1 Overview

Annex 146B provides information on the optional powering topologies. The class power requirements are specified in Clause 104.

146B.1.1 Point-to-point powering topologies

The point-to-point powering topology is defined to enable characterization of the DCR. The point-to-point powering topology is illustrated in Figure 146B–1.

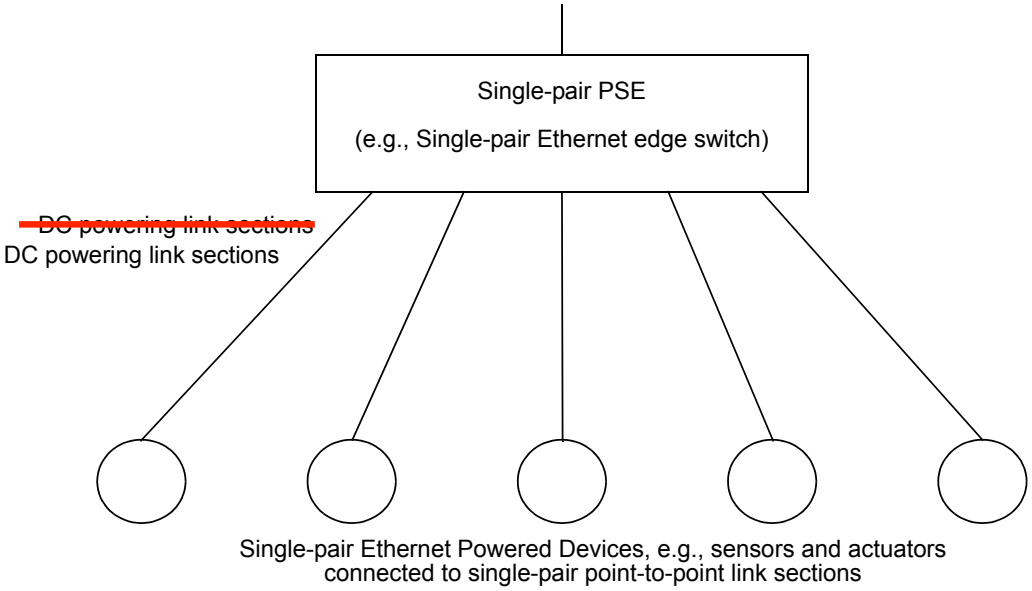

Figure 146B–1—Point-to-point powering topology

146B.1.1.1 Point-to-point link segment DCR characteristics

The point-to-point link segment DCR characteristics are given in Table 146B–1.