10 Mb/s Single Twisted Pair Ethernet
10BASE-T1L PHY Control State Diagram
Version 2 (Comment #584)

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10BASE-T1L PHY Control State Diagram

- Depending on the implementation the PHY Control state machine in D2.0, can run into synchronization issues, if FORCE mode is active. See presentation:

  http://www.ieee802.org/3/cg/public/adhoc/fitzgerald_0815_10baset1l_phy_control_synch.pdf

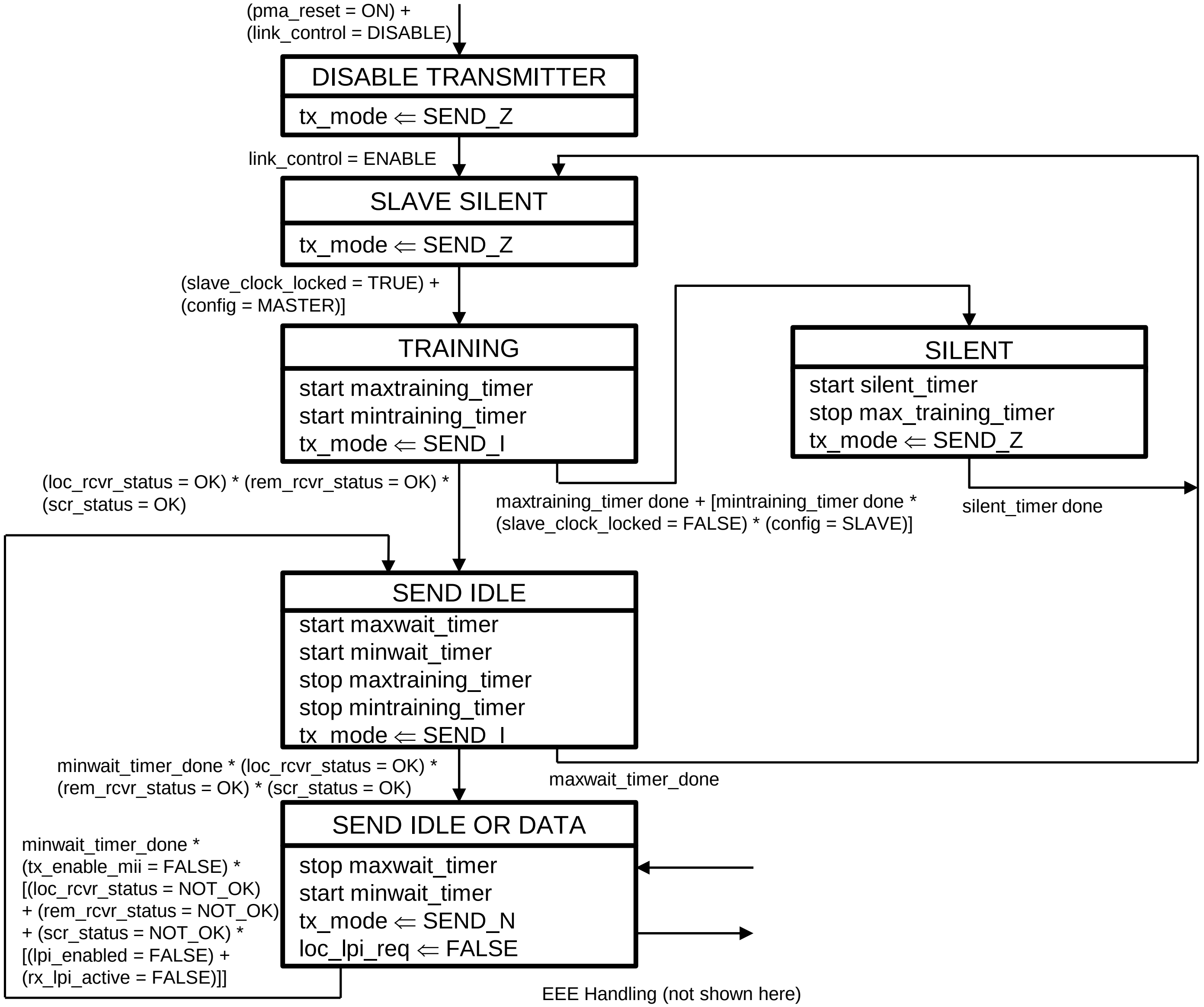
- Main reason for these issues is that both, Master and Slave PHY provide a “training_timer”, which limits the maximum time, a PHY may stay in training and if both timers are not synchronized, then it can happen, that for one PHY only a part of the training time remains, so that this PHY cannot finalize the training and therefore has to start training again.

- This condition may, depending on the implementation, persist for a longer time.

- To solve this issue, some changes in the PHY Control state machine are suggested.

- **The race condition between the training timers in the master and the slave PHY is solved by not only keeping the slave PHY in SILENT state, until the slave clock is acquired, but also the master PHY, thus allowing the slave PHY to synchronize on the master PHY training.**

10BASE-T1L PHY Control State Diagram



10BASE-T1L PHY Control State Diagram

Needed changes to other sections of the draft:

Rename „training_timer“ to „maxtraining_timer“.

Add the following timers to the timer section:

mintraining_timer:	A timer used to set the minimum time a slave PHY stays in training mode before going to SILENT state in case a loss of clock lock is detected. The timer shall expire 100 ms ± 1 ms after being started.
silent_timer:	A timer used to set the time a PHY stays in SILENT state. The timer shall expire 100 ms ± 1 ms after being started.

Add the following variable to the variables section:

slave_clock_locked:	This variable is set TRUE, if the clock recovery circuit on the slave PHY detects a stable clock, locked on the master PHY clock. Implementations may benefit from checking scr_status for deciding, if the slave clock is locked. If there is no signal received from the master PHY or the slave clock is unstable, this variable has to be set back to FALSE. Values: TRUE or FALSE

Thank You