10 Mb/s Single Twisted Pair Ethernet

10BASE-T1L PHY Control State Diagram (Comment #584)

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10BASE-T1L PHY Control State Diagram

- Depending on the implementation the PHY Control state machine in D2.0, can run into synchronization issues, if FORCE mode is active. See presentation:

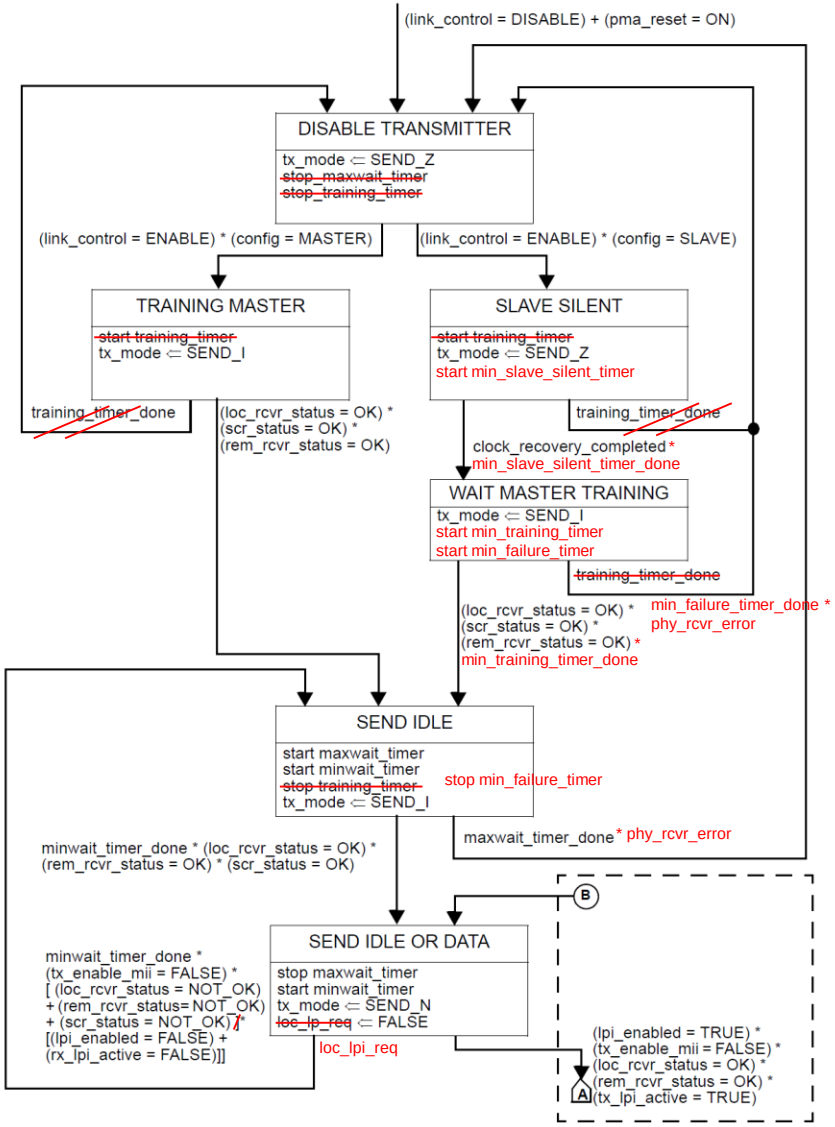
  http://www.ieee802.org/3/cg/public/adhoc/fitzgerald_0815_10baset1l_phy_control_synch.pdf

- Main reason for these issues is that both, Master and Slave PHY provide a “training_timer”, which limits the maximum time, a PHY may stay in training and if both timers are not synchronized, then it can happen, that for one PHY only a part of the training time remains, so that this PHY cannot finalize the training and therefore has to start training again.

- This condition may, depending on the implementation, persist for a longer time.

- To solve this issue, some changes in the PHY Control state machine are suggested.

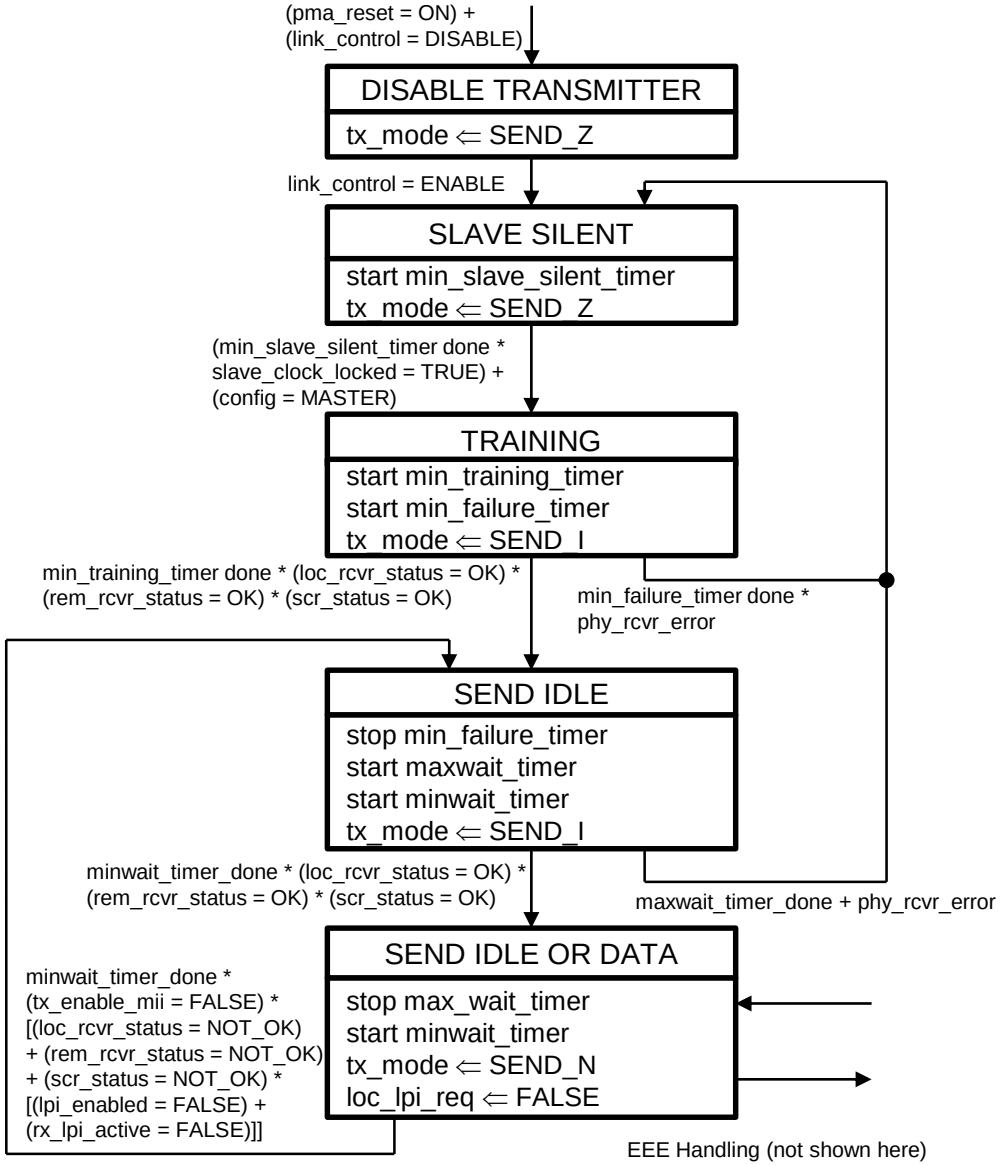
10BASE-T1L PHY Control State Diagram



This state machine can now be simplified by combining the Master and Slave training states (see next page).

Changes (in red) to:
Figure 146-14 – PHY Control state diagram (part a)

10BASE-T1L PHY Control State Diagram



Implementing these changes, the PHY Control state diagram can be simplified by using the same „TRAINING“ state for Master and Slave PHY.

Timers (need to be added to the timer section):

min_slave_silent_timer:
Minimum time (10 ms ± 1 ms) the slave PHY stays in silent mode.

min_training_timer:
Minimum time (10 ms ± 1 ms) the PHY stays in training mode.

min_failure_timer:
Minimum time (50 ms ± 1 ms) the slave PHY stays in training mode before going back to „SLAVE SILENT“ state, if the slave PHYs clock is not locked anymore or another unrecoverable error is detected.

10BASE-T1L PHY Control State Diagram

- The 10 ms timer values for min_slave_silent_timer and min_training_timer can be used for the Master PHY to synchronize on the current slave training state.
- The min_failure_timer allows, that e.g. after enabling of the local transmitter, the Slave PHY clock may be unstable for up to 50 ms (after enabling the Slave PHYs transmitter), until the echo canceller is trained; the Master PHY needs to be aware, that during this time the transmit signal of the Slave PHY may have a higher clock jitter (and e.g. waits with its own training for at least 50 ms after the Slave PHY starts to transmit).
- slave_clock_locked (needs to be added to the variables section):
  This variable is set TRUE, if the clock recovery circuit on the slave PHY detects a stable clock, locked on the Master PHY clock. Implementations may benefit from checking scr_status for deciding, if the slave clock is locked.
  Values: TRUE or FALSE
- phy_rcvr_error (needs to be added to the variables section):
  This variable is set TRUE, if the receiver of the PHY detects an unrecoverable error, which requires a restart of the training (triggering of phy_rcvr_error is implementation specific).
  Values: TRUE or FALSE

10BASE-T1L PHY Control State Diagram

- The suggested changes provide the following improvements:
  - Preventing of possible race conditions during Master and Slave PHY training by removing the training timeout.
  - Added 10 ms timers for SLAVE SILENT and TRAINING states allow synchronization of the Master PHY on the Slave PHY training state.
  - Simplification of the state diagram by having the same „TRAINING“ state for Master and Slave PHY.
  - No training timeout needed anymore, only supervisory of the training for unrecoverable errors, e.g. loss of clock synchronization of the slave PHY.
  - Added a fast path from SEND IDLE state back to SLAVE SILENT STATE, if an unrecoverable error is detected by the receiver.
  - For recoverable errors, the PHY still stays in SEND IDLE state until the maxwait_timer elapsed, trying to get the link back to normal operation.

Thank You