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Optional Cable Resistance Measurement

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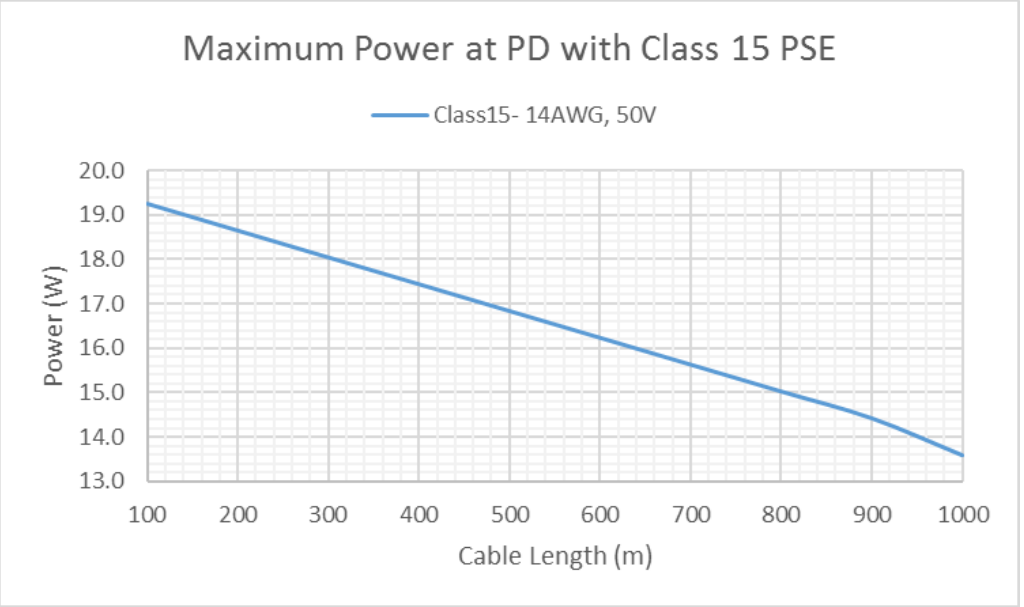
Presentation Outline

- Motivation- Reclaim Power Lost in Cable
- Leveraging existing SCCP protocol for resistance measurement
- Measurement- Overview
- PD and PSE Power Budgeting Calculations
- Optional Implementation
- SCCP flowchart
- Optional SCCP Registers
- SCCP Electrical Requirements
- Baseline Text for 104.7

Motivation- Reclaim Power Lost in Cable

- Systems with shorter cables are penalized
- For Example: Class 15 systems (14AWG, $V_{PSE\text{-}min}$ = 50V)
  - $P_{CLASS(min)}$ = 19.4W – This is the minimum power every Class 5 PSE is capable of supplying
  - $P_{PD(max)}$ = 13.6W – This is the maximum power any Class 5 PD is allowed to draw
  - This is with an assumption that 5.87W of power is always lost in the cable
  - 5.87W is calculated as $I_{PI-max}{}^2 \times R_{loop(CLASS-max)} = 0.388A^2 \times 39ohms$
  - For systems with shorter links, for instance a 100meter link with about 3ohms loop resistance,
    - Power lost in the cable is less than 0.5W
  - With no change in PSE, the PD can now draw almost 19W a 40% increased power



Specified by AWG and Length								
			1000m			300m		
AWG	Class	Vpse, min	Ipi, max	Rloop, max (60C)	Ppd 1000m	Ipi, max	Rloop, max (60C)	Ppd 300m
18AWG	1	20	102	59	1.4	326	18	4.6
14AWG	2	20	155	39	2.2	488	12	6.8
24AWG	3	20	52	116	0.7	169	36	2.4
18AWG	4	50	254	59	8.9	815	18	28.5
14AWG	5	50	388	39	13.6	1221	12	42.7
24AWG	6	50	129	116	4.5	400	36	14.0

Reference: http://www.ieee802.org/3/cg/public/May2018/stewart_3g_01f_0518.pdf and IEEE802.3cg Draft 2.0

Leveraging existing SCCP protocol for resistance measurement

- Each SCCP transaction is initiated with a PSE Reset Pulse followed by PD Presence Pulse
- While the PD is pulling down for the presence pulse, the PSE can measure current and voltage at its PI and calculate cable resistance
- However, variability of PD Pull down voltage can introduce significant error in calculated resistance
- To eliminate this uncertainty, PD reports to PSE the voltage at its PI during the presence pulse
  - This can be implemented with an ADC measuring and reporting the Pull down voltage at PD's PI

  OR
  - With a voltage shunt regulating a constant voltage and reporting that voltage

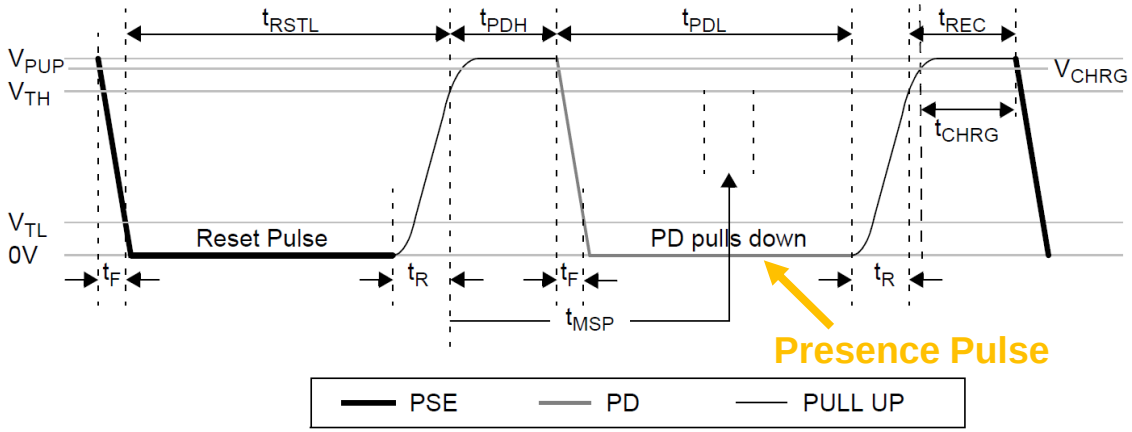
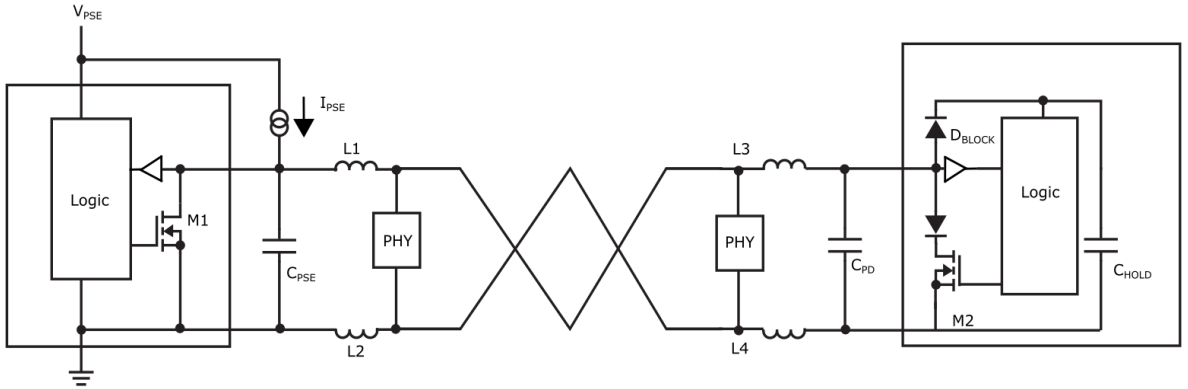


Figure 104–10—Reset command timing diagram



Reference: http://www.ieee802.org/3/bu/public/sep14/gardner_3bu_1_0914.pdf and IEEE802.3cg Draft 2.0

Measurement - Overview

- PSE Sources a current in the range of 9mA to 16mA during PD Presence pulse
  - PSE knows or measures this current value with the accuracy required to support the measurement
  - PSE measures voltage at its PI with the accuracy required to support the measurement
  - PSE-side measurement accuracy is a function of the PSEs desired R_{cable} measurement accuracy, not specified by standard
- PD reports voltage at its PI during the Presence pulse
  - PD reports the voltage as an 8 bit value with an accuracy of +/- 20mV and LSB of 10mV
  - PD also requests a target power level
- PSE then calculates the cable resistance as:
- $$R_{cable} = \frac{V_{meas-PSE} - Vreport_{-PD}}{I_{meas-PSE}}$$
- PSE then reports the power allocated to PD through the PSE Status 2 register (clause 45)

PD and PSE Power Budgeting Calculations

- $R_{CABLE\_MEAS} = \frac{V_{MEAS\_PSE,min} - V_{report\_PD,max}}{I_{MEAS\_PSE,min}}$
- $R_{CABLE} = Min\ ((R_{CABLE\_MEAS}), R_{LOOP(CLASS\text{-}max)})$
- If $P_{PD\_REQ} > P_{PD(max)}$
  - $P_{PD\_ASSIGN} = Min\ \{P_{PD\_REQ}\ , (P_{CLASS(min)} - (I_{PI(MAX)}{}^2 \times R_{CABLE}))\}$
    - Note: When $R_{CABLE} = R_{LOOP(CLASS\text{-}max)}$; $(P_{CLASS(min)} - I_{PI(MAX)}{}^2 \times R_{CABLE}) = P_{PD(max)}$
- Else ($P_{PD\_REQ} \leq P_{PD(max)}$)
  - $P_{PD\_ASSIGN} = P_{PD\_REQ}$
- Sample: $P_{PSE\_ALLOC} = V_{PSE(min)} \times \frac{V_{PSE(min)} - \sqrt{(V_{PSE(min)}{}^2 - 4 \times R_{CABLE} \times P_{PD\_ASSIGN})}}{2 \times R_{CABLE}}$

[a] $V_{PSE(max)}$ is the maximum allowed voltage at the PSE PI over the full range of operating conditions.
[b] $V_{PSE\_OC(min)}$ is the minimum allowed open circuit voltage measured at the PSE PI.
[c] $I_{PI(max)}$ is the maximum current flowing at the PSE and PD PIs except during inrush or an overload condition. $I_{PI(max)}$ may be exceeded during inrush or an overload (see 104.4.6.2). Users are cautioned to be aware of the ampacity of cabling, as installed, and local codes and regulations (see 104.8.1).
[d] $P_{Class(min)}$ is the minimum average available output power at the PSE PI.
[e] $P_{PD(max)}$ is the maximum average available power at the PD PI.

PD INFO Register and PSE Control Register – Optional Implementation

- Modify Table 104-9 and 45-211q as shown in this slide

Table 104-9- CLASS_TYPE_INFO Register Table

Bit(s)	Name	Description	R/W
b[15:12]	Type	15 14 13 12 1 1 1 0 = Type A 1 1 0 1 = Type B 1 0 1 1 = Type C 0 1 1 1 = Type D	RO
b[11]	pd_faulted	1- error condition has occurred… 0 - no error condition detected	RO/LH
b[10]	~~Reserved~~ Cable Resistance Measurement	1- Cable resistance measurement enabled 0 - Cable resistance measurement disabled	RO
b[9:0]	Class	9 8 7 6 5 4 3 2 1 0 1 1 1 1 1 1 1 1 1 0 =Class 0 1 1 1 1 1 1 1 1 0 1 =Class 1 1 1 1 1 1 1 1 0 1 1 =Class 2	RO

Table 45-211q- PODL PSE Control register bit definitions

Bit(s)	Name	Description	R/W
13.0.15:~~23~~	Reserved	Value always 0	RO
13.0.2	Enable cable resistance measurement	1 = Cable resistance measurement enabled 0 = Cable resistance measurement disabled	R/W
13.0.1	Enable power classification	1 = Power classification enabled 0 = Power classification enabled	R/W
13.0.0	PSE Enable	1 = PSE enabled 0 = PSE enabled	R/W

PSE Status 2 register changes

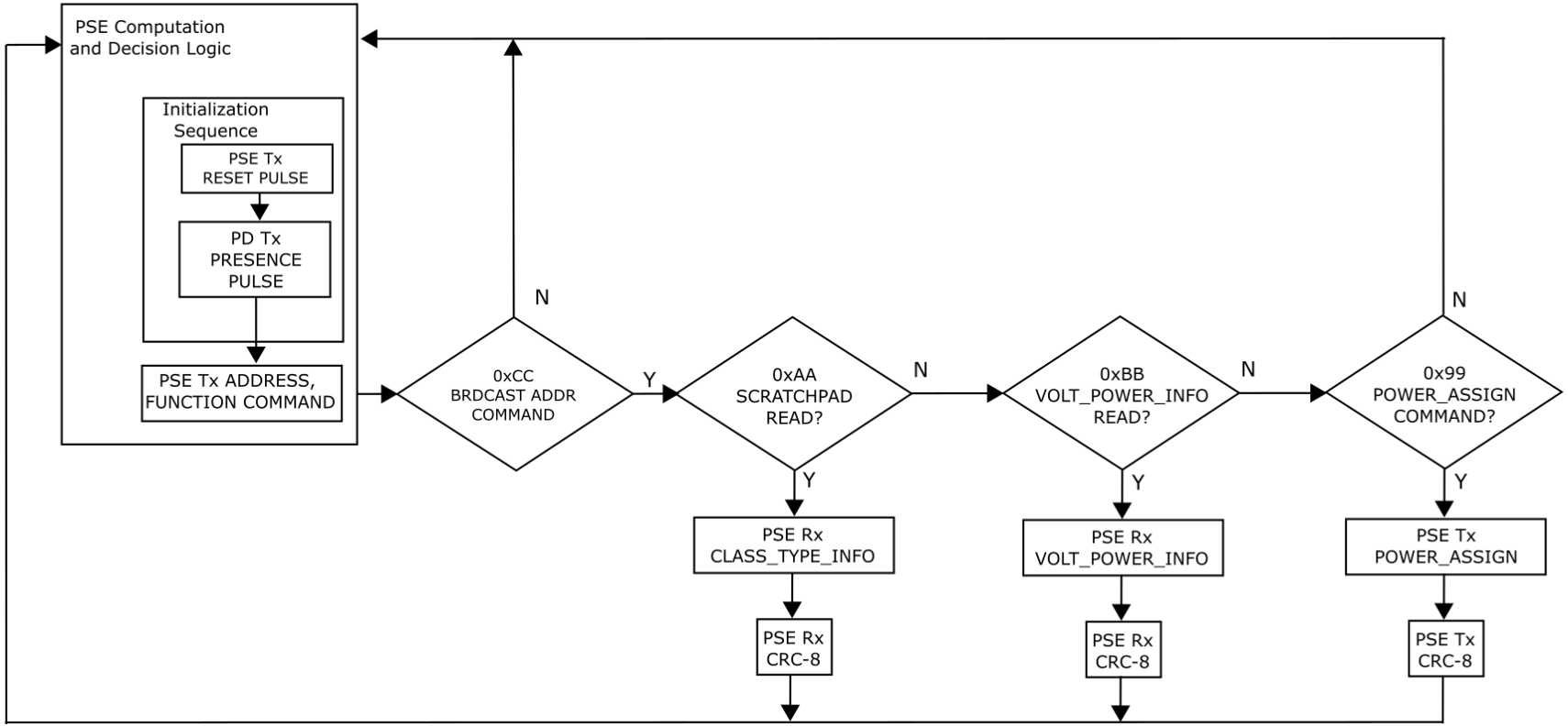
- Modify Table 45-211s as shown in this slide

Table 45–211s—PoDL PSE Status 2 register bit definitions

Bit(s)	Name	Description				R/W
13.2.15	Invalid Class	1 = Invalid PD class detected 0 = No invalid PD class detected				RO/LH
13.2.14:~~39~~	Reserved	Value always 0				RO
13.2.8:3	~~Reserved~~ PD Assigned Power	PD Assigned Power				RO
13.2.2:0	PD Type	2	1	0		RO
		1	1	1	= Unknown	
		1	1	0	= Reserved	
		1	0	~~x~~0	~~Reserved~~ Type E PD	
		0	1	1	= Type D PD	
		0	1	0	= Type C PD	
		0	0	1	= Type B PD	
		0	0	0	= Type A PD	

SCCP Flowchart

- Add Two SCCP Commands:
  - 0xBB : VOLT_POWER_INFO Read
  - 0x99 : POWER_ASSIGN Write
- Replace Figure 104-13 with the figure shown on this slide



SCCP Functions from the PD/ PSE State diagrams

- Modify Clause 104.4 and 104.5 as shown below

104.4.3.5 Functions

do_classification

This function returns the following variables:

CLASS_TYPE_INFO register: (…description of register…)

PSEs that support cable resistance measurement shall also return the VOLT_POWER_INFO, POWER_ASSIGN registers. Refer Table 104-10, 104-11 for description of contents.

104.5.3.5 Functions

do_sccp

This function returns the following variable to the PSE:

CLASS_TYPE_INFO register: refer to Table 104–9 for a description of the contents.

PDs that support cable resistance measurement shall also return the VOLT_POWER_INFO register. Refer Table 104-10 for description of contents.

Optional SCCP Registers

- Add Optional SCCP Registers:

- (Table 104.10) VOLT_POWER_INFO:
  - Voltage Reported by PD as an 8 bit value
  - Initial Power Requested by PD as a 6 bit value
    - (0.3125W/ LSB)
  - 2 bits Reserved

- (Table 104.11) POWER_ASSIGN:
  - PD Assigned Power, by PSE, as a 6 bit value
    - (0.3125W/ LSB)
  - 10 bits Reserved

Table 104-10 VOLT_POWER_INFO Register

Bit(s)	Name	Description	R/W
b[15:14]	Reserved	Value Always 0	RO
b[13:8]	PD Requested Power	Power Requested by PD, 0.3125 W/ LSB	RO
b[7:0]	Voltage at PD PI during Presence Pulse	+/- 20mV tolerance, 10mV per LSB	RO

Table 104-11 POWER_ASSIGN Register

Bit(s)	Name	Description	R/W
b[15:6]	Reserved	Value Always 0	RO
b[5:0]	PD Assigned Power	PD Assigned Power, 0.3125 W/ LSB	WO

SCCP Electrical Requirements

- Modify Table 104-8 as shown in this slide

- PSE Input Logic Low threshold is determined as:
- $V_{TL\text{-}PSE} = V_{TL\text{-}PD} + \text{Link Resistance}_{(max)} \times \text{Probe Current}_{(max)}$
- For Type E PSEs:
  - $\text{Link Resistance}_{(max)} \times \text{Probe Current}_{(max)} = 59\text{ohms} \times 16\text{mA} = 0.944\text{V}$
- Hence, $V_{TL} = 2\text{V}$ for Type E PSEs

- PDs that support cable resistance measurement, have a longer presence pulse to allow 50/60 Hz noise rejection during the measurement

Table 104-8 SCCP electrical requirements

Item	Parameter	Symbol	Unit	Min	Max	PSE/PD type	Additional Information
1	PSE Pull-up Voltage	V_{PUP}	V	$V_{good\_PSE\_max}$	5	All	See Table 104-1
2	PSE Pull-up Current	I_{PUP}	mA	9	16	All	
3	Input Logic High Voltage	V_{TH}	V	3	-	All	
4	Input Logic Low Voltage	V_{TL}	V	-	1	~~All~~ A, B,C,D, Type E PD	
5	Input Logic Low Voltage	V_{TL}	V	-	2	Type E PSE	
~~5~~ 6	Sink Current	I_L	mA	30	-	All	$V_{port} > 0.8\text{V}$
15	Presence-Detect Low Time	t_{PDLOW}	ms	2.5	7.5	A, B, C, D	
				2.8	5.2	E	
				21	31	E	PDs that support link segment resistance measurement

104.7 Baseline Text

- Modify Clause 104.7

Implementation of SCCP by PSEs and PDs that present a valid detection signature is optional. PDs that present an invalid detection signature as specified in Table 104–6 shall implement SCCP. The PSE acts as a master during the SCCP exchange, controlling the PD that acts as the slave device. SCCP is a current-sinking, wired-OR (e.g., open-drain or open-collector), half-duplex bidirectional serial data bus. The PSE sources the required pull-up current. ~~The logic high voltage is limited by the voltage signature device at the PD.~~ PDs can derive power from the PSE's pull-up current during classification via the PD PI.

Measurement of cable resistance by PSEs and PDs that implement SCCP is optional. PSEs and PDs that implement cable resistance measurement shall support the VOLT_POWER_INFO and POWER_ASSIGN registers (Table 104.10, 104.11). PSEs that implement cable resistance measurement shall report assigned power through PSE Status Register 2 (See 45.2.7b.3).

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Thank You!

QUESTIONS? FEEDBACK?