45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

Commented [PB1]: #315, #276, #277, #278: PLCA registers
Add PLCA as a separate MMD

Add following text after "For 10, 100 and 1000 Mb/s PHYs, further management capability is defined in the Clause 22 extension MMD."

For PHYs supporting the optional PLCA RS defined in clause 148, namely 10BASE-T1S, additional management capabilities are defined in the PLCA MMD.

Change Table 45–1 as follows (unchanged rows not shown):

Table 45–1—MDIO Manageable Device addresses

Device address	MMD name
…	…
14 through ~~28~~ 27	Reserved
28	PLCA
…	…

Change Table 45–2 as follows (unchanged rows not shown):

Table 45–2—Devices in package registers bit definitions

Bits	Name	Description	R/W
…	…	…	…
m.6.13	Clause 22 extension present	1 = Clause 22 extension present in package 0 = Clause 22 extension not present in package	RO
m.6.12	PLCA present	1 = PLCA present in package 0 = PLCA not present in package	RO
m.6.~~12~~11:0	Reserved	Value always 0	RO
…	…	…	…

45.2.1 PMA/PMD register

Change the row for 1.2103 through 1.2303 and insert new rows in Table 45–3 as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.2103 through 1.2293~~303~~	Reserved	
1.2294	10BASE-T1L PMA control	45.2.1.174a
1.2295	10BASE-T1L PMA status	45.2.1.174b
1.2296	Reserved	
1.2297	Reserved	
1.2298	10BASE-T1L test mode control	45.2.1.174c
1.2299	10BASE-T1S PMA control	45.2.1.174d
1.2300	10BASE-T1S PMA status	45.2.1.174e
1.2301 through 1.2302	Reserved	
1.2303	10BASE-T1S test mode control	45.2.1.174f
…		

45.2.1.16 BASE-T1 PMA/PMD extended ability register (1.18)

Change the row for 1.18.15.2 and insert new rows in Table 45–19 as follows (unchanged rows not shown):

Table 45–19—BASE-T1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[1]
1.18.15:~~2~~4	Reserved	Value always 0	RO
1.18.3	10BASE-T1S ability	1 = PMA/PMD is able to perform 10BASE-T1S 0 = PMA/PMD is not able to perform 10BASE-T1S	RO
1.18.2	10BASE-T1L ability	1 = PMA/PMD is able to perform 10BASE-T1L 0 = PMA/PMD is not able to perform 10BASE-T1L	RO
…			

[1]RO = Read only

45.2.1.173 BASE-T1 PMA/PMD control register (Register 1.2100)

Change the row for 1.2100.3:0 in Table 45–141 as follows (unchanged rows not shown):

Table 45–141—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[2]
…			
1.2100.3:0	Type Selection	3 2 1 0 1 x x x = Reserved 0 1 x x = Reserved 0 0 1 1 = 10BASE-T1S 0 0 1 ~~x~~0 = ~~Reserved~~10BASE-T1L 0 0 0 1 = 1000BASE-T1 0 0 0 0 = 100BASE-T1	R/W

Insert 45.2.1.174a through 45.2.1.174h after 45.2.1.174 as follows:

45.2.1.174a 10BASE-T1L PMA control register (Register 1.2294)

The assignment of bits in the 10BASE-T1L PMA control register is shown in Table 45–142a.

Table 45–142a—10BASE-T1L PMA control register bit definitions

Bit(s)	Name	Description	R/W[3]
1.2294.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2294.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2294.13	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
1.2294.12	Transmit voltage amplitude control	1 = Enable 2.4 Vpp operating mode 0 = Enable 1.0 Vpp operating mode	R/W
1.2294.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2294.10	EEE functionality	1 = Enable EEE functionality 0 = Disable EEE functionality	R/W
1.2294.9:0	Reserved	Value always 0	RO

45.2.1.174a.1 PMA/PMD reset (1.2294.15)

Resetting the 10BASE-T1L PMA/PMD is accomplished by setting bit 1.2294.15 to a one. This action shall set all 10BASE-T1L PMA/PMD registers to their default states. As a consequence, this action may change the internal state

[2]RO = Read only, R/W = Read/Write

[3]RO = Read only, R/W = Read/Write, SC = Self clearing

of the 10BASE-T1L PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self clearing, and the 10BASE-T1L PMA/PMD shall return a value of one in bit 1.2294.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1L PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2294.15.

During a reset, the 10BASE-T1L PMA/PMD shall respond to reads from bits 1.2294.15, 1.8.15:14, and 1.0.15. Reads for all other bits shall be ignored.

This operation may interrupt data communication.

Bit 1.2294.15 is a copy of bit 1.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1L PMA/PMD.

45.2.1.174a.2 Transmit disable (1.2294.14)

When bit 1.2294.14 is set to a one, the PMA shall disable output on the transmit path. When bit 1.2294.14 is set to a zero, the PMA shall enable output on the transmit path.

Bit 1.2294.14 is a copy of bit 1.9.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.174a.3 Loopback (1.2294.13)

The 10BASE-T1L PMA shall be placed in loopback mode of operation when bit 1.2294.13 is set to a one. When bit 1.2294.13 is set to a one, the 10BASE-T1L PMA shall accept data on the transmit path and return it on the receive path. The default value of bit 1.2294.13 is zero. Bit 1.2294.13 is a copy of 1.0.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.1.174a.4 Transmit voltage amplitude control (1.2294.12)

When bit 1.2294.12 is set to one, the 10BASE-T1L PMA shall transmit using the 2.4 Vpp operating mode according to 146.5.4.1. When bit 1.2294.12 is set to zero, the 10BASE-T1L PMA shall transmit using the 1.0 Vpp operating mode according to 146.5.4.1. The default value of bit 1.2294.12 is zero.

45.2.1.174a.5 Low-power (1.2294.11)

When the low-power ability is supported, the 10BASE-T1L PMA/PMD may be placed into a low-power mode by setting bit 1.2294.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the 10BASE-T1L PMA/PMD. The behavior of the 10BASE-T1L PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2294.11 is zero.

NOTE—This operation may interrupt data communication. The data path of the 10BASE-T1L PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

Bit 1.2294.11 is a copy of bit 1.0.11 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the 10BASE-T1L PMA/PMD in low-power mode.

45.2.1.174a.6 EEE functionality(1.2294.10)

When bit 1.2294.10 is set to one, the 10BASE-T1L PHY shall enable EEE functionality. When bit 1.2294.10 is set to zero, the 10BASE-T1L PHY shall disable EEE functionality. The default value of bit 1.2294.10 is zero.

45.2.1.174b 10BASE-T1L PMA status register (Register 1.2295)

The assignment of bits in the 10BASE-T1L PMA status register is shown in Table 45–142b.

Table 45–142b—10BASE-T1L PMA status register bit definitions

Bit(s)	Name	Description	R/W[4]
1.2295.15:14	Reserved	Value always 0	RO
1.2295.13	Loopback ability	1 = PHY has loopback ability 0 = PHY has no loopback ability	RO
1.2295.12	2.4 Vpp operating mode ability	1 = PHY has 2.4 Vpp operating mode ability 0 = PHY does not have 2.4 Vpp operating mode ability	RO
1.2295.11	Reserved	Value always 0	RO
1.2295.10	EEE Ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2295.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2295.8	Low-power ability	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability	RO
1.2295.7:3	Reserved	Value always 0	RO
1.2295.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2295.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.2295.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

45.2.1.174b.1 Loopback ability (1.2295.13)

When read as a one, this bit indicates that the 10BASE-T1L PHY supports PMA loopback. When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support PMA loopback.

45.2.1.174b.2 2.4 Vpp operating mode ability (1.2295.12)

When read as a one, this bit indicates that the 10BASE-T1L PHY supports a transmit level of 2.4 Vpp. When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support a transmit level of 2.4 Vpp.

45.2.1.174b.3 EEE ability (1.2295.10)

When read as a one, this bit indicates that the 10BASE-T1L PHY supports EEE. When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support EEE.

[4]RO = Read only, LL = Latching Low

45.2.1.174b.4 Receive fault ability (1.2295.9)

When read as a one, bit 1.2295.9 indicates that the 10BASE-T1L PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2295.9 indicates that the 10BASE-T1L PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.174b.5 Low-power ability (1.2295.8)

When read as a one, bit 1.2295.8 indicates that the 10BASE-T1L PMA/PMD supports the low-power ability. When read as a zero, bit 1.2295.8 indicates that the 10BASE-T1L PMA/PMD does not support the low-power feature. If the 10BASE-T1L PMA/PMD supports the low-power feature, then it is controlled using either bit 1.2294.11 or bit 1.0.11.

45.2.1.174b.6 Receive polarity (1.2295.2)

When read as a zero, bit 1.2295.2 indicates that the polarity of the receiver is not reversed. When read as a one, bit 1.2295.2 indicates that the polarity of the receiver is reversed.

45.2.1.174b.7 Receive fault (1.2295.1)

When read as a one, bit 1.2295.1 indicates that the 10BASE-T1L PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2295.1 indicates that the 10BASE-T1L PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2295.9. The 10BASE-T1L PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit.

45.2.1.174b.8 Receive link status (1.2295.0)

When read as a one, bit 1.2295.0 indicates that the 10BASE-T1L PMA/PMD receive link is up. When read as a zero, bit 1.2295.0 indicates that the 10BASE-T1L PMA/PMD receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.1.174c 10BASE-T1L test mode control register (Register 1.2298)

The assignment of bits in the 10BASE-T1L test mode control register is shown in Table 45–142c. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–142c—10BASE-T1L test mode control register bit definitions

Bit(s)	Name	Description	R/W[5]
1.2298.15:13	Test mode control	15 14 13 1 x x = Reserved 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2298.12:0	Reserved	Value always 0	RO

45.2.1.174c.1 Test mode control (1.2298.15:13)

Transmitter test mode operations defined by bits 1.2298.15:13, are described in 146.5.2. The default value for bits 1.2298.15:13 is zero.

45.2.1.174d 10BASE-T1S PMA control register (Register 1.2299)

The assignment of bits in the 10BASE-T1S PMA control register is shown in Table 45–142d.

Table 45–142d—10BASE-T1S PMA control register bit definitions

Bit(s)	Name	Description	R/W[6]
1.2299.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2299.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2299.13	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
1.2299:12	Reserved	Value always 0	RO
1.2299.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2299.10	Multidrop mode	1 = Enable operation over mixing segment network 0 = Disable operation over mixing segment network	R/W
1.2299.9:0	Reserved	Value always 0	RO

[5]RO = Read only, R/W = Read/Write
[6]RO = Read only, R/W = Read/Write, SC = Self clearing

45.2.1.174d.1 PMA/PMD reset (1.2299.15)

Resetting the 10BASE-T1S PMA/PMD is accomplished by setting bit 1.2299.15 to a one. This action shall set all 10BASE-T1S PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1S PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self clearing, and the 10BASE-T1S PMA/PMD shall return a value of one in bit 1.2299.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1S PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2299.15.

During a reset, the 10BASE-T1S PMA/PMD shall respond to reads from bits 1.2299.15, 1.8.15:14, and 1.0.15. Reads for all other bits shall be ignored.

This operation may interrupt data communication.

Bit 1.2299.15 is a copy of 1.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1S PMA/PMD.

45.2.1.174d.2 Transmit disable (1.2299.14)

When bit 1.2299.14 is set to a one, the PMA shall disable output on the transmit path. When bit 1.2299.14 is set to a zero, the PMA shall enable output on the transmit path.

Bit 1.2299.14 is a copy of bit 1.9.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.174d.3 Loopback (1.2299.13)

The 10BASE-T1S PMA shall be placed in loopback mode of operation when loopback bit 1.2299.13 is set to a one~~, and PLCA enable bit in MDIO register 3.2291.13 is set to a zero~~. When in loopback the 10BASE-T1S PMA shall accept data on the transmit path and return it on the receive path. The default value of bit 1.2299.13 is zero. Bit 1.2299.13 is a copy of 1.0.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

Commented [PB2]: #315, #276, #277, #278: PLCA registers
Remove PLCA registers from PMA

45.2.1.174d.4 Low-power (1.2299.11)

When the low-power ability is supported, the 10BASE-T1S PMA/PMD may be placed into a low-power mode by setting bit 1.2299.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the 10BASE-T1S PMA/PMD. The behavior of the 10BASE-T1S PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2299.11 is zero.

NOTE—This operation interrupts data communication. The data path of the 10BASE-T1S PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

Bit 1.2299.11 is a copy of bit 1.0.11 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the 10BASE-T1S PMA/PMD in low-power mode.

45.2.1.174d.5 Multidrop mode (1.2299.10)

The 10BASE-T1S PMA/PMD shall operate in multidrop mode over a mixing segment network when bit 1.2299.10 is set to a one. The default value of bit 1.2299.10 is zero. If multidrop mode is not supported according to bit 1.2300.7, writing to bit 1.2299.10 shall have no effect.

45.2.1.174e 10BASE-T1S PMA status register (Register 1.2300)

The assignment of bits in the 10BASE-T1S PMA status register is shown in Table 45–142e.

Table 45–142e—10BASE-T1S PMA status register bit definitions

Bit(s)	Name	Description	R/W[7]
1.2300.15:14	Reserved	Value always 0	RO
1.2300.13	Loopback ability	1 = PHY has loopback ability 0 = PHY has no loopback ability	RO
1.2300.12:10	Reserved	Value always 0	RO
1.2300.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2300.8	Low-power ability	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability	RO
1.2300.7	Multidrop ability	1 = PMA/PMD has the ability to operate over a mixing segment network 0 = PMA/PMD does not have the ability to operate over a mixing segment network	RO
1.2300.6:2	Reserved	Value always 0	RO
1.2300.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.2300.0	Reserved	Value always 0	RO

45.2.1.174e.1 10BASE-T1S loopback ability (1.2300.13)

When read as a one, this bit indicates that the 10BASE-T1S PHY supports PMA loopback. When read as a zero, this bit indicates that the 10BASE-T1S PHY does not support PMA loopback.

45.2.1.174e.2 Receive fault ability (1.2300.9)

When read as a one, bit 1.2300.9 indicates that the 10BASE-T1S PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2300.9 indicates that the 10BASE-T1S PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.174e.3 Low-power ability (1.2300.8)

When read as a one, bit 1.2300.8 indicates that the 10BASE-T1S PMA/PMD supports the low-power ability. When read as a zero, bit 1.2300.8 indicates that the 10BASE-T1S PMA/PMD does not support the low-power feature. If the 10BASE-T1S PMA/PMD supports the low-power feature, then it is controlled using either bit 1.2299.11 or bit 1.0.11.

45.2.1.174e.4 Multidrop ability (1.2300.7)

When read as a one, bit 1.2300.7 indicates that the 10BASE-T1S PMA/PMD supports multidrop operation over a mixing segment network. When read as a zero, bit 1.2300.7 indicates that the 10BASE-T1S PMA/PMD does not

[7]RO = Read only

support multidrop operation over a mixing segment network. If the 10BASE-T1S PMA/PMD supports multidrop operation, then it is controlled using bit 1.2299.10, otherwise bit 1.2299.10 has no effect.

45.2.1.174e.5 Receive fault (1.2300.1)

When read as a one, bit 1.2300.1 indicates that the 10BASE-T1S PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2300.1 indicates that the 10BASE-T1S PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2300.9. The 10BASE-T1S PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit.

45.2.1.174f 10BASE-T1S test mode control register (Register 1.2303)

The assignment of bits in the 10BASE-T1S test mode control register is shown in Table 45–142f. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–142f—10BASE-T1S test mode control register bit definitions

Bit(s)	Name	Description	R/W[8]
1.2303.15:13	Test mode control	15 14 13 1 1 x = Reserved 1 0 1 = Reserved 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2303.12:0	Reserved	Value always 0	RO

45.2.1.174f.1 Test mode control (1.2303.15:13)

Transmitter test mode operations defined by bits 1.2303.15:13, are described in 147.5.1. The default value for bits 1.2303.15:13 is zero.

[8]RO = Read only, R/W = Read/Write

45.2.3 PCS Registers

Change the row for 3.1809 through 3.2303 and insert new rows in Table 45–176 as follows (unchanged rows not shown):

Table 45–176—PCS registers

Register address	Register name	Subclause
…		
3.1809 through 3.~~2303~~2277	Reserved	
3.2278	10BASE-T1L PCS control	45.2.3.58a
3.2279	10BASE-T1L PCS status 1	45.2.3.58b
3.2280 through 3.229~~088~~	Reserved	
~~3.2289~~	~~10BASE-T1S PLCA control 1~~	~~45.2.3.58c~~
~~3.2290~~	~~10BASE-T1S PLCA control 2~~	~~45.2.3.58d~~
3.2291	10BASE-T1S PCS control	45.2.3.58e
3.2292	10BASE-T1S PCS status 1	45.2.3.58f
3.2293 through 3.2303	Reserved	
…		

Commented [PB3]: #315, #276, #277, #278: PLCA registers
Remove PLCA registers from PCS

Insert 45.2.3.58a through 45.2.3.58i after 45.2.3.58 as follows:

45.2.3.58a 10BASE-T1L PCS control register (Register 3.2278)

The assignment of bits in the 10BASE-T1L PCS control register is shown in Table 45–220a. The default value for each bit of the 10BASE-T1L PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–220a—10BASE-T1L PCS control register bit definitions

Bit(s)	Name	Description	R/W[9]
3.2278.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2278.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2278.13:0	Reserved	Value always 0	RO

[9]RO = Read only, R/W = Read/Write, SC = Self Clearing

45.2.3.58a.1 PCS reset (3.2278.15)

Resetting the 10BASE-T1L PCS is accomplished by setting bit 3.2278.15 to a one. This action shall set all 10BASE-T1L PCS registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1L PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1L PCS shall return a value of one in bit 3.2278.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1L PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2278.15. During a reset, a PCS shall respond to reads from bits 3.0.15, 3.8.15:14, and 3.2278.15. Reads for all other bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2278.15 is a copy of 3.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1L PCS.

45.2.3.58a.2 Loopback (3.2278.14)

The 10BASE-T1L PCS shall be placed in a loopback mode of operation when bit 3.2278.14 is set to a one. When bit 3.2278.14 is set to a one, the 10BASE-T1L PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2278.14 is zero.

Bit 3.2278.14 is a copy of 3.0.14 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.58b 10BASE-T1L PCS status 1 register (Register 3.2279)

The assignment of bits in the 10BASE-T1L PCS status 1 register is shown in Table 45–220b. All the bits in the 10BASE-T1L PCS status 1 register are read only; a write to the 10BASE-T1L PCS status 1 register shall have no effect.

Table 45–220b—10BASE-T1L PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[10]
3.2279.15:12	Reserved	Value always 0	RO
3.2279.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2279.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2279.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2279.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2279.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2279.6:3	Reserved	Value always 0	RO
3.2279.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2279.1:0	Reserved	Value always 0	RO

[10]RO = Read only

45.2.3.58b.1 Tx LPI received (3.2279.11)

When read as a one, bit 3.2279.11 indicates that the transmit 10BASE-T1L PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2279.11 indicates that the 10BASE-T1L PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.58b.2 Rx LPI received (3.2279.10)

When read as a one, bit 3.2279.10 indicates that the receive 10BASE-T1L PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2279.10 indicates that the 10BASE-T1L PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.58b.3 Tx LPI indication (3.2279.9)

When read as a one, bit 3.2279.9 indicates that the transmit 10BASE-T1L PCS is currently receiving LPI signals. When read as a zero, bit 3.2279.9 indicates that the 10BASE-T1L PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.58b.4 Rx LPI indication (3.2279.8)

When read as a one, bit 3.2279.8 indicates that the receive 10BASE-T1L PCS is currently receiving LPI signals. When read as a zero, bit 3.2279.8 indicates that the 10BASE-T1L PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.58b.5 Fault (3.2279.7)

When read as a one, bit 3.2279.7 indicates that the 10BASE-T1L PCS has detected a fault condition on either the transmit or receive path. When read as a zero, bit 3.2279.7 indicates that the 10BASE-T1L PCS has not detected a fault condition.

45.2.3.58b.6 PCS receive link status (3.2279.2)

When read as a one, bit 3.2279.2 indicates that the 10BASE-T1L PCS receive link is up. When read as a zero, bit 3.2279.2 indicates that the 10BASE-T1L PCS receive link was down since the last read from this bit. This bit is a latching low reflection of the variable scr_status. If the bit is read, while scr_status = OK, then this bit is set. If scr_status = NOT_OK, then this bit is reset.

~~**45.2.3.58c 10BASET1S PLCA control 1 (Register 3.2289)**~~

~~The assignment of bits in the 10BASE-T1S PLCA control 1 register is shown in Table 45–220c.~~

Commented [PB4]: #315, #276, #277, #278: PLCA registers
Remove PLCA registers from PCS

~~**Table 45–220c—10BASET1S PLCA control 1 register bit definitions**~~

~~Bit(s)~~	~~Name~~	~~Description~~	~~R/W[11]~~
~~3.2289.15:8~~	~~MAX_ID~~	~~8 bit field indicating the max number of nodes on the PLCA network~~	~~R/W~~
~~3.2289.7:0~~	~~local_nodeID~~	~~8 bit field indicating the local ID of the node on the PLCA network~~	~~R/W~~

~~[11]R/W = Read/Write~~

~~45.2.3.58c.1 MAX_ID (3.2289.15:8)~~

~~When 10BASE-T1S PCS is in PLCA mode and local_nodeID is set to value 0, bits 3.2289.15:8 define the number of maximum nodes that can be handled on the PLCA network. The default value of bits 3.2289.15:8 is 8.~~

~~45.2.3.58c.2 local_nodeID (3.2289.7:0)~~

~~When 10BASE-T1S PCS is in PLCA mode, bits 3.2289.7:0 define the ID of the node in the network. The default value of bits 3.2289.7:0 is 255.~~

~~45.2.3.58d 10BASET1S-PLCA control 2 (Register 3.2290)~~

~~The assignment of bits in the 10BASE-T1S PLCA control 2 register is shown in Table 45–220d.~~

Commented [PB5]: #315, #276, #277, #278: PLCA registers
Remove PLCA registers from PCS

~~Table 45–220d—10BASET1S-PLCA control 2 register bit definitions~~

~~Bit(s)~~	~~Name~~	~~Description~~	~~R/W[12]~~
~~3.2290.15:0~~	~~TO_TIMER~~	~~16 bit field indicating the time between PLCA transmit opportunities expressed in bit times~~	~~R/W~~

~~45.2.3.58d.1 TO_TIMER (3.2290.15:0)~~

~~When 10BASE-T1S PCS is in PLCA mode, bits 3.2290.15:0 define the time between PLCA transmit opportunities expressed in bit times. The default value of bits 3.2290.15:0 is 20.~~

45.2.3.58e 10BASE-T1S PCS control register (Register 3.2291)

Commented [PB6]: #315, #276, #277, #278: PLCA registers
Remove PLCA registers from PCS

The assignment of bits in the 10BASE-T1S PCS control register is shown in Table 45–220e. The default value for each bit of the 10BASE-T1S PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–220e—10BASE-T1S PCS control register bit definitions

Bit(s)	Name	Description	R/W[13]
3.2291.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2291.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
~~3.2291.13~~	~~PLCA enable~~	~~1 = Enable PLCA mode~~ ~~0 = Disable PLCA mode~~	~~R/W~~
~~3.2291.12~~	~~PLCA reset~~	~~1 = PLCA reset~~ ~~0 = Normal operation~~	~~R/W, SC~~
3.2291.~~11~~13:0	Reserved	Value always 0	RO

~~[12]R/W = Read/Write~~

[13]RO = Read only, R/W = Read/Write, SC = Self Clearing

45.2.3.58e.1 PCS reset (3.2291.15)

Resetting the 10BASE-T1S PCS is accomplished by setting bit 3.2291.15 to a one. This action shall set all 10BASE-T1S PCS registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1S PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1S PCS shall return a value of one in bit 3.2291.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1S PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2291.15. During a reset, a PCS shall respond to reads from bits 3.0.15, 3.8.15:14, and 3.2291.15. Reads for all other bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2294.15 is a copy of 3.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1S PCS.

45.2.3.58e.2 Loopback (3.2291.14)

The 10BASE-T1S PCS shall be placed in a loopback mode of operation when bit 3.2291.14 is set to a one. When bit 3.2291.14 is set to a one, the 10BASE-T1S PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2291.14 is zero.

Bit 3.2291.14 is a copy of 3.0.14 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

~~45.2.3.58e.3 PLCA enable (3.2291.13)~~

~~The 10BASE-T1S PCS shall be placed in PLCA mode of operation when bit 3.2291.13 is set to a one. The default value of bit 3.2291.13 is zero.~~

~~45.2.3.58e.4 PLCA reset (3.2291.12)~~

~~Resetting the 10BASE-T1S PCS PLCA state is accomplished by setting bit 3.2291.12 to a one. As a consequence, this action may change the internal state of the 10BASE-T1S PCS and the state of the physical link. This bit is self-clearing, and the 10BASE-T1S PCS shall return a value of one in bit 3.2291.12 when a PLCA reset is in progress; otherwise, it shall return a value of zero.~~

~~NOTE—This operation may interrupt data communication.~~

45.2.3.58f 10BASE-T1S PCS status 1 register (Register 3.2292)

The assignment of bits in the 10BASE-T1S PCS status 1 register is shown in Table 45–220f. All the bits in the 10BASE-T1S PCS status 1 register are read only; a write to the 10BASE-T1S PCS status 1 register shall have no effect.

Table 45–220f—10BASE-T1S PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[14]
3.2292.15:~~14~~13	Reserved	Value always 0	RO
~~3.2292.13~~	~~PLCA ability~~	~~1 = Supports PLCA mode~~ ~~0 = Does not support PLCA mode~~	~~RO~~

[14]RO = Read only, LH = Latching high, LL = Latching low

Commented [PB7]: #315, #276, #277, #278: PLCA registers
Remove PLCA registers from PCS

Commented [PB8]: #315, #276, #277, #278: PLCA registers
Remove PLCA registers from PCS

Commented [PB9]: #315, #276, #277, #278: PLCA registers
Remove PLCA registers from PCS

3.2292.12:8	Reserved	Value always 0	RO
3.2292.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2292.6:0	Reserved	Value always 0	RO

~~45.2.3.58f.1 PLCA ability (3.2292.13)~~

~~When read as a one, this bit indicates that the 10BASE-T1S PHY supports PLCA. When read as a zero, this bit indicates that the 10BASE-T1S PHY does not support PLCA.~~

45.2.3.58f.2 Fault (3.2292.7)

When read as a one, bit 3.2292.7 indicates that the 10BASE-T1S PCS has detected a fault condition on either the transmit or receive path. When read as a zero, bit 3.2292.7 indicates that the 10BASE-T1S PCS has not detected a fault condition.

45.2.13 PLCA registers

The assignment of registers in the PLCA is shown in Table 45–354.

Table 45–176—PLCA registers

Register address	Register name	Subclause
28.0	PLCA control 1	45.2.13.1
28.1	PLCA control 2	45.2.13.2
28.2	PLCA TO Timer	45.2.13.3
28.3 through 28.4	Reserved	
28.5, 28.6	PLCA devices in package	45.2.13.4
28.7 through 28.14	Reserved	
28.15	PLCA status	45.2.13.5
28.16 through 28.65 535	Reserved	

Commented [PB10]: #315, #276, #277, #278: PLCA registers
Remove PLCA registers from PCS

Commented [PB11]: #315, #276, #277, #278: PLCA registers
Add subclause for PLCA registers

Commented [PB12]: #556: PLCA status
Add PLCA status register from http://www.ieee802.org/3/cg/public/adhoc/beruto_3cg_PLCA_status.pdf slide 8, moving register to appropriate location as per comments #315, #276, #277, #278

45.2.13.1 PLCA Control 1 register (Register 28.0)

The assignment of bits in the PLCA control 1 register is shown in Table 45–355

Table 45-355—PLCA control 1 register bit definitions

Bit(s)	Name	Description	R/W[15]
28.0:15	PLCA enable	1 = Enable PLCA 0 = Disable PLCA	R/W
28.0:14	PLCA reset	1 = PLCA reset 0 = Normal operation	R/W, SC
28.0:13:0	Reserved	Value always 0	RO

45.2.13.1.1 PLCA enable (28.0.15)

The PHY shall be placed in PLCA mode of operation when bit 28.0.15 is set to one. The default value of bit 28.0.15 is zero.

45.2.13.1.2 PLCA reset (28.0.14)

Resetting the PLCA functions is accomplished by setting bit 28.0.14 to one. This bit is self-clearing, and shall read as one while PLCA reset is in progress, otherwise, it shall read as 0.

NOTE—This operation may interrupt data communication.

45.2.13.2 PLCA Control 2 register (Register 28.1)

The assignment of bits in the PLCA control 2 register is shown in Table 45–356

Table 45-356—PLCA control 2 register bit definitions

Bit(s)	Name	Description	R/W[16]
28.1.15:8	MAX_ID	8 bit field indicating the max number of nodes on the PLCA network	R/W
28.1.7:0	local_nodeID	8 bit field indicating the local ID of the node on the PLCA network	R/W

Commented [PB13]: #556: PLCA status
Add PLCA status bit from http://www.ieee802.org/3/cg/public/adhoc/beruto_3cg_PLCA_status.pdf slide 8, moving register to appropriate location as per comments #315, #276, #277, #278

[15] RO = Read only, R/W = Read/Write, SC = Self Clearing
[16] R/W = Read/Write

45.2.13.2.1 MAX_ID (28.1.15:8)

When PLCA is enabled and local_nodeID is set to value 0, bits 28.1.15:8 define the number of maximum nodes that can be handled on the PLCA network. The default value of bits 28.1.15:8 is 8.

45.2.13.2.2 local_nodeID (28.1.7:0)

When PLCA is enabled, bits 28.1.7:0 define the ID of the node in the network. The default value of bits 28.1.7:0 is 255.

45.2.13.3 PLCA TO Timer register (Register 28.2)

The assignment of bits in the PLCA TO Timer register is shown in Table 45–357

Table 45-357—PLCA TO Timer register bit definitions

Bit(s)	Name	Description	R/W[17]
28.2.15:0	TO_TIMER	16 bit field indicating the time between PLCA transmit opportunities expressed in bit times	R/W

45.2.13.3.1 TO_TIMER (28.2.15:0)

When PLCA is enabled, bits 28.2.15:0 define the time between PLCA transmit opportunities expressed in bit times. The default value of bits 28.2.15:0 is 20.

45.2.13.4 PLCA devices in package (Registers 28.5 and 28.6)

The PLCA devices in package registers are defined in Table 45–2.

45.2.13.5 PLCA Control 1 register (Register 28.15)

The assignment of bits in the PLCA status register is shown in Table 45–358

Table 45-358—PLCA status register bit definitions

Bit(s)	Name	Description	R/W[18]
28.15:15	PLCA status	1 = PLCA is actively receiving or transmitting the BEACON 0 = PLCA is not receiving or transmitting the BEACON	RO
28.15:14:0	Reserved	Value always 0	RO

[17] R/W = Read/Write
[18] RO = Read only

45.2.13.5.1 PLCA status (28.15.15)

Read-only bit indicating whether PLCA RS is actively receiving or transmitting the BEACON.