IEEE P802.3cg 10BASE-T1S MDI Parallel Inductance

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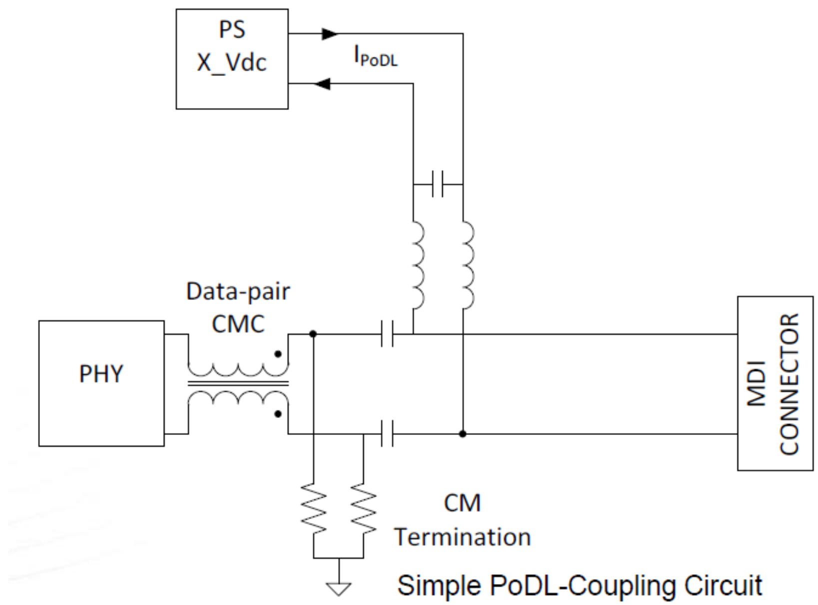
Purpose

- The purpose of this presentation is to:
  - Discuss a proposed resolution to Draft 2.0 comment #364:
    - "Where do the values for L come from? Unless we use PoDL they seem way too high. It states nowhere if this is optional or for PoDL only."
  - Suggest keeping inductance limits to allow for optional "engineered" power
  - Examine the effect of inductive loading presented by a node on the 10BASE-T1S mixing segment
  - Propose revisions to 147.9.2 and Table 147-3

Adding PoDL or Engineered Power

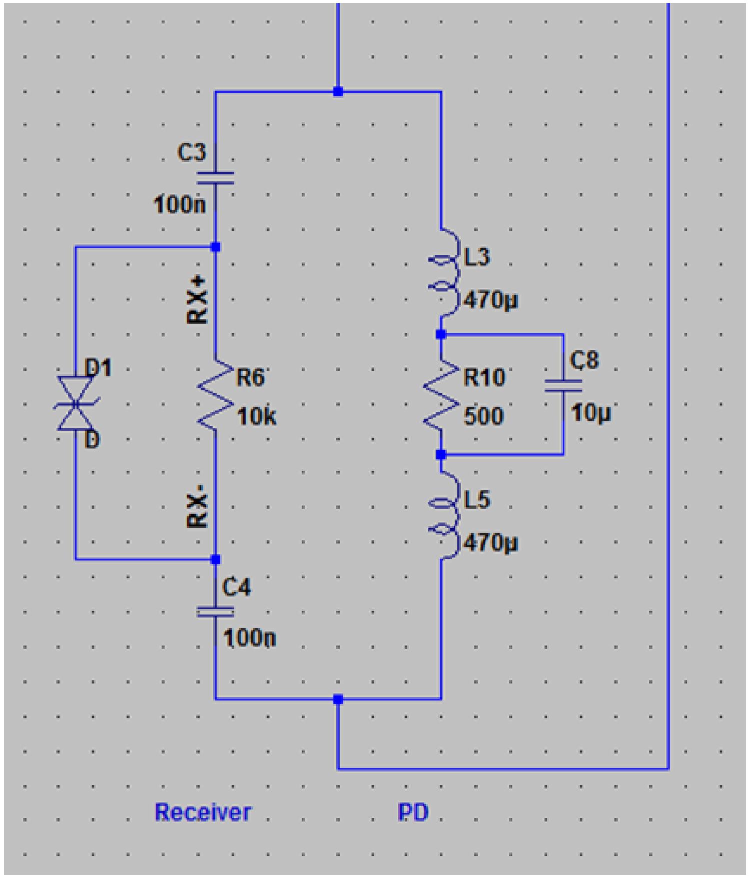
- PoDL is not currently planned for 10BASE-T1S
- Do not want to preclude “engineered” power
  - See [17 Jan 2018 Ad Hoc] on optional engineered power
- For PoDL or engineered power, PSE and PD couple to bus via a pair of inductors
  - PSE is shown; PD is identical
- If inductors are used, need inductance limits to allow (at minimum) a working 8-node system

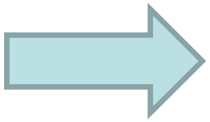


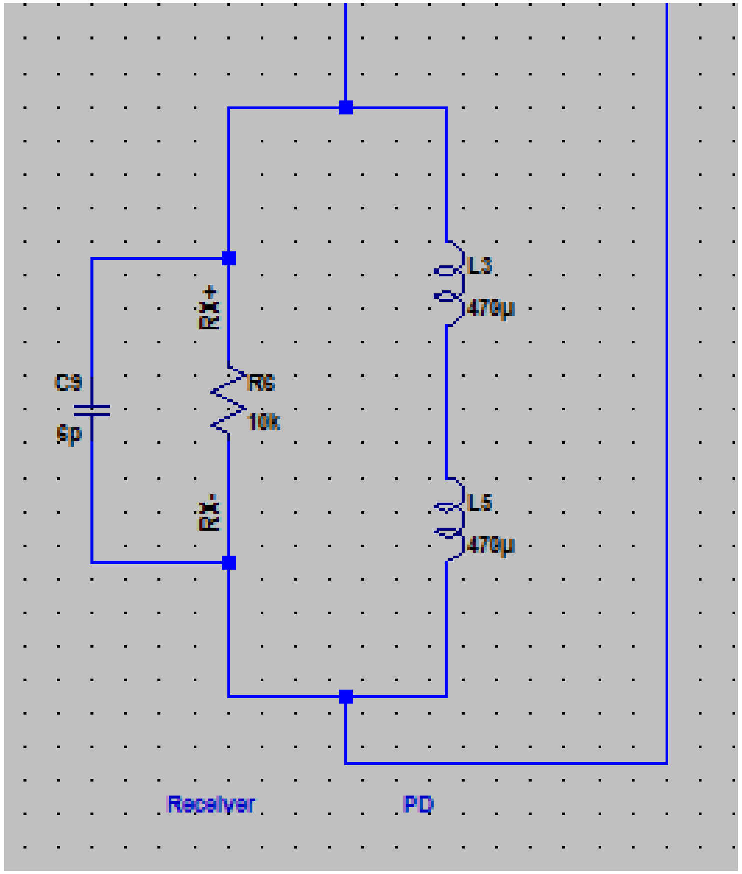
Simple PoDL-Coupling Circuit

Taken from:
PRACTICAL CONSIDERATIONS FOR IMPLEMENTING PoDL-COUPLING CIRCUITS
http://www.ieee802.org/3/bu/public/jan15/pischl_3bu_1_0115.pdf

Simplification of Receiver and PD

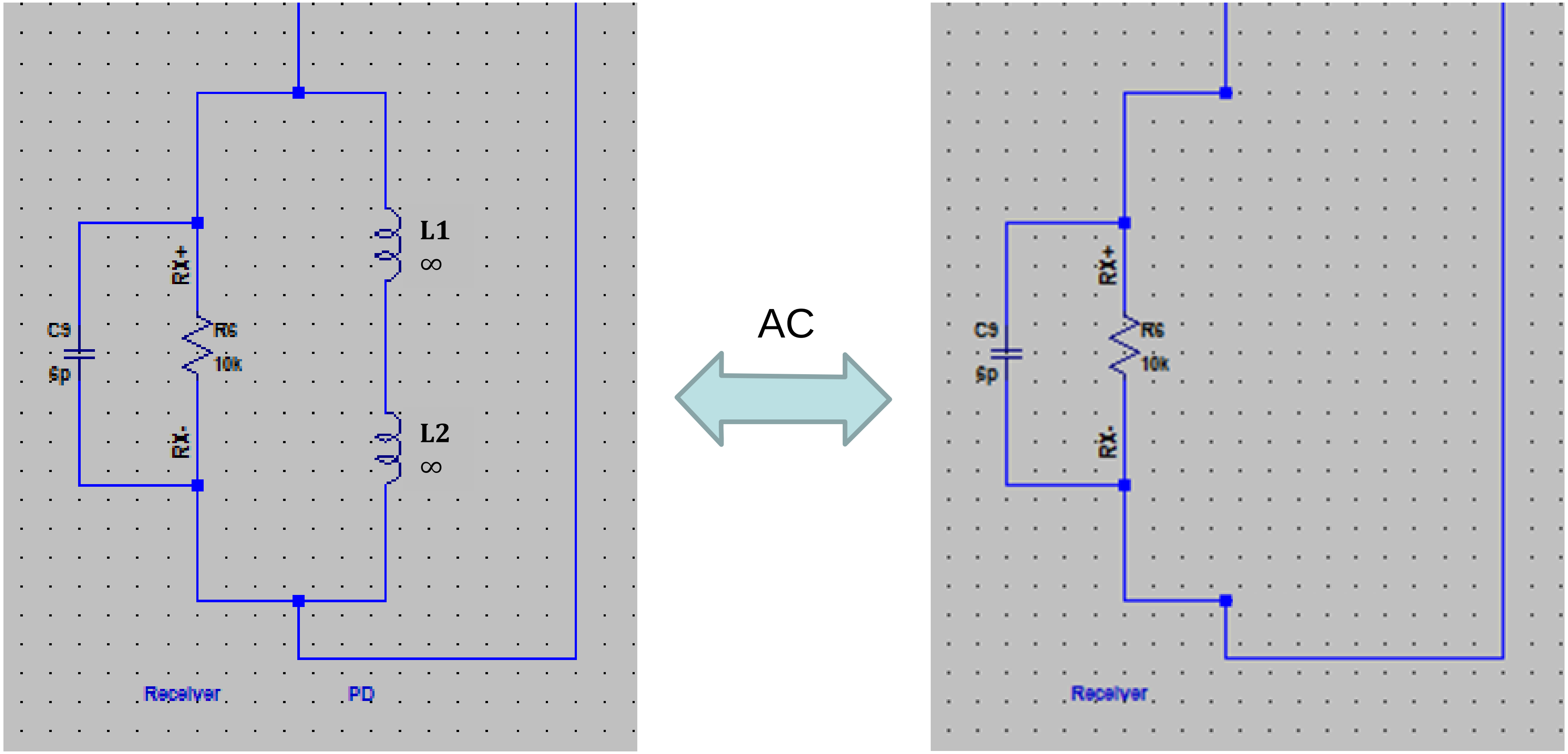






Receiver + PD loads end up looking like RLC across the line

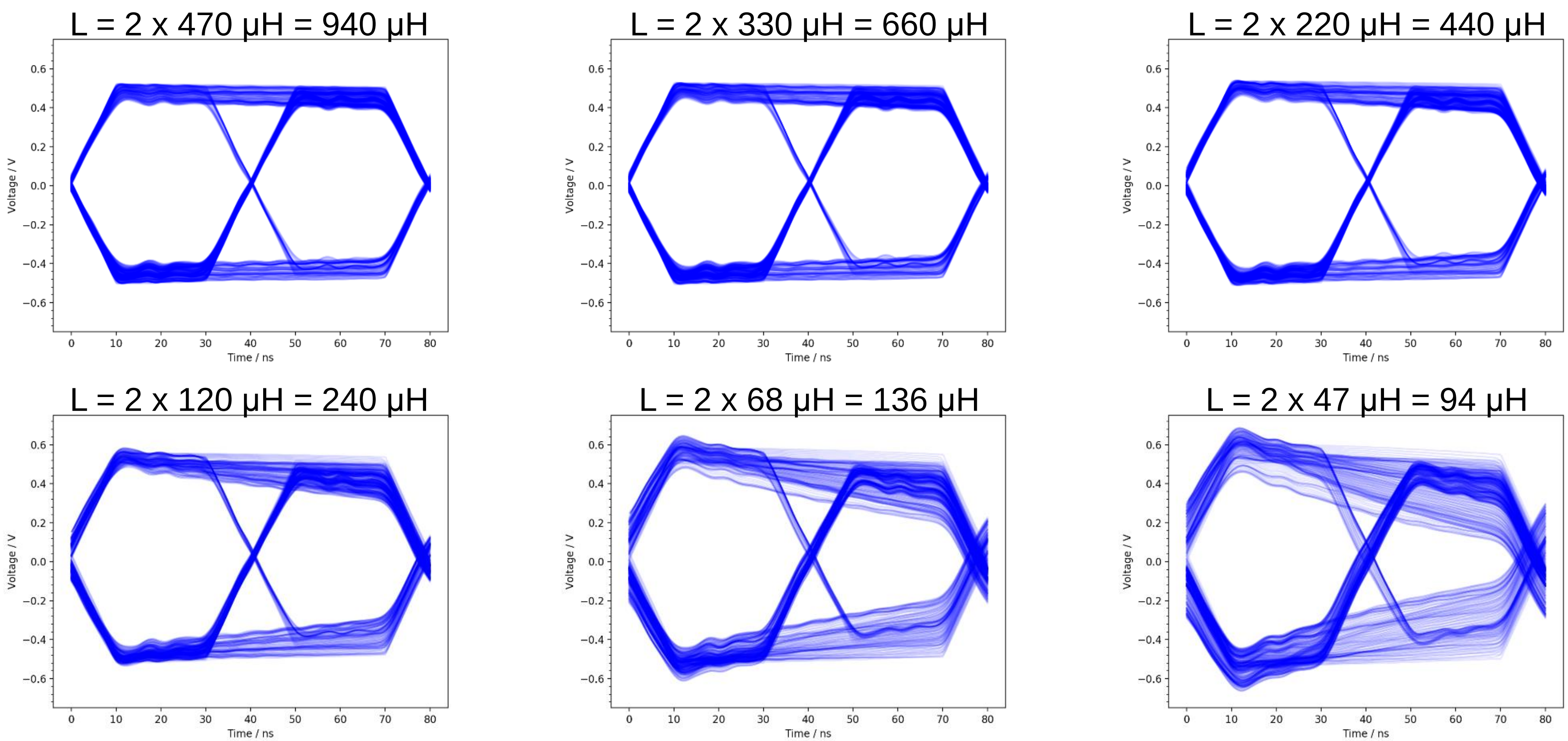
No Inductors Needed Without Data Line Power



Not including inductors is the same as having an infinite inductance at AC frequencies

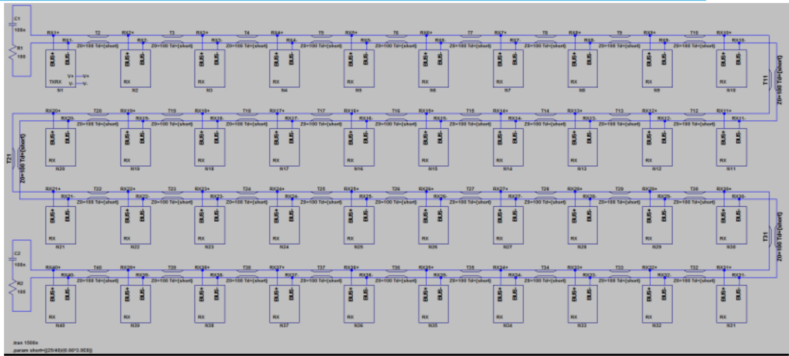
Origin of inductance limits in Draft 2.0

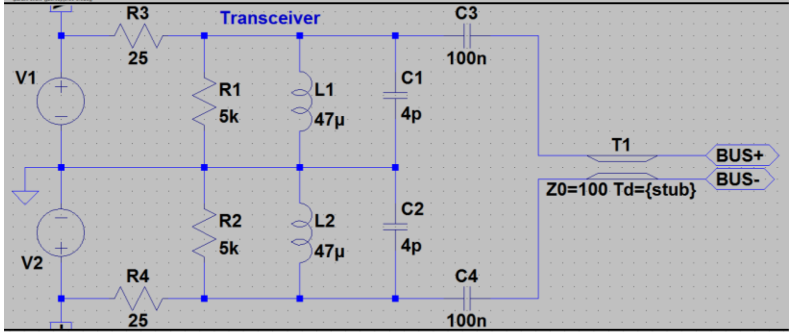
- Limits in Draft 2.0 were derived for a 40 node system
- Inductance impairs the signal as shown below
- Lower inductance values are appropriate (cost effective) for lower node count systems

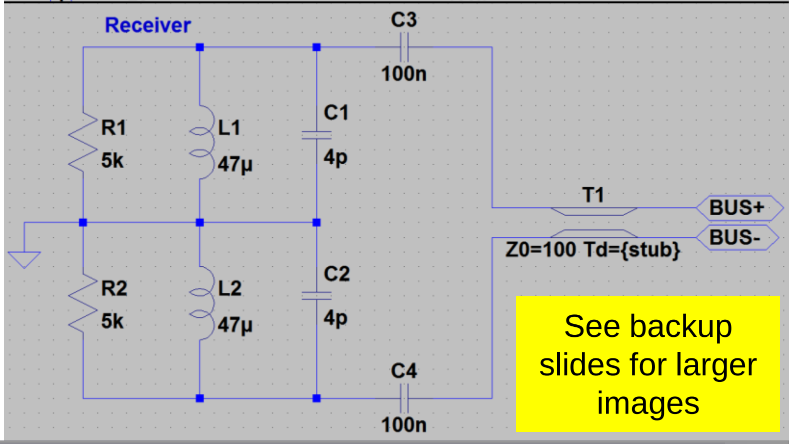


Revisited Time-Domain Simulations to Explore Inductance Range

- LTSpice time-domain simulations to sweep inductance range
- Analogous to capacitance measurements by Piergiorgio and Gian Marco
- Three configurations:
  - Equal node spacing
  - “Clumped” spacing
    - Transmitter at one end of 25 m cable
    - Receivers at other end, separated by 45 mm
  - Approximately equal (random)
    - See backup slides
- Results suggest **80 µH minimum** inductance for an 8 node system





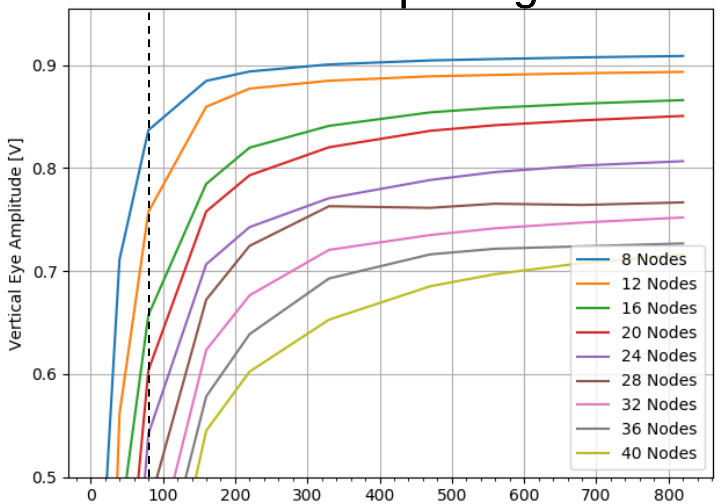


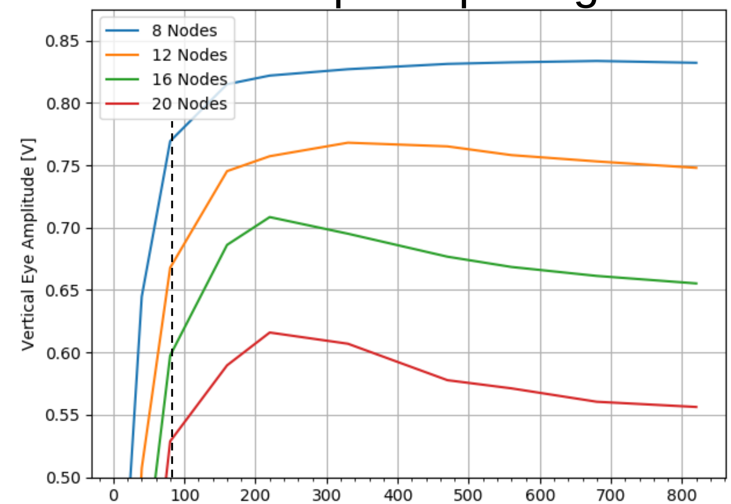
See backup slides for larger images

Eye Opening vs. Inductance

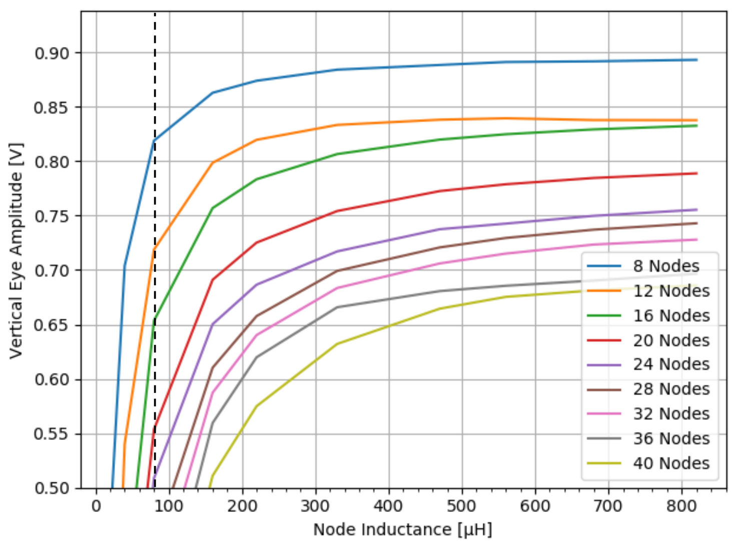
Even Spacing | Clumped Spacing

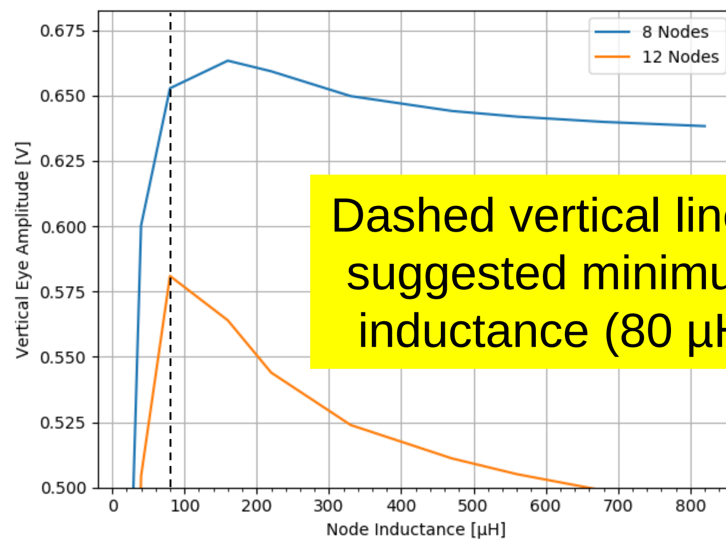
4.5 pF





15 pF





Dashed vertical line = suggested minimum inductance (80 µH)

Conclusions

- A minimum inductance per node limit of 80 µH will ensure an 8-node system will work (regardless of locations of nodes on the bus)
- Inductors are only necessary when using DC power on the data lines (“engineered” power)
  - Not including inductors is equivalent to using an infinite parallel inductance
- Keeping a minimum inductance limit prevents accidentally breaking the system, adds minimal complexity to the draft
  - System **will not work** with small (< 40 µH) node inductances
- Systems with larger node counts will require engineering with more node inductance
- Maximum inductance is set in practice by parasitic capacitance
- Suggest edits (next slide) to Draft 2.0 to clarify the origin of the inductors and to set new inductance limits

Proposed Changes to Draft 2.0

Original text in 147.9.2:

The MDI shall present a minimum parallel impedance across the MDI attachment points based on impedance Equation (147–6) and limits for R, L, Ctot and Cnode over the stated frequency range, where Ctot is the maximum total capacitance across all attachment points, while Cnode is the maximum capacitance for each attachment point.

Revise text in 147.9.2 as follows:

The MDI shall present a minimum parallel impedance across the MDI attachment points based on impedance Equation (147–6) and limits for R, L, Ctot and Cnode <u>given in Table 147-3</u> over the stated frequency range. Ctot is the maximum total capacitance across all <u>MDI</u> attachment points, <u>while R, L, and Cnode are the resistance, inductance, and capacitance</u> for each <u>MDI</u> attachment point.

<u>Inductive elements are only required in the case where power is applied across the data lines. Removing the parallel inductance is equivalent to setting L to infinity in Equation (147-6). The parasitic capacitance of inductive elements forms a portion of Cnode.</u>

Revise Table 147-3 as follows:

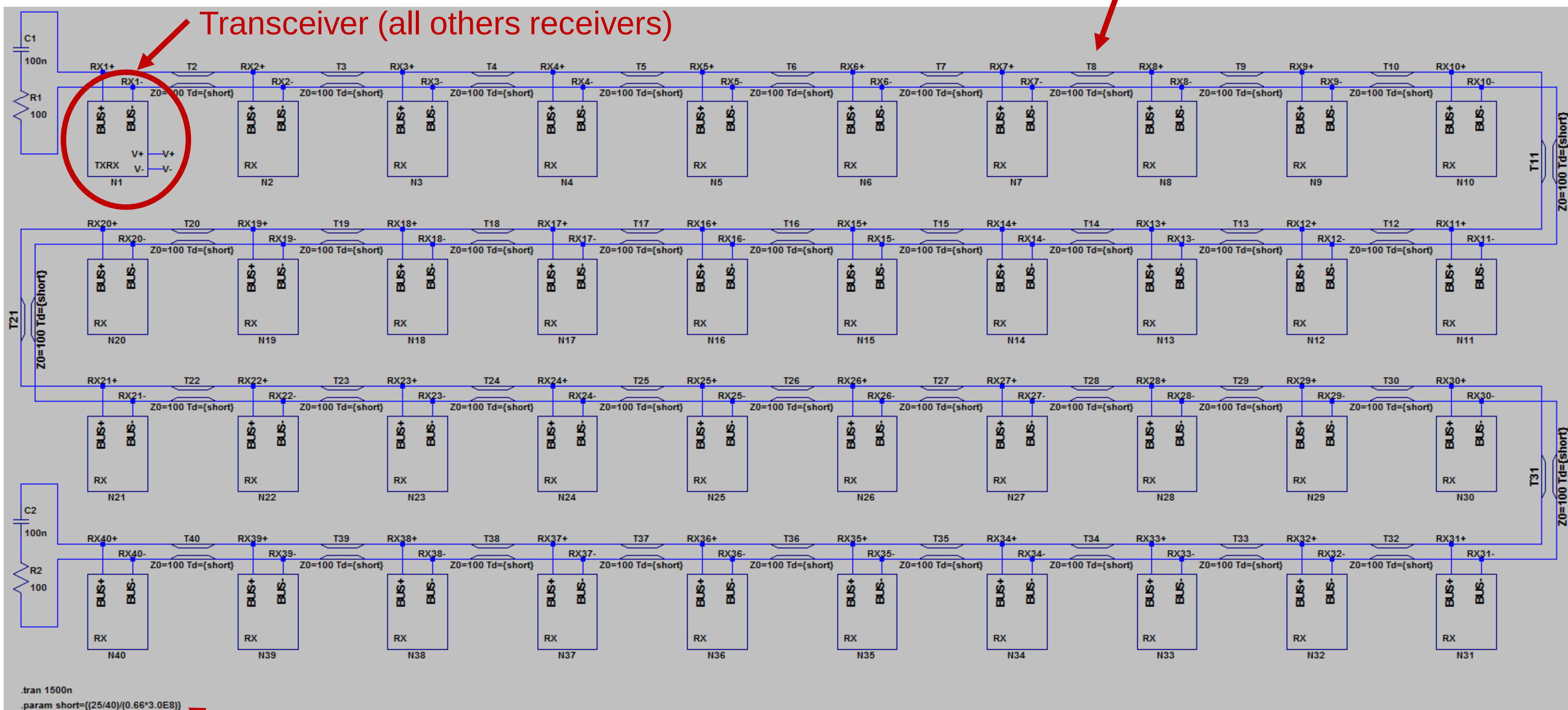
Set the minimum inductance = 80 uH.

Delete the maximum inductance.

Thank you!

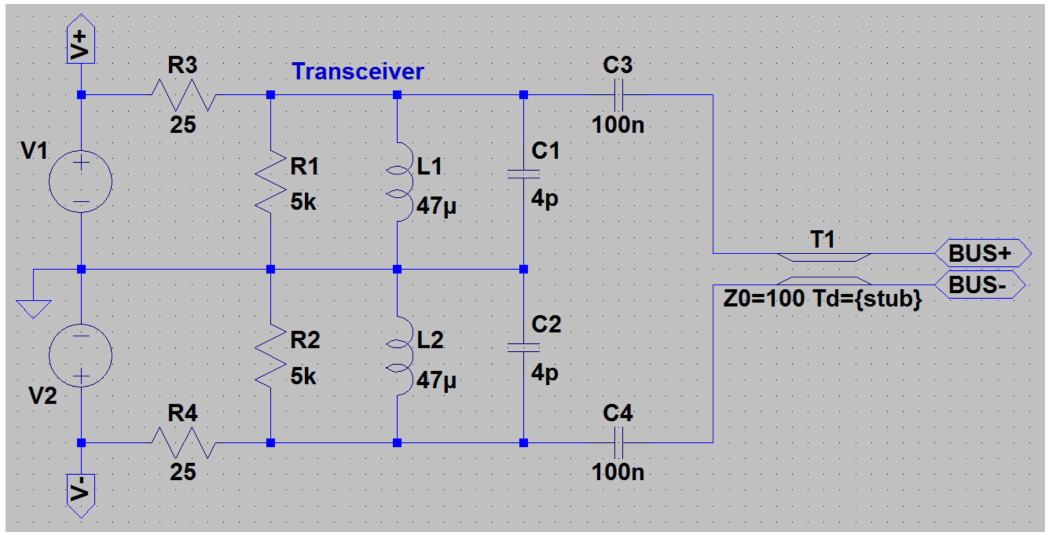
System Model

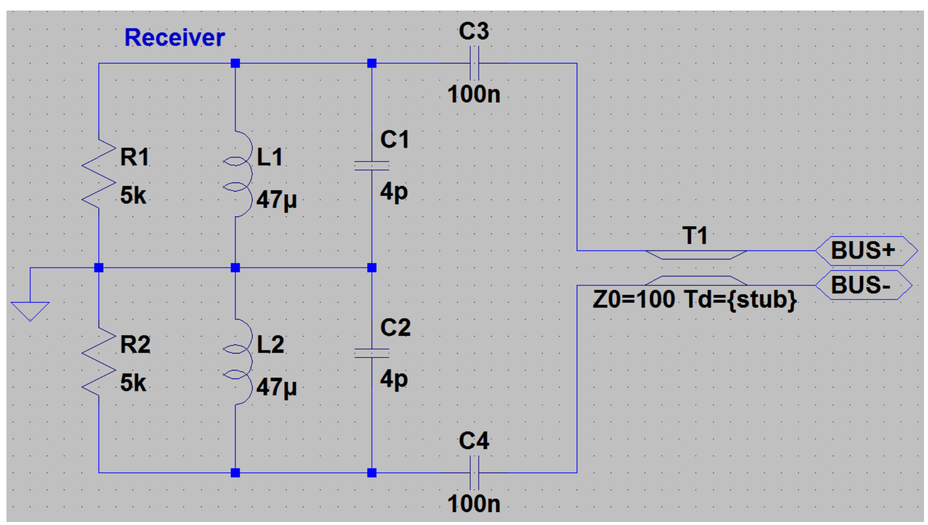
Lossless transmission lines interconnect nodes



Spice Parameters:
transient simulation, 1500 ns duration
transmission lines = 100 Ω impedance, Vp = 0.66 c

Transceiver and receiver models





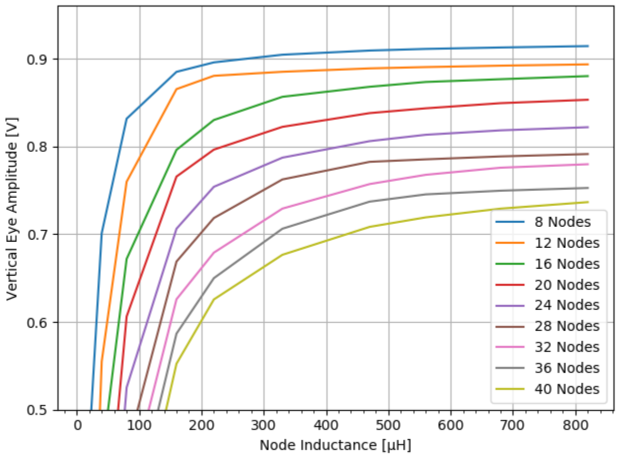
Random Spacing

- Nodes are distributed according to the Dirichlet distribution, with alpha = 2
- The Dirichlet distribution has spacings which are approximately 1/N, where N = number of nodes, and always add up to a given number (total length, 25 meters)
- Larger alpha means closer to 1/N distribution
- Spacing never allowed to be less than 45 mm
- Example node-node spacing for 40 nodes:

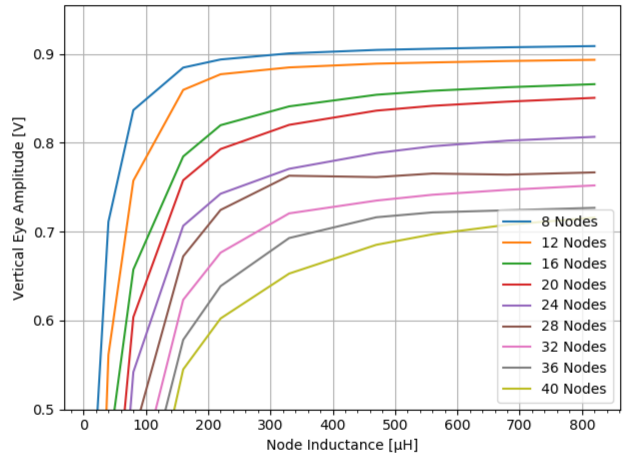
0.09619243, 0.27956314, 1.03099979, 0.38469428, 1.17017827, 0.73485392, 0.78107103, 0.16216035, 0.96522010, 1.22474533,
0.78679250, 0.26906987, 0.49366241, 0.97767188, 0.30975411, 0.71598570, 0.81962640, 0.94305348, 0.40174377, 1.24174782,
0.79793620, 0.32668700, 0.46305764, 0.98382086, 0.30223105, 0.56826058, 0.99469240, 0.61385905, 0.08587518, 0.12292422,
0.15200672, 0.54225893, 0.80276839, 0.25149688, 0.42584166, 0.49894405, 0.60199593, 1.33792044, 1.02471723, 0.31391904

Comparison of Equal and Approximately Equal (Random) Node Spacing

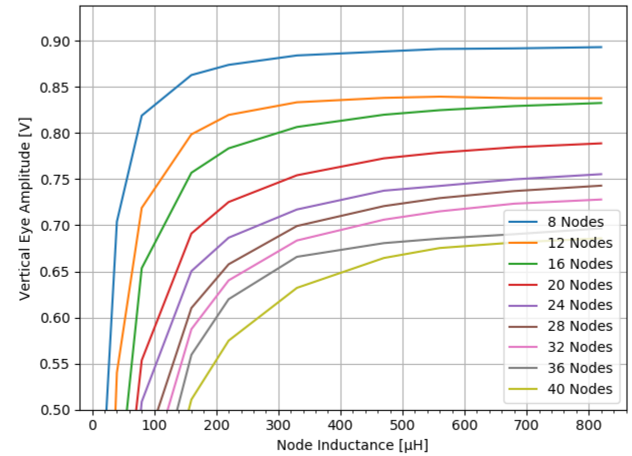
Equal Spacing, C = 2 pF



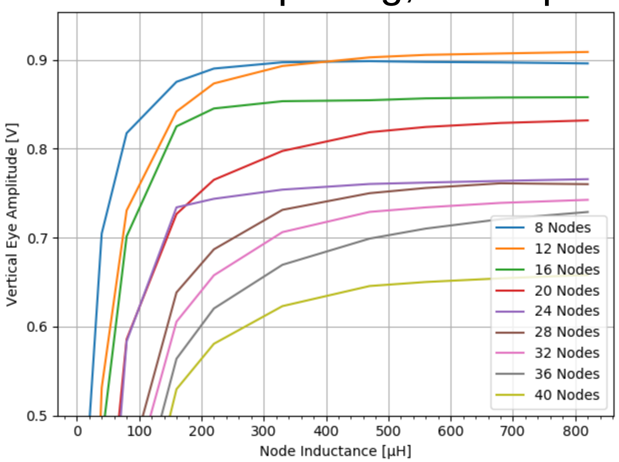
Equal Spacing, C = 4.5 pF



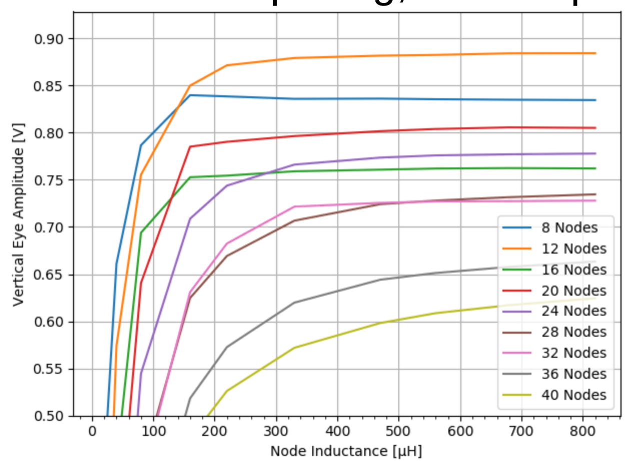
Equal Spacing, C = 15 pF



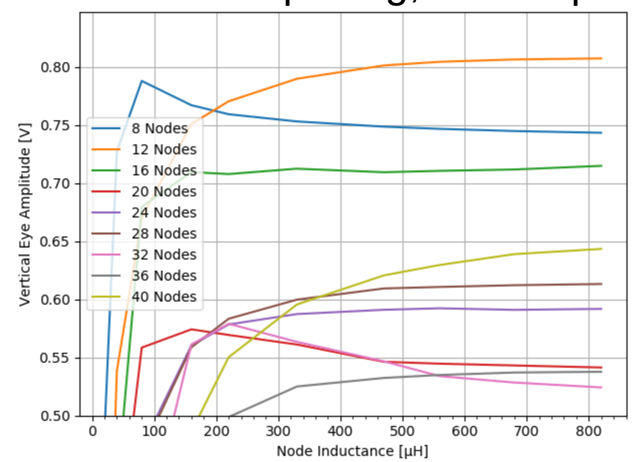
Random Spacing, C = 2 pF



Random Spacing, C = 4.5 pF

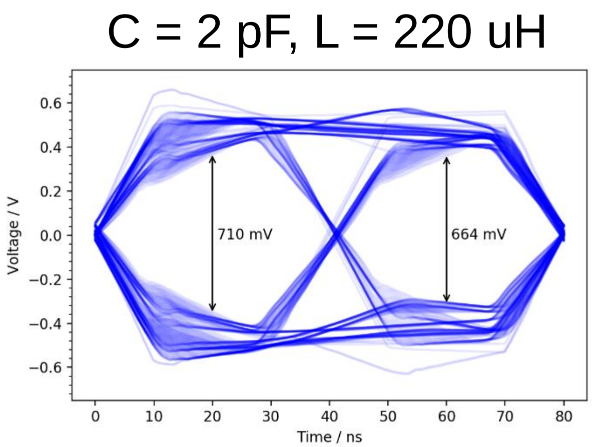


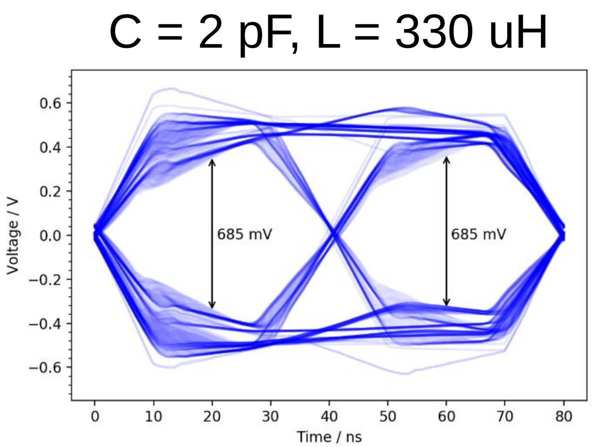
Random Spacing, C = 15 pF

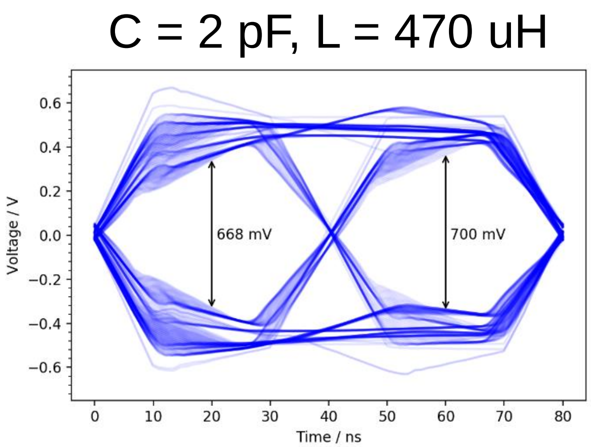


A fair evaluation of random spacing would require multiple (~1000 or more) trials

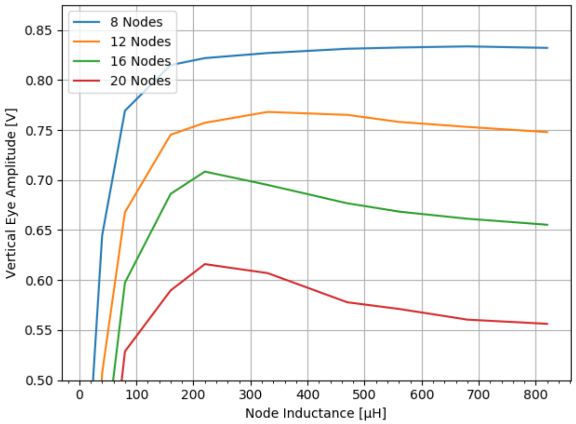
Explanation of Apparent Optimum in Clumped Configuration Results







- For clumped configuration, decrease in eye opening with increasing inductance is a real effect caused by reflection geometry
- Changing the reflection geometry eliminates this effect



- Left Plot: 25 meter cable
- Right Plot: 5 meter cable
- Ideal RLC components
- Results cannot be easily predicted without simulation