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IEEE 802.3cg
Unbalanced PLCA Issue
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Unbalanced PLCA Issue (comment 613)

Contributors

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Introduction

- **PLCA test environment:**
 - 2 Nodes (A and B) with PLCA enabled
 - MACs A and B keep sending back to back
 - **The issue we see:**
 - Sometimes, the pattern is ABB instead AB
 - Results in a 1:2 bandwidth ratio instead 1:1
- unbalanced bandwidth distribution w/ PLCA

Unbalanced Bandwidth

- The pattern we expect to see:

Bus cycle	1		2		3		4		5		6		7		8	
TO	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
Node A	TX	COL	TX	COL	TX	COL	TX	COL	TX	COL	TX	COL	TX	COL	TX	COL
Node B	COL	TX	COL	TX	COL	TX	COL	TX	COL	TX	COL	TX	COL	TX	COL	TX

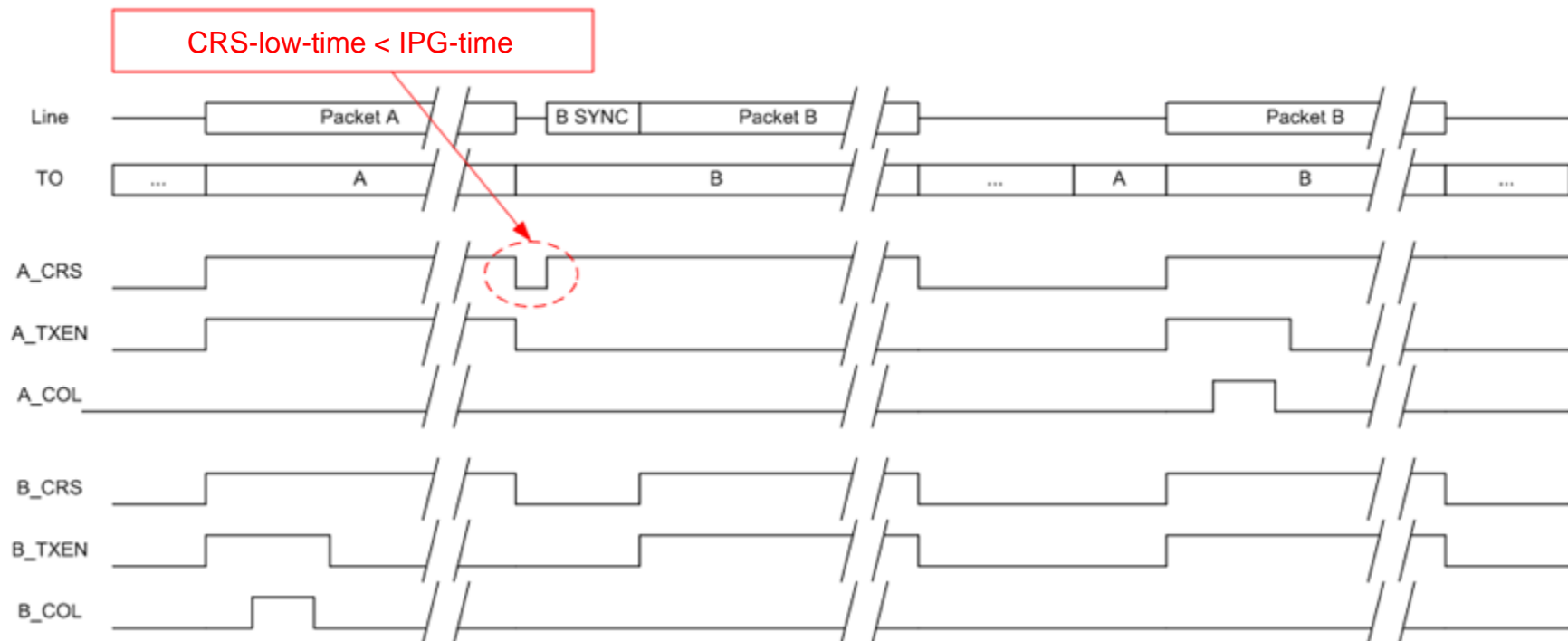
- What we see instead, is:

Bus cycle	1		2		3		4		5		6		7		8	
TO	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
Node A	TX	-	-	COL	TX	-	-	COL	TX	-	-	COL	TX	-	-	COL
Node B	COL	TX	-	TX	COL	TX	-	TX	COL	TX	-	TX	COL	TX	-	TX

→ An unevenly balanced bandwidth distribution like this would render PLCA hardly predictable!

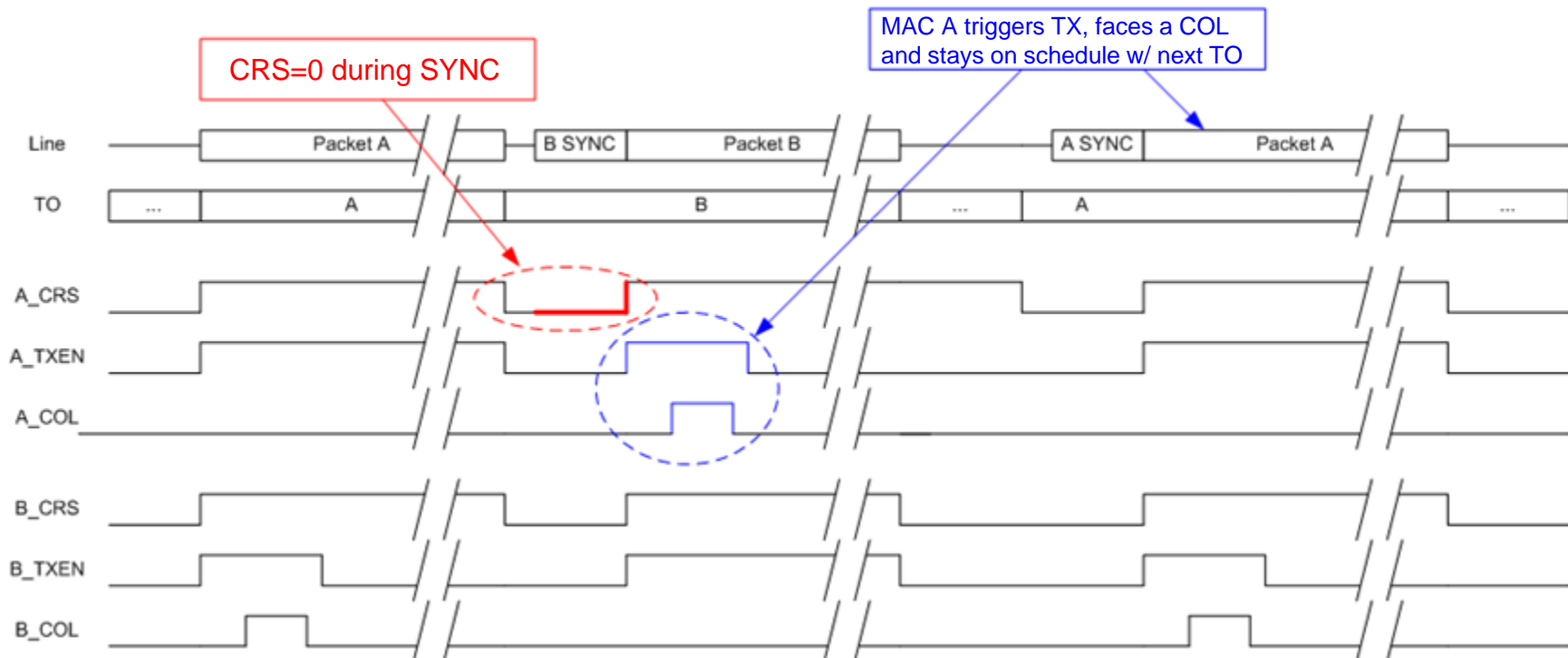
Root Cause

- According to the current spec, PLCA RS will de-assert CRS only for a short time, smaller than the required minimal IPG time
- MAC of node A will not be capable to start transmission of its next pending packet during this period, and may lose its next TO



Proposal

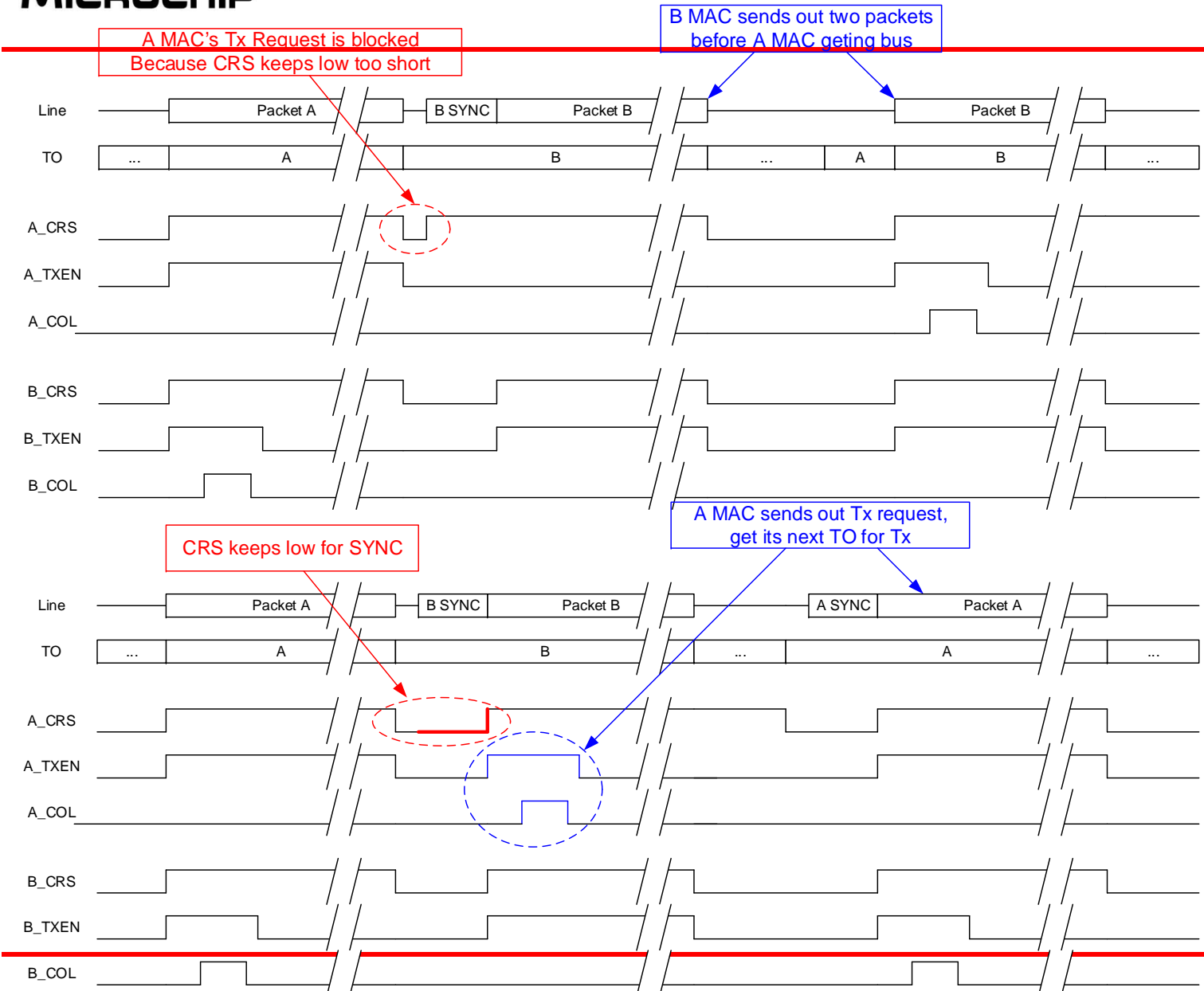
- Always de-assert CRS between two adjacent packets for at least the min. IPG time
- We can achieve this by keeping CRS de-asserted also during the PLCA SYNC period





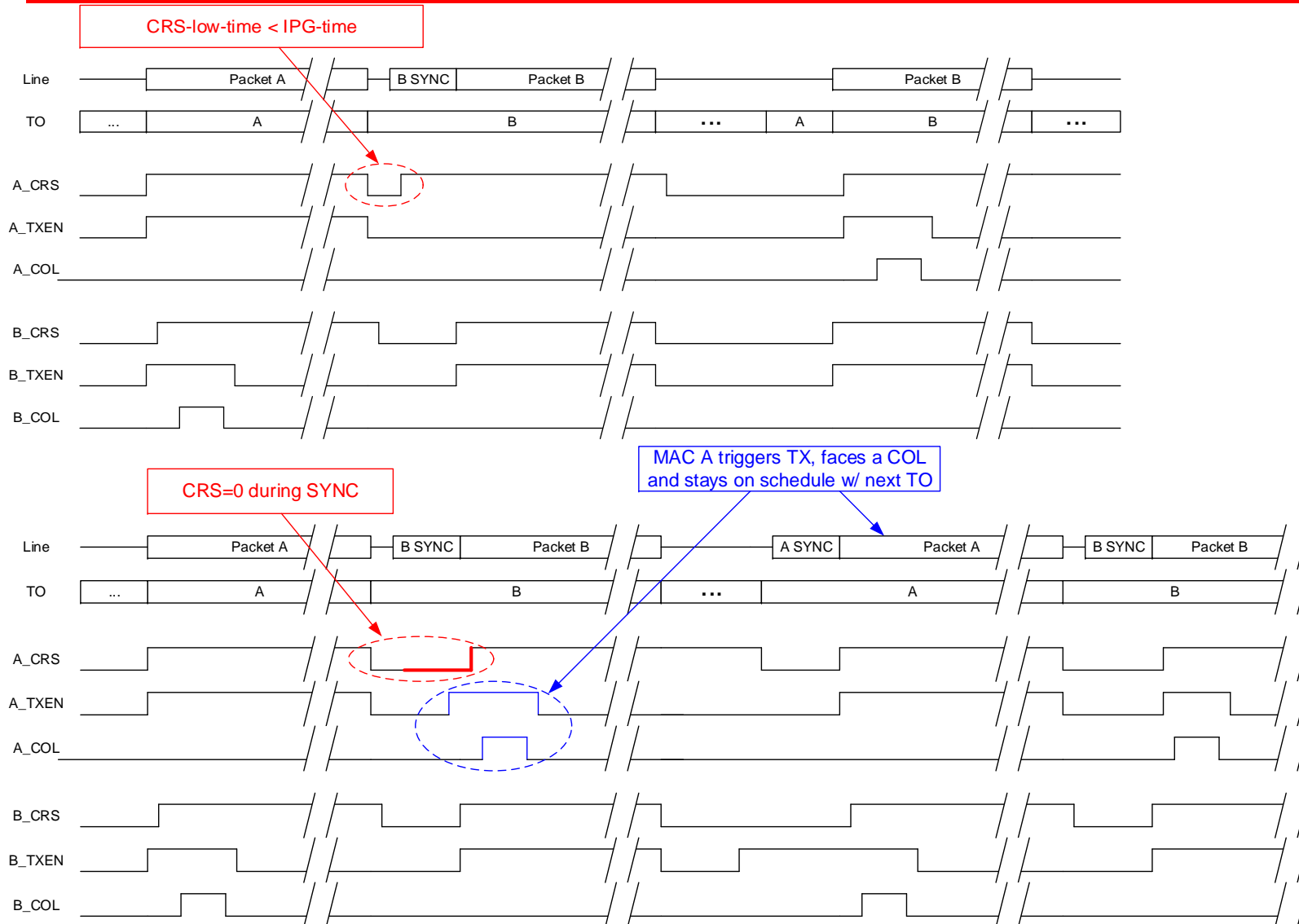
Picture w/o cable delay

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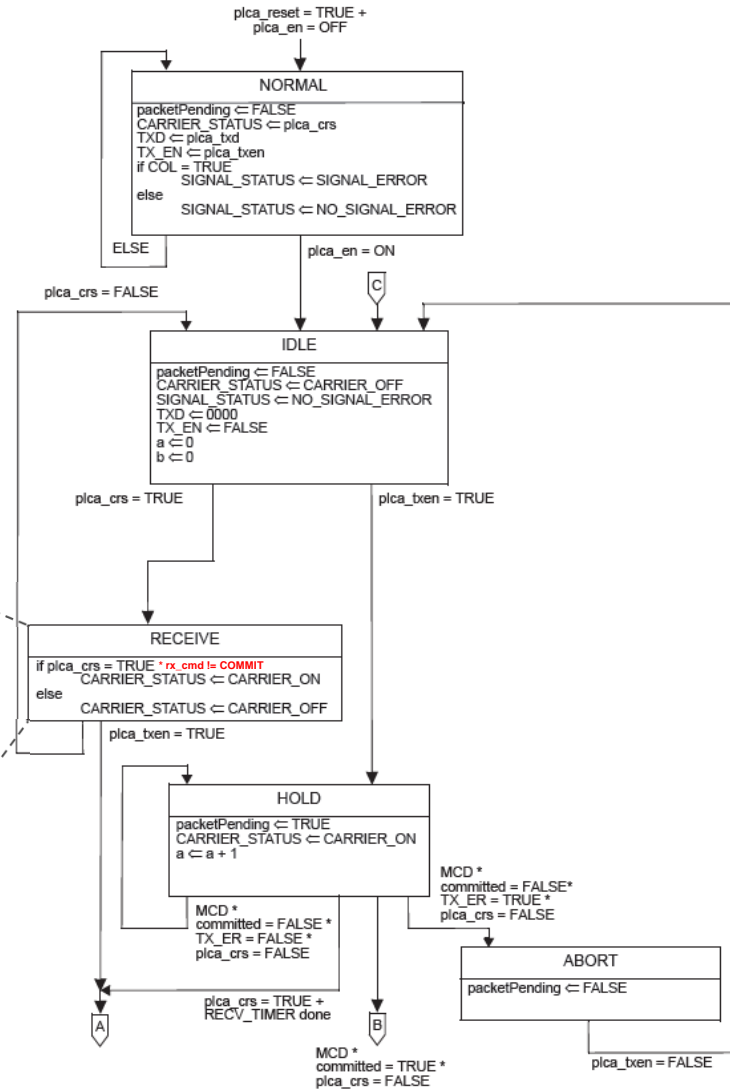
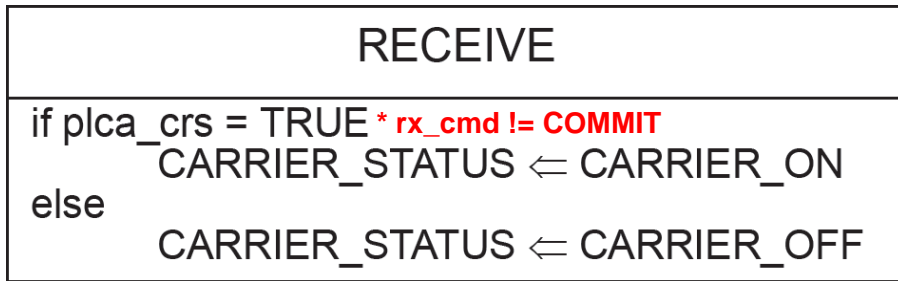
Picture with cable delays





Resulting Spec Change

- In Figure 148-6 (IEEE Draft P802.3cg/D2.0)
 - Change “if *plca_crs* = TRUE”
 - to “if *plca_crs* = TRUE * *rx_cmd* != COMMIT”



Conclusion

- **We were able to validate that the proposed solution will fix the unbalanced behavior of PLCA**
- **This issue was also seen by Canova Tech and they agreed on the proposed spec change**



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Thank You!

