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IEEE802.3cg TF

Short Reach PCS, PMA and PLCA baseline proposal

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- PMA
  - Adoption of DME
  - Definition of primitives
- PCS
  - Adoption of 4b5b coding
  - Adoption of TX state machine
  - Adoption of RX state machine
  - Adoption of MII clause 22
- PLCA
  - Adoption of state machines
  - Definition as optional reconciliation sublayer

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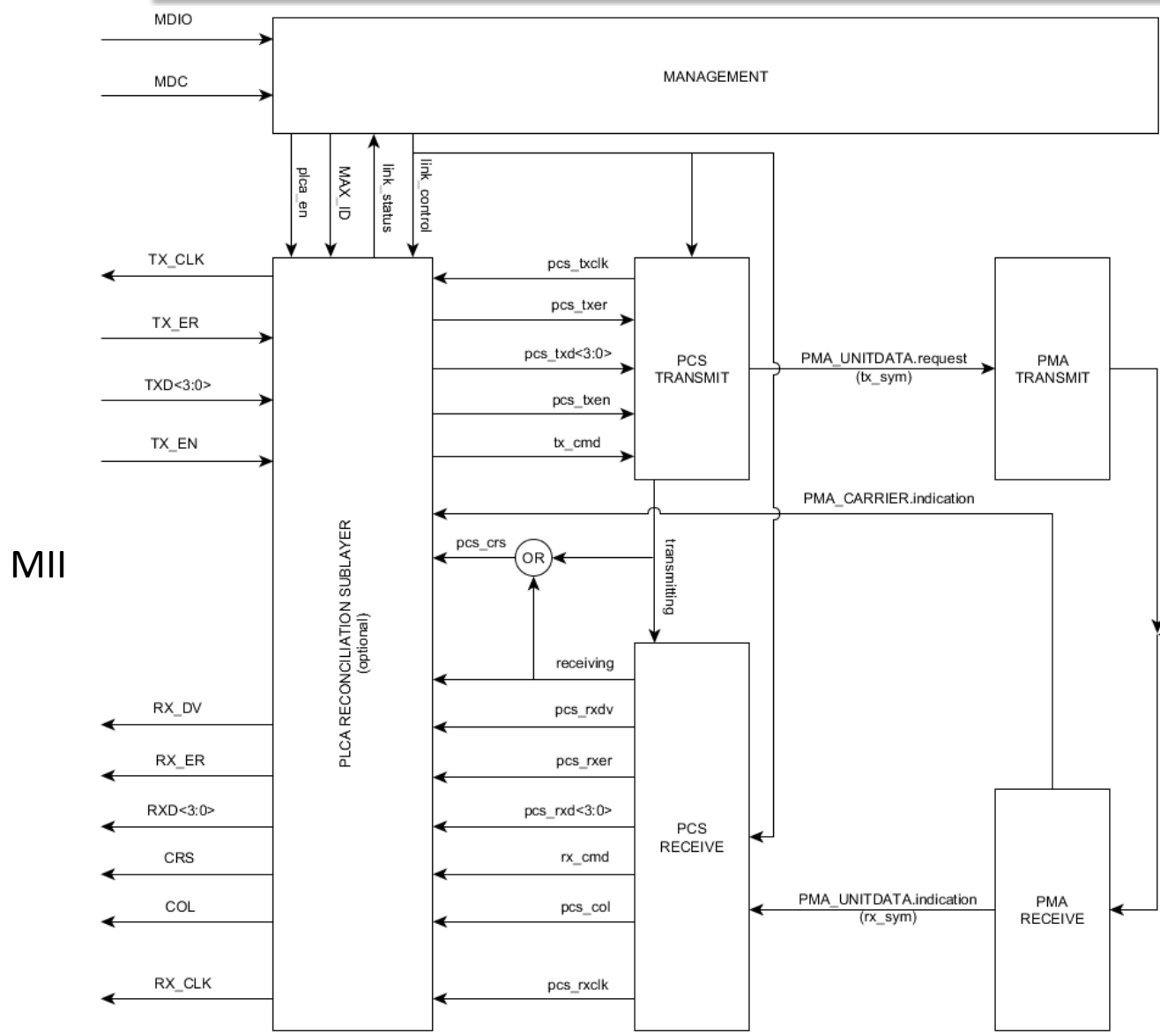
PCS functions converts MII data to 4B/5B encoded symbols for the PMA to serialize into a DME encoded voltage levels

PLCA is an optionally enabled feature for the short reach use case which improves performance over a multidrop network.

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When PLCA is not enabled/implemented the PCS functions maps directly to the homonymous MII signals, and the system reverts to a standard CSMA/CD compliant PHY.

PMA

Line Coding
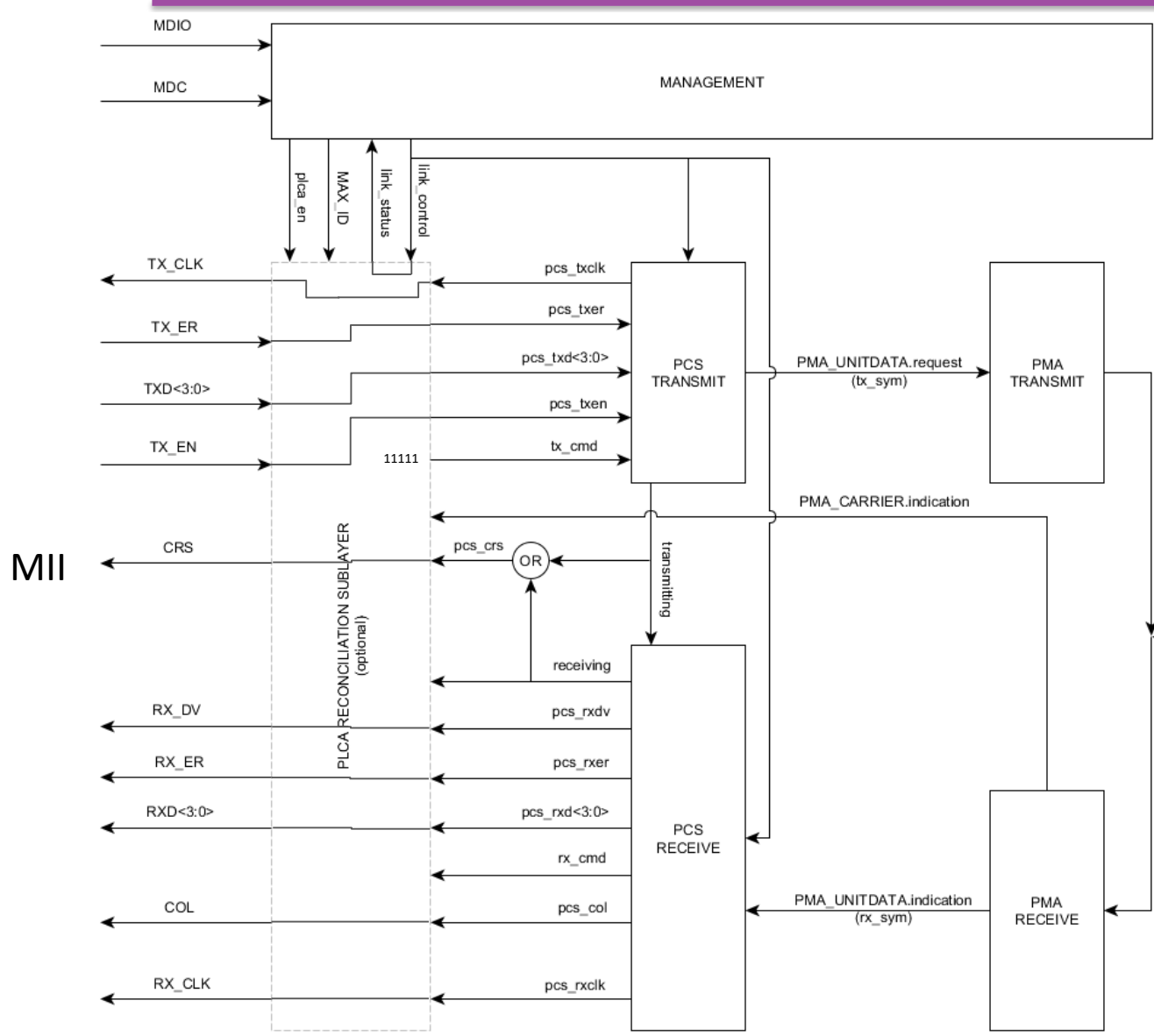
- 5B data is serialized <u>LSB first</u> and encoded using DME as in figure 98-4 and 98-5 of 802.3bp with the exception of timings
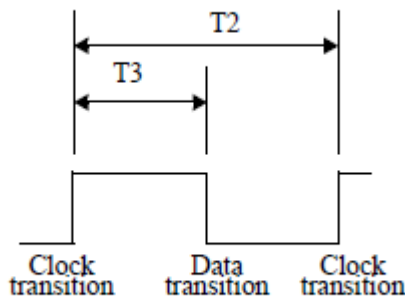

Figure 98–5—DME page transition timing

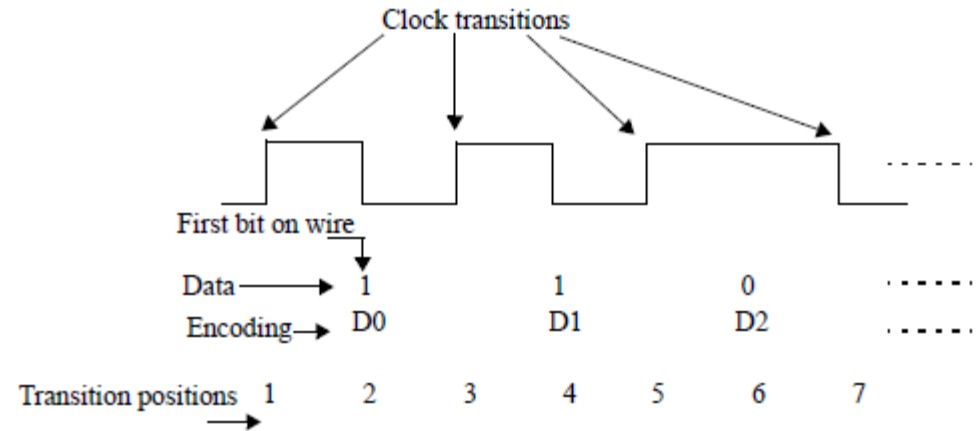
Figure 98–4—Data bit encoding within DME pages

	Parameters	Min	Typ	Max	Units
T2	Clock transition to clock transition		80		ns
T3	Clock transition to data transition (data = 1)		40		ns

- Transmitter Baud Rate tolerance shall be $\pm$ 100ppm of nominal frequency (see T2 and T3)

- Transmitter peak differential output:
  - When measured with 100 Ω termination, transmit differential signal at MDI shall be within range of 1 V $\pm$ 30% peak-to-peak

- DME reception:
  - To be able to detect the DME bits, the receiver should have the capability to receive DME signals sent with the electrical specifications of the PHY.

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- During transmission, PMA_UNITDATA.request conveys to the PMA using tx_sym the value of the 5B symbol to be sent over the single transmit pair using Differential Manchester Encoding (DME). A signal transmitter is used to generate the DME signal on the wire using the transmit clock TX_TCLK (25 MHz). The PMA Transmit Function derives the TX_TCLK from a local clock source.

- When the 5B symbol 'I' (11111) which represent SILENCE is conveyed to the PMA through the PMA_UNITDATA.request primitive, the PMD shall be put in a high impedance state within 1 bit time.

- When any other 5B symbol is conveyed via the same primitive, the PMA TX function shall signal the PMD to drive the line at least 0.5 bit time prior to transmitting the first DME encoded bit.

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- The PMA Receive function comprises a single receiver for DME modulated signals on a single balanced pair. PMA Receive has the ability to translate the received signals on the single pair into the PMA_UNITDATA.indication parameter rx_sym. It detects 5B symbol sequences from the signals received at the MDI and presents these sequences to the PCS Receive function.

- When no signals are received from the MDI, or the PMA Receive function is not yet aligned to the 5b symbol boundary, the rx_sym parameter is set to the 5b 'I' symbol (5'b11111). The PMA Receive has the ability to align the received symbols stream to a 5b sequence of 'JJ' or 'NN'

- The parameter PMA_CARRIER.indication is generated by PMA Receive to indicate the status of the receive carrier at the local PHY. This variable indicates whether the receive PMA function is synchronized to the DME modulated bit stream. This primitive is only used by PLCA optional reconciliation sublayer, thus it's not required when PLCA is not implemented.

PCS

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Name	4b	5b	Name	4b	5b	Special Function
0	0000	11110	I	-	11111	SILENCE
1	0001	01001	J	-	11000	SYNC
2	0010	10100	K	-	10001	SSD
3	0011	10101	T	-	01101	ESD
4	0100	01010	R	-	00111	ESDOK
5	0101	01011	H	-	00100	ESD
6	0110	01110	N	-	01000	BEACON
7	0111	01111				
8	1000	10010				
9	1001	10011				
A	1010	10110				
B	1011	10111				
C	1100	11010				
D	1101	11011				
E	1110	11100				
F	1111	11101				

CODES REPRESENTING VALID 4B DATA   **CODES USED FOR SIGNALING**

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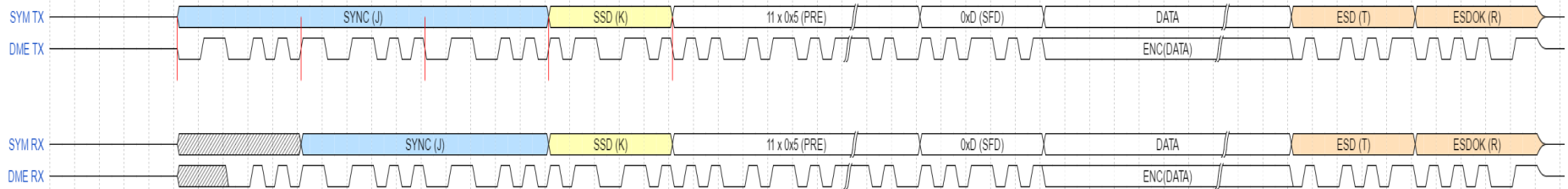
- PCS TX function replaces the first four 5B-encoded nibbles of packet preamble with the following symbol sequence, to allow receiver synchronization:
  - J, J, J, K (00011 00011 00011 10001)
- PCS TX function then inserts 5B encoded MII data followed by ESD and either ESDOK or EDERR symbols depending on TX_ERR state during packet transmission
- PMA RX exploits the first three '0' DME bits of the first 'J' symbol to synchronize on DME stream, then uses the following two 'J' symbols to align on 5B boundary
- PCS RX detects the 'JK' sequence to regenerate at the proper point in time the packet preamble conveyed to MII, along with the packet data following the SFD.
- RX_ER is regenerated from ESD sequence accordingly
- Pretty similar to what PCS functions do in 802.3bw (100base-T1 PHY).
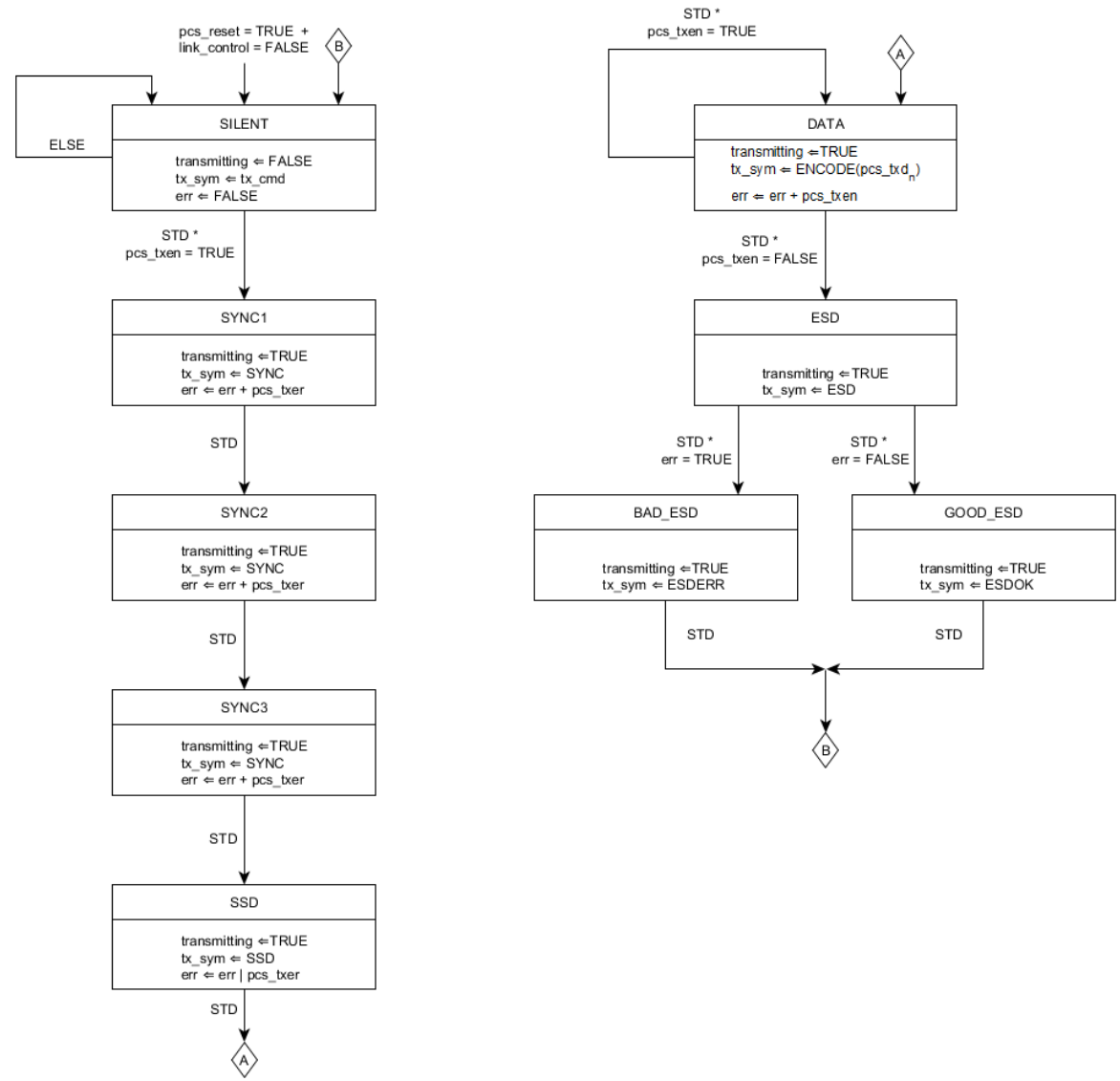
- **pcs_reset**: The pcs_reset parameter set by the PCS Reset function.
  - Value: ON or OFF
- **pcs_txen**: The TX_EN signal of the MII as specified in .. When optional PLCA is enabled, this signal is generated as specified in .. When set to FALSE transmission is disabled. When set to TRUE transmission is enabled.
  - Value TRUE or FALSE
- **pcs_txer**: The TX_ER signal of the MII as specified in .. When optional PLCA is enabled, this signal is generated as specified in .. When set to FALSE it indicates a non-errored transmission. When set to TRUE it indicates an errored transmission
  - Value: TRUE or FALSE
- **pcs_txd**: The TXD signal of the MII as specified in .. When optional PLCA is enabled, this signal is generated as specified in .. The signal represent a 4B nibble to transmit
- **tx_cmd**: a 5B symbol generated in . . . to perform optional PLCA functionality. When PLCA optional reconciliation sublayer is not implemented, tx_cmd shall be set to SILENCE, that is the 5B symbol 'I' (11111).
- **tx_sym**: a 5B symbol to transmit, generated from the 4B data or directly passed from tx_cmd according to ..

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- **transmitting**: the transmitting variable is set in the PCS data transmission as defined in figure… When this variable is set to TRUE it indicates a transmission is ongoing.

  — Value: TRUE or FALSE

- **err**: the err variable is set in the PCS data transmission as defined in figure… This variable is used to detect a pcs_txer during transmission; if such error is detected, a ESDERR symbol is sent at the end of transmission

  — Value: TRUE or FALSE

- **SYNC**: five bit symbol defined as 'J' in 4b/5b encoding

- **ESD**: five bit symbol defined as 'T' in 4b/5b encoding

- **ESDERR**: five bit symbol defined as 'H' in 4b/5b encoding

- **ESDOK**: five bit symbol defined as 'R' in 4b/5b encoding

- **ENCODE**: in the PCS transmit process, this function takes as its arguments the pcs_txd 4b data and returns the corresponding 5b symbol as defined in . . .
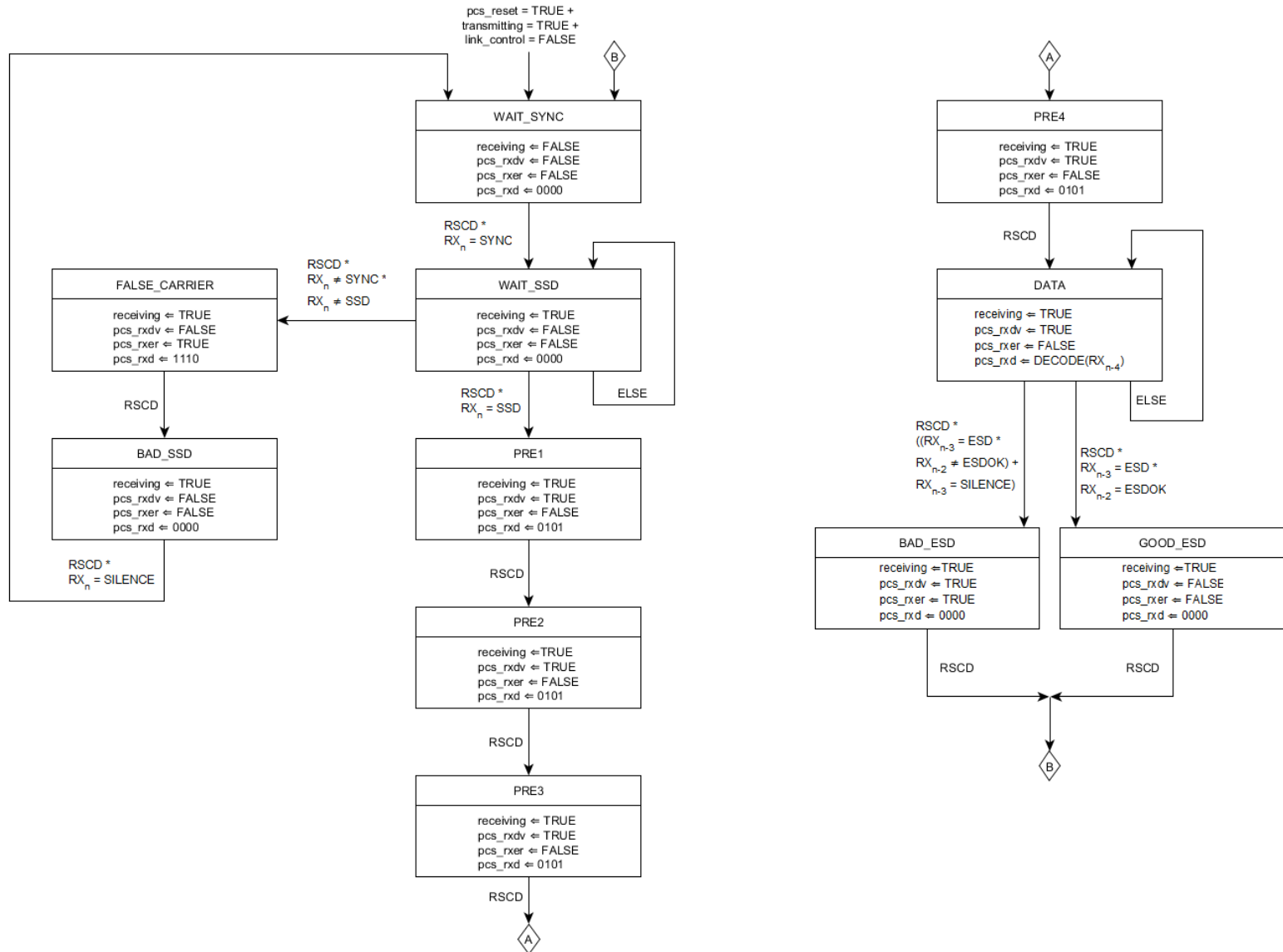
- STD: alias for symbol timer done, synchronous to PCS TX clock

- **pcs_reset**: The pcs_reset parameter set by the PCS Reset function.
  - Value: ON or OFF
- **receiving**: the receiving variable is set in the PCS data receive as defined in figure… When this variable is set to TRUE it indicates a receive is ongoing.
  - Value: TRUE or FALSE
- **pcs_rxdv**: The RX_DV signal of the MII as specified in 22.2.2.7.
- **pcs_rxer**: The RX_ER signal of the MII as specified in 22.2.2.10.
- **pcs_rxd**: PCS decoded data synchronous to RX_CLK.
- **RXn**: Received 5b symbol generated by PMA receive at time n
- **SYNC**: A five bit symbol defined as 'J' in 4b/5b encoding
- **ESD**: A five bit symbol defined as 'T' in 4b/5b encoding
- **ESDOK**: A five bit symbol defined as 'R' in 4b/5b encoding
- **SSD**: A five bit symbol defined as 'K' in 4b/5b encoding
- **SILENCE**: A five bit symbol defined as 'I' in 4b/5b encoding

- **DECODE**: in the PCS receive process, this function takes as its arguments the RXn 5b symbol and returns the corresponding 4b data as defined in ...
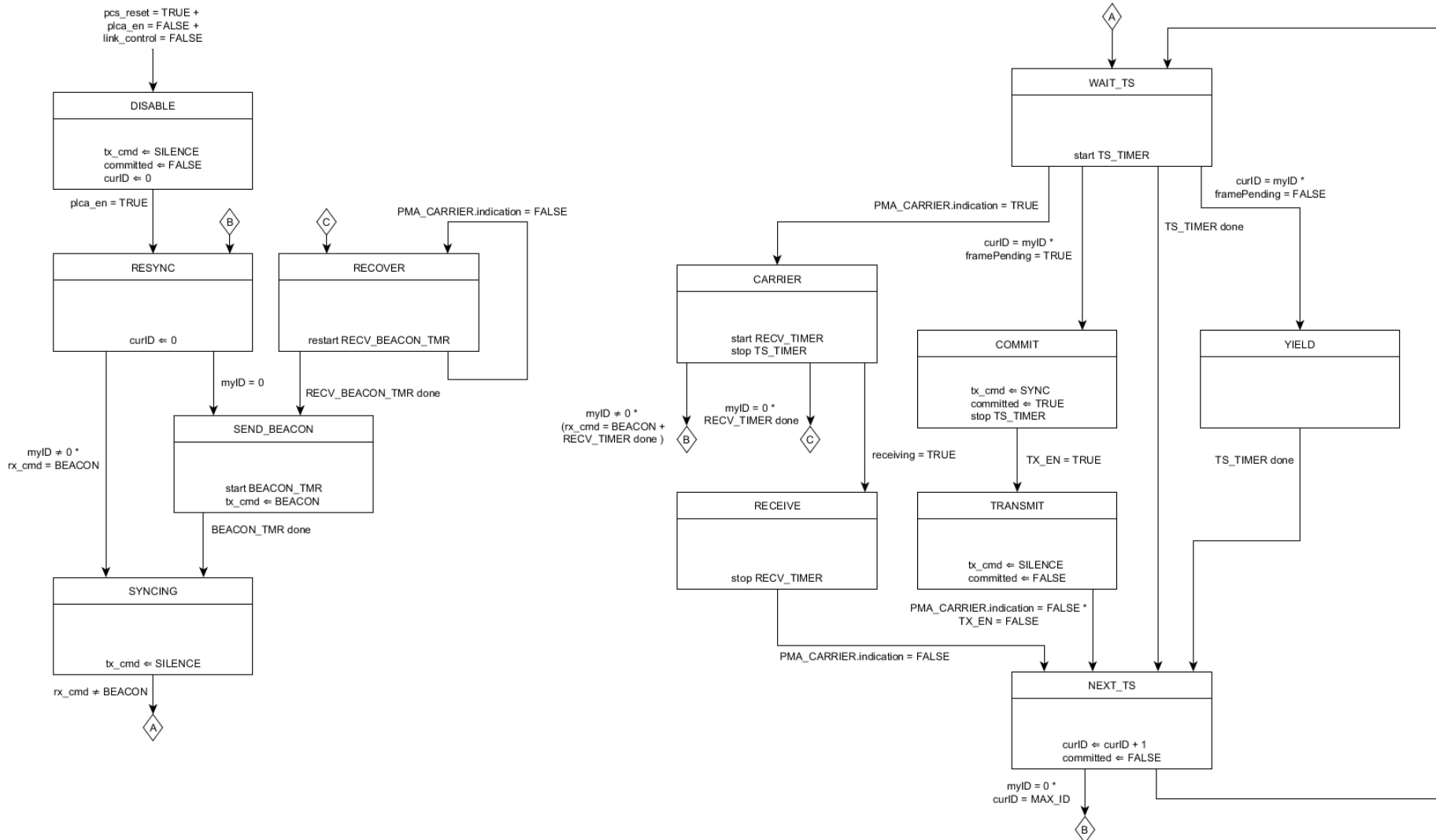
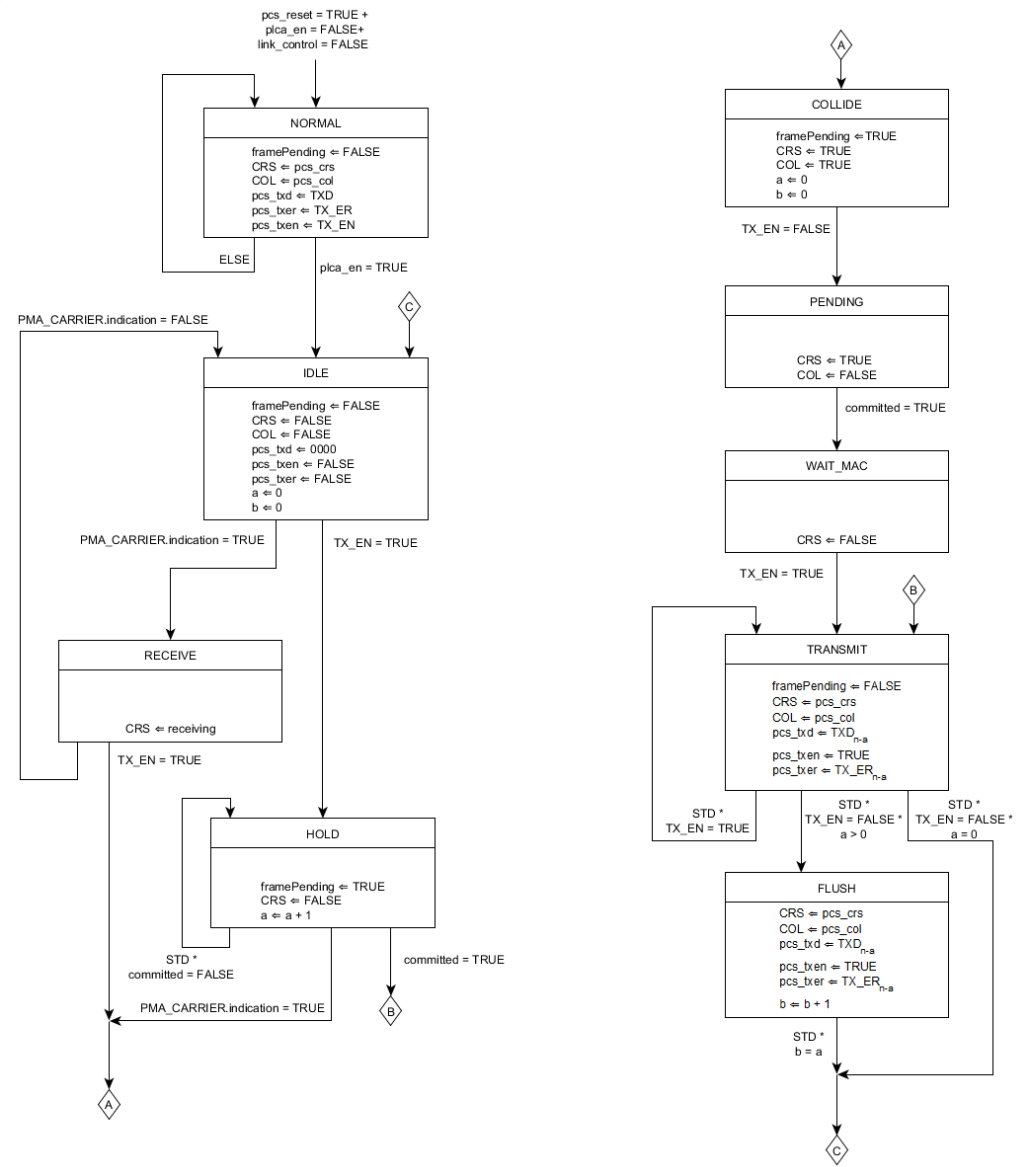- **RSCD**: alias for Receive Symbol Conversion Done

PLCA

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- **plca_en**: generated by management interface, enables PLCA functions. When set to FALSE the TX functions revert to standard CSMA/CD.
  - Value: TRUE or FALSE

- **link_control**: generated by management interface, enables PCS TX and RX functions. When set to FALSE MII data from MAC is discarded and receiver functions are disabled.
  - Value: TRUE or FALSE

- **link_status**: generated by PLCA reconciliation sublayer, informs the management interface that the PHY is ready to send/receive data via MII interface.
  When PLCA function is not enabled/implemented link_status shall be continuously assigned to the link_control current value.
  - Value: TRUE or FALSE

- **myID:** generated by the management interface, represents the PLCA time slot ID assigned to the PHY. Special value '0' is assigned to the master node, indicating the PHY shall generate BEACON signals as described in ...
  - Value: integer value from 0 (master) to MAX_ID

- **MAX_ID:** generated by the management interface, indicates the number of time slots to be allocated, that is the maximum number of PHYs that can join the multidrop network. This parameter is only meaningful for the master PHY (myID = 0), for slave PHYs is a don't care.
  - Value: integer number from 0 to implementation defined value

- **committed:** internal variable used to synchronize PLCA processes as depicted in ...
  - Value: TRUE or FALSE

- **framePending:** internal variable used to synchronize PLCA processes as depicted in ...
  - Value: TRUE or FALSE

- **BEACON_TIMER**: represents the time for which the master PHY signals a BEACON condition on the line when a PLCA cycle starts. It shall be set to 20 BT to allow the slave PHYs to properly recover the signal.

- **RECV_TIMER**: the time a PHY waits after PMA detects a carrier on the line (i.e. it is aligned at least on DME bit stream as described in ...) and the PCS RX actually achieves synchronization. The purpose of this timer is to allow early detection of carrier on the line to minimize time slot skew (see ...) allowing smaller time slots (see TS_TIMER) and increased efficiency. In presence of false carrier events, this timer expires and triggers a recovery function as described in ... (slave PHY waits for a new BEACON while master PHY waits for all slaves to be silent before sending a new BEACON). Timer value is implementation defined but shall be greater than PHY total RX latency including PMD, PMA and PCS RX.

- **TS_TIMER**: this is the time slot timer, as defined in (...). It shall be set according to maximum allowed PHY TX and RX latencies and maximum MDI to MDI propagation delay, as reported in (...).
For a 25m cable and 10BT of total RX+TX latency a safe default value is 20BT (see ...).

- **RECV_BEACON_TIMER:** during a recovery operation (see ...) the master PHY needs to wait for all slave PHYs to be silent before sending a new BEACON.
This timer value shall be set at least to TS_TIMER * (MAX_ID + 1) for safe operations.

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Thank You !

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