10 Mb/s Single Twisted Pair Ethernet

10BASE-T1L LPI Refresh Synchronization

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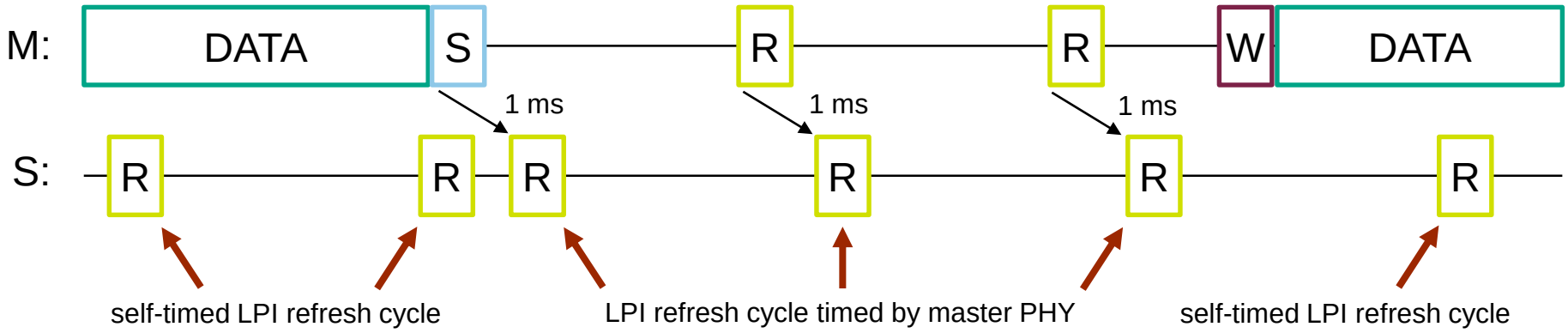
LPI Refresh Synchronization

- An assymetric LPI scheme is used for 10BASE-T1L, **currently without any synchronization** of the timing between both PHYs.
- The intention of this presentation is to **show an idea on how the LPI timing of the slave PHY can be synchronized** to the master PHY LPI timing, to prevent a (partial) overlapping of the refresh cycles.
- While in LPI mode, the master PHY is always timing its quiet/refresh cycle on its own.
- As long as the slave PHY is the only PHY in LPI mode, also the slave PHY is timing its quiet/refresh cycle on its own.
- As soon as master and slave PHY are both in LPI mode, the slave PHYs LPI cycle is synchronized with the master PHYs LPI cycle.
- This is done using an additional state machine for detecting the LPI refresh cycle from the master PHY.
- Each time an LPI sleep or refresh cycle of the master PHY is detected by the slave PHY a timer (lpi_sync_timer) is started and used instead of the lpi_quiet_timer to time the quiet phase.
- An LPI refresh cycle from the master PHY is detected by evaluating the check_idle function (a PHY is reliably receiving idle telegrams, which is only the case, if the PHY is actively receiving idle data from the far end PHY) in combination with the lpi_rx_active variable, which is true, if the far end PHY is in LPI mode.

LPI Refresh Synchronization

- The lpi_sync_timer (1 ms) is significantly shorter than the lpi_quiet_timer (6 ms) and used to synchronize the slave PHYs LPI timing with the master PHYs timing.
- If both PHYs are in LPI mode, then the slave PHY will start to transmit its refresh cycle approx. 1 ms after the master PHY has started to transmit a refresh cycle.
- Therefore after the first sleep cycle has been sent (which cannot be synchronized, so there may be an overlapping, as one PHY is exiting from normal operation into LPI mode), the slave PHYs LPI cycle will be in sync with the masters PHY LPI cycle.
- If the master PHY goes out of LPI mode, then the slave PHY will time its LPI cycle on its own again.
- The master PHY timing always is constant, for the slave PHY timing the quiet interval may be shortened down to zero or slightly increased by up to the refresh cycle length to synchronize the LPI refresh cycle of the slave PHY with the master PHY.



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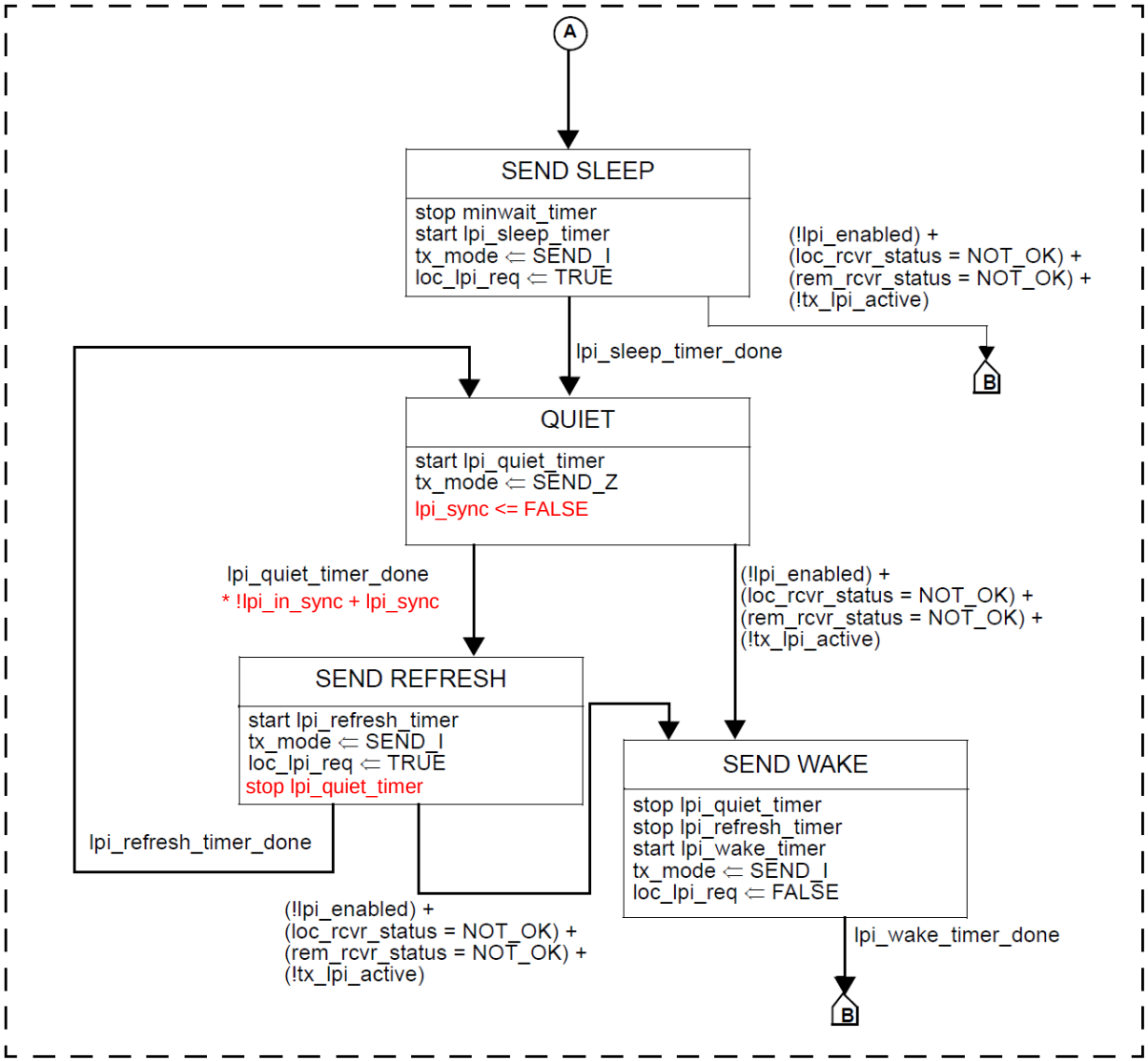

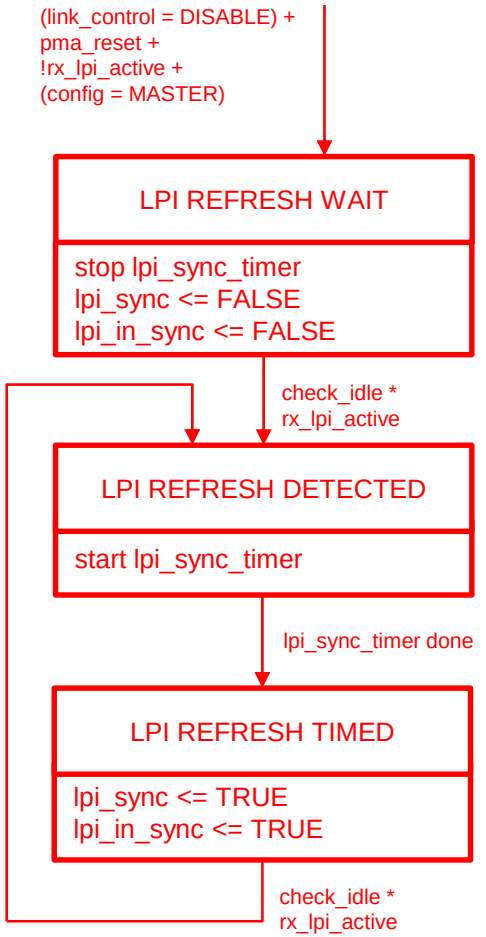

LPI Refresh Detection State Diagram

lpi_sync_timer: 1 ms ± 100 µs,
no auto restart

Questions

- Are issues expected, if the slave PHY is during the first synchronization to the master PHY not having a constant refresh cycle?

- For the quiet timing in Clause 78 currently 6000 to 6300 µs is intended to be specified. This is valid for the self timed quiet cycle. During synchronization of the slave PHY LPI cycle to the master PHY LPI cycle, values between 0 µs and approx. 6510 µs will be possible for the first time of synchronization. Is there a need to specify this explicitly in the Clause 78 timings and if yes, how could this be done?

- Are there other (better) proposals for synchronization of the master and the slave PHY quiet/refresh cycle?

- As I can for EEE only work on a theoretical base, there will be need for a detailed review on EEE for 10BASE-T1L. Who is willing to help here?

Thank You