

10 Mb/s Single Twisted Pair Ethernet PCS Layer Requirements

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IEEE P802.3cg 10 Mb/s Single Twisted Pair Ethernet Task Force

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PCS Layer

- The PCS layer is needed to convert the MII 10 Mbit/s data stream and also the PHY control information into a PAM-3 symbol stream in an efficient way.
- Currently a self synchronizing scrambler in combination with a 4B3T line code is being used.
- The PHY control information (e.g. SOF, EOF, Error) are being coded in the inter-frame gap between the Ethernet packets using a special comma sequence ("000 000") followed by three ternary symbols.
- To allow an independent implementation of the PCS layer and the PMA layer, modern PHY implementations code the control information within the normal data stream, so that no additional control information need to be fed from the PCS layer into the PMA layer.
- Nevertheless the physical coding on the link segment and especially also the coupling networks for the communication signal and the power have a significant influence on the PCS layer implementation requirements.
- A separation of the PCS layer and the PMA layer could allow an easy exchange of the PMA layer, e.g. from a PAM-3 for the long distance PHY to a DME encoding for a short distance PHY.

PCS Layer



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PCS Layer

- There are different requirements for the PCS layer, which have to be fulfilled:
 - Data and control information should be included into the same binary data stream.
 - As there is likely no FEC code, there is a need for a defined start of a data or control packet, so that a single bit error does not destroy the data stream for a longer duration.
 - The lower frequency content of the communication signal needs to be limited to allow an acceptable size of the power coupling inductors and the signal coupling capacitors.
 - The maximum BLW of the communication signal needs to be limited, not to run into the diode clamping of the inductors needed for intrinsically safe segments.
 - There needs to be an efficient way to code the binary signal into a PAM-3 line code.
- On the following slides the different requirements are explained in more detail.

Encoding of Data and Control Information

- Currently there are two different efficient encoder types for encoding the data and control information into a common binary data stream being used in the field of Ethernet:
 - 64B/66B or 128B/130B (or similar) encoders, which need 2 bit overhead, additionally to the payload data.
 - A "01" transition at the beginning of a packet signalizes a data packet.
 - A "10" transition at the beginning of a packet signalizes a control packet.
 - "00" and "11" are not allowed and cause a receive error.
 - 64B/65B or 80B/81B (or similar) encoders, which need 1 bit overhead additionally to the payload data
 - A single "0" at the beginning of a packet signalizes a data packet.
 - A single "1" at the beginning of a packet signalizes a control packet.
 - While a code with only one bit for distinguishing between a data and a control packet provides a lower coding overhead, such codes typically require an additional error correcting code (e.g. RS or LDPC), because otherwise flipping of this single bit could have a significant impact on the PHY receive side.
- The longer the data block is, the less coding overhead is necessary.
- On the other side, the longer the data block gets, also the latency of the PHY is being increased.
- Therefore a 64B/66B encoding (or even using smaller packets) could be a good compromise.

Limitation of Lower Corner Frequency

- The lower corner frequency of the PHY receive input path is currently approx. 200 kHz.
- This is a good compromise between cutting of low frequency disturbers, but not cutting of too much signal energy.
- For the current 4B3T encoding a maximum of 5 consecutive "+1" or -1" and a maximum of 10 consecutive "0" (including the "000 000" comma sequence) can occur, limiting the lower frequency content of the signal to values in the range of 750 kHz.
- While the high pass filter corner frequency of the receiver is in the range of 200 kHz, allowing for component tolerances the lower communication signal frequency part should be in the range of 250 kHz or above.
- Depending on the chosen coupling network for providing energy to the link segment, using two times 500 µH inductors in combination with 200 nF capacitors (as discussed in the "PHY Coupling Network" presentation), the 200 kHz high pass filter allows for a power supply noise tolerance (excluding the coupling network) of up to 100 mV_{pp} assuming 10 mV_{pp} in-band noise.
- Going to a lower high pass filter frequency would cause a need for higher inductance values or would cause a reduced power supply noise tolerance.

Limitation of maximum allowed BLW

- The coupling circuit intended to be used for intrinsically safe applications, will contain several clamping diodes, which have an influence on the communication signal.
- The higher the BLW is, the higher the influence of the clamping diodes will be, especially at higher temperatures.
- More details on this effect are given in the "PHY Coupling Network" presentation.
- The maximum BLW should not exceed approx. 10 % to prevent an unintended clamping of the communication signal.
- As the specified, maximum allowed BER is 10⁻⁹, the probability for a BLW of more than 10 % should be below 10⁻¹¹, to have some safety margin.

Mapping the Binary Data to PAM-3 Symbols

- There needs to be an efficient way of coding the binary data stream into PAM-3 symbols.
- The easiest way would be to just encode 3 binary data bits (8 combinations) into 2 ternary symbols (9 combinations, with "00" not being used).
- Nevertheless this coding on its own would not lead to a DC and BLW free line code.
- Therefore such a coding needs some kind of preprocessing (e.g. by scrambling the binary data stream).
- Alternatively a more complex line code, which provides a DC free communication signal with a low BLW needs to be implemented.

Summary

- The encoding of the data stream from the MII interface to the PMA layer consists of several steps, which are necessary to provide the PMA with a symbol stream that fulfills the requirements of the link segment:
 - There is need for a robust encoding, which allows a BER of less than 10⁻⁹, even without FEC, which means, that the signaling of control information should not rely on a single bit.
 - The encoding of the control information should add only a small overhead.
 - This could e.g. being achieved by a 64B/66B or similar coding.
 - The BLW should not exceed 10 % with a probability of less than 10⁻¹¹.
 - Are there scrambler polynomials or other methods, which support (in combination with the PAM-3 symbol encoding) such a requirement?
 - The encoding needs to support a high pass filter characteristic of the system with a corner frequency of 200 kHz or higher to allow an acceptable size of the coupling network components.
 - The binary data stream needs to be converted to a PAM-3 data stream.
 - Ideally this encoding is such simple (e.g. 3B2T), so that this part could be easily exchanged to support e.g. a
 DME encoding for the short distance PHYs (in this case just three DME instead of two PAM-3 symbols could be
 transmitted).
 - If a more complex line code is necessary to maintain the BLW limits and to provide a DC free signal, then the maximum block length, for which the BLW limit is being guaranteed, should not be longer than e.g. 16 to 32 bits.

Thank You

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