10 Mb/s Single Twisted Pair Ethernet

10BASE-T1L PoDL Ideas

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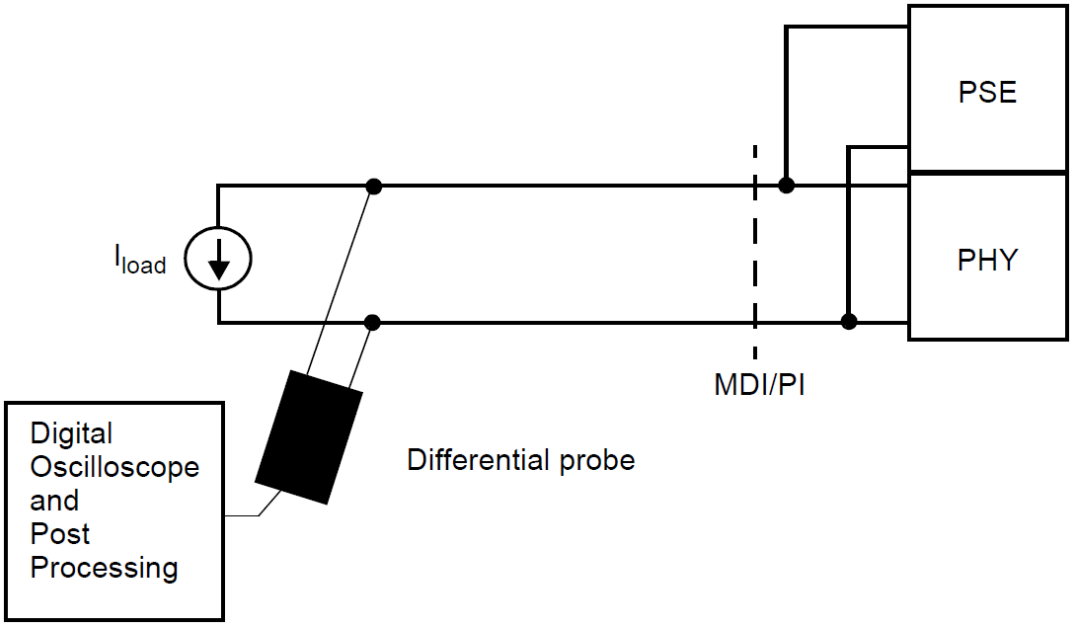
PSE Power Feeding Ripple and Noise

- Clause 104 specifies in 104.4.6.3 the maximum allowed PSE ripple and transients, depending if the PoDL circuit is intended to be used with a 100BASE-T1 (66.666 MSymbols/s) or 1000BASE-T1 (750 MSymbols/s) PHY.
- A 10BASE-T1 PHY has a symbol rate of 7.5 MSPS/s, therefore it is necessary to align the specified ripple and noise frequency range to the lower signal frequency.
- The ripple and noise measurement at the MDI is done using a differential probe, in conjunction with a scope and some kind of post processing, which is described on the next slide.



PSE Power Feeding Ripple and Noise

- The differential probe is having a nominal impedance of 100 Ω in the higher frequency range.
- In the lower frequency range the impedance is described by the following formula (104-1):

$$Z_{in}(f) = 100\ \Omega \pm 0.1\ \% \times \frac{\sqrt{f^2 + f_1^2}}{f}$$

- Reason for the change in the input impedance is the coupling capacitance for AC coupling the differential probe to the powered system.

- The transfer function of the differential probe is specified to be:

$$H_1(f) = \frac{f}{\sqrt{f^2 + f_1^2}}\ with\ f_1 = 31.8\ kHz\ for\ 100BASE-T1\ and f_1 = 318\ kHz\ for\ 1000BASE-T1$$

- Assuming, that the source impedance of the ripple or noise is significantly higher than the input impedance of the differential probe, the specified transfer function compensates for the change in input impedance over frequency of the differential probe.

- For a PSE being specified for the use with a 100BASE-T1 PHY, the corner frequency f_1 is specified to be 31.8 kHz, this equals to a coupling capacitance of 100 nF in each input path of the differential probe.

- As the 10BASE-T1L PHY symbol rate is approx. ten times lower, it is suggested to use a 1 µF coupling capacitor in each input path of the differential probe, resulting in a corner frequency f_1 of **3.18 kHz**.

PSE Power Feeding Ripple and Noise

- In Clause 104, table 104-4, the maximum allowed noise and ripple voltage at the output of the differential probe is limited to **100 mV_{pp}**, measured at the MDI, within a frequency range of **1 kHz to 10 MHz**.
- Within the communication signal frequency range a maximum noise and ripple voltage of **10 mV_{pp}** at the MDI is allowed (this takes approx. 1/3 of the **overall noise immunity of about 30 mV_{pp}** being measured with the current FPGA based evaluation board for the 10BASE-T1L PHY, which is already a significant amount).
- To adopt the noise and ripple voltage output of the differential probe to the relevant frequency range the following transfer function is being used during the post-processing:

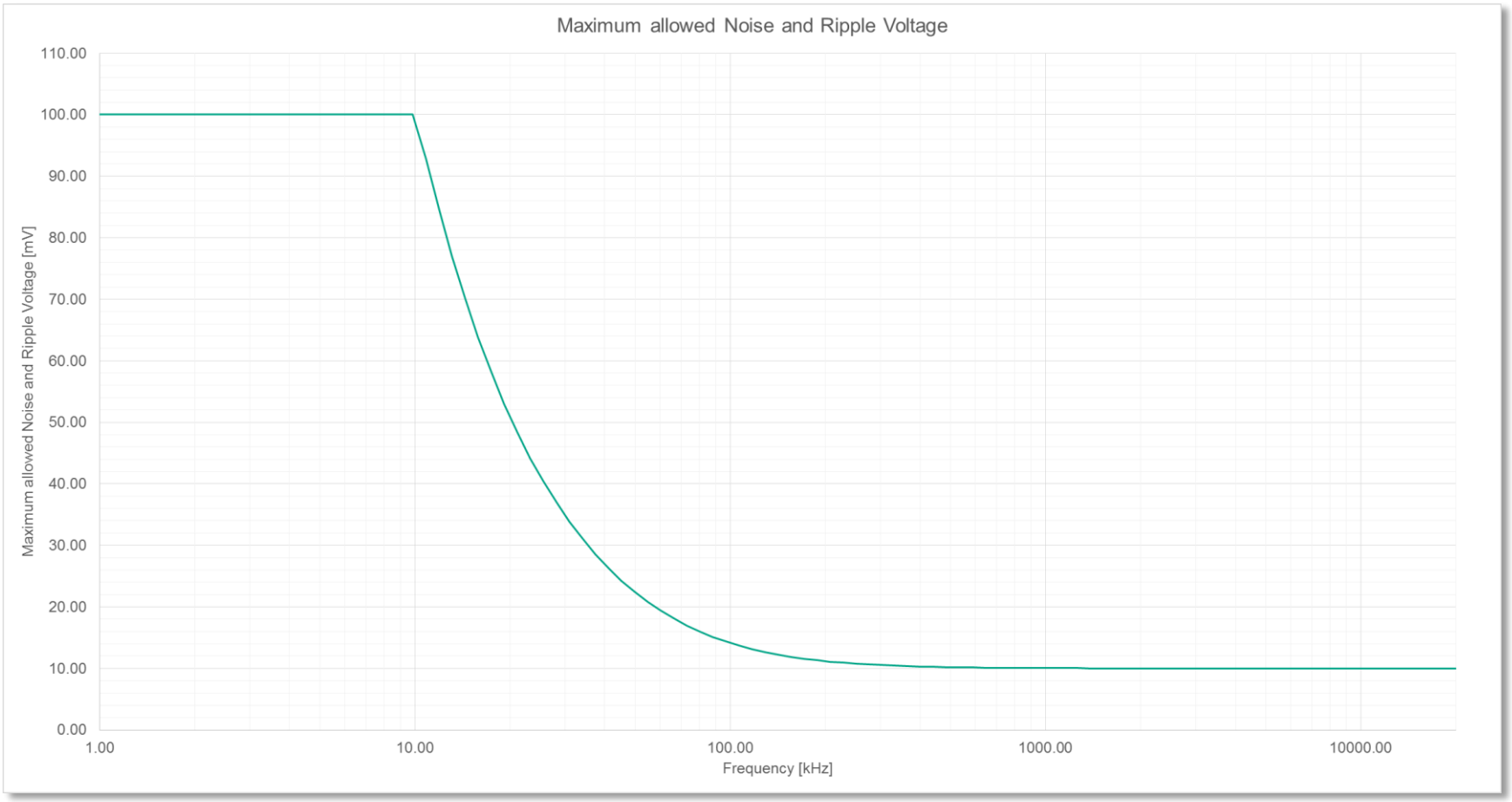
$$H_2(f) = \frac{f}{\sqrt{f^2 + f_2^2}} \; with \; f_2 = 1 \; MHz \; for \; 100BASE-T1 \; and f_2 = 10 \; MHz \; for \; 1000BASE-T1$$

- As the symbol rate of a 10BASE-T1L PHY is approx. ten times lower than that of a 100BASE-T1 PHY and 100 times lower than that of a 1000BASE-T1 PHY, it is suggested to set the corner frequency f_2 to **100 kHz** for a 10BASE-T1L link segment.
- It seems to make sense for a PD to use the same noise values and noise frequency range as for the PSE.

PSE Power Feeding Ripple and Noise

- The following diagram shows the resulting maximum allowed noise and ripple voltage:

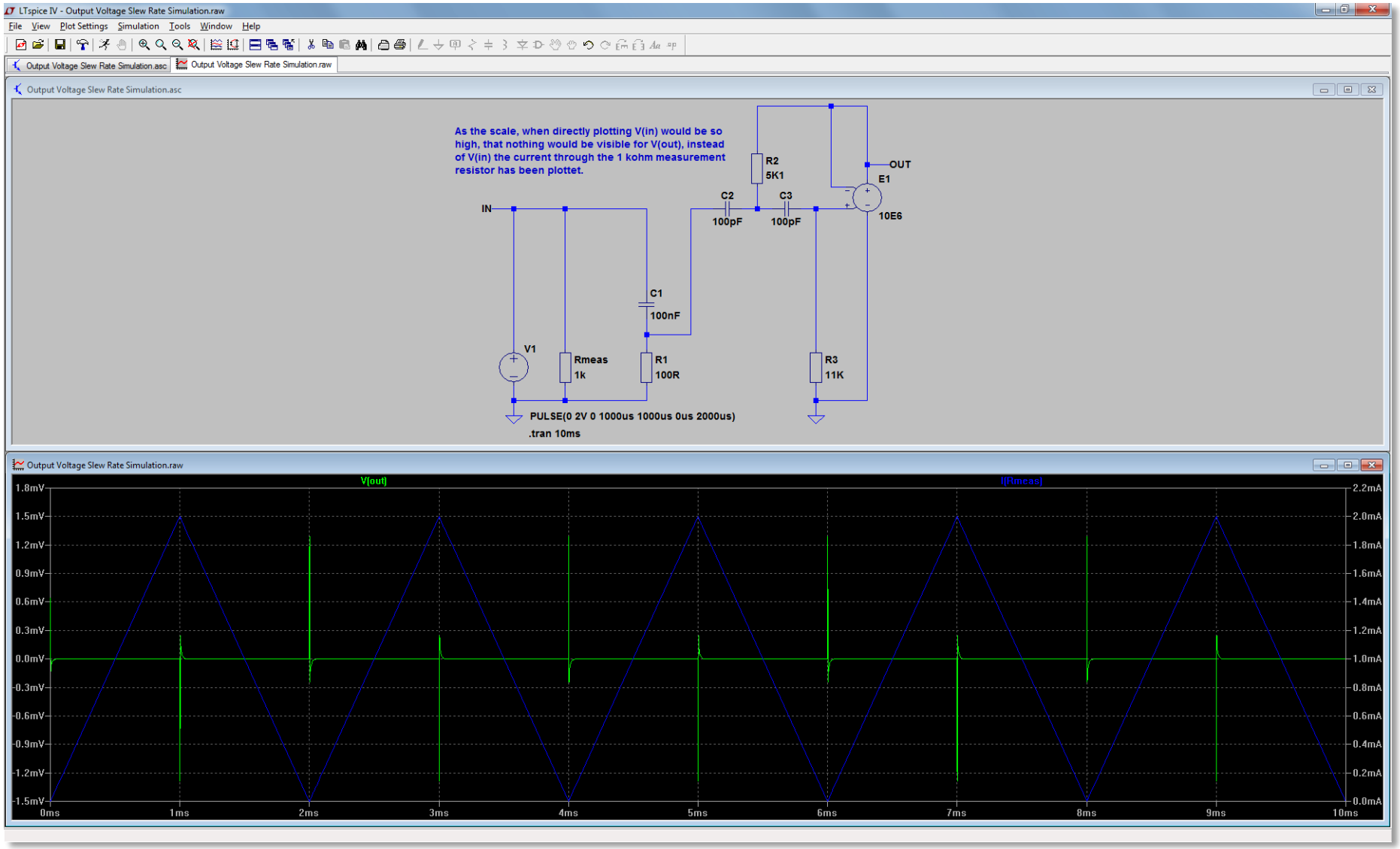
$$U_{noise}(f) = \min\left(100\ mv_{pp}, \frac{10\ mv_{pp}}{H_2(f)}\right)$$



PSE Output Voltage Slew Rate Limitation

- Clause 104 specifies in 104.4.6 a maximum output voltage slew rate of 22 V/ms for a PSE intended to be used with a 100BASE-T1 PHY and a maximum output voltage slew rate of 200 V/ms for a PSE intended to be used with a 1000BASE-T1 PHY.
- As the symbol rate of a 10BASE-T1L PHY is approx. ten times lower than that of a 100BASE-T1 PHY and 100 times lower than that of a 1000BASE-T1 PHY, it is suggested to specify a maximum output voltage slew rate (dV/dt) for the PSE of **2 V/ms**.
- The following slide shows a simulation for a PSE output voltage slew rate of 2 V/ms in combination with the 2nd order 200 kHz high pass filter as being implemented in the current FPGA based evaluation board for the 10BASE-T1L PHY.
- Applying a triangular waveform with a slew rate of ±2 V/ms leads, after the 200 kHz high-pass filter, to spikes in the range of ± 1.3 mV, which seem to be acceptable.
- Reducing the high-pass filter frequency to lower values would significantly increase the voltage of the spikes, so that the maximum allowed slew rate would need to be reduced even further.
- As for the PSE the maximum output voltage slew rate is being specified, it seems to make sense to specify also 2 V/ms as maximum input voltage slew rate for the PD to accept.

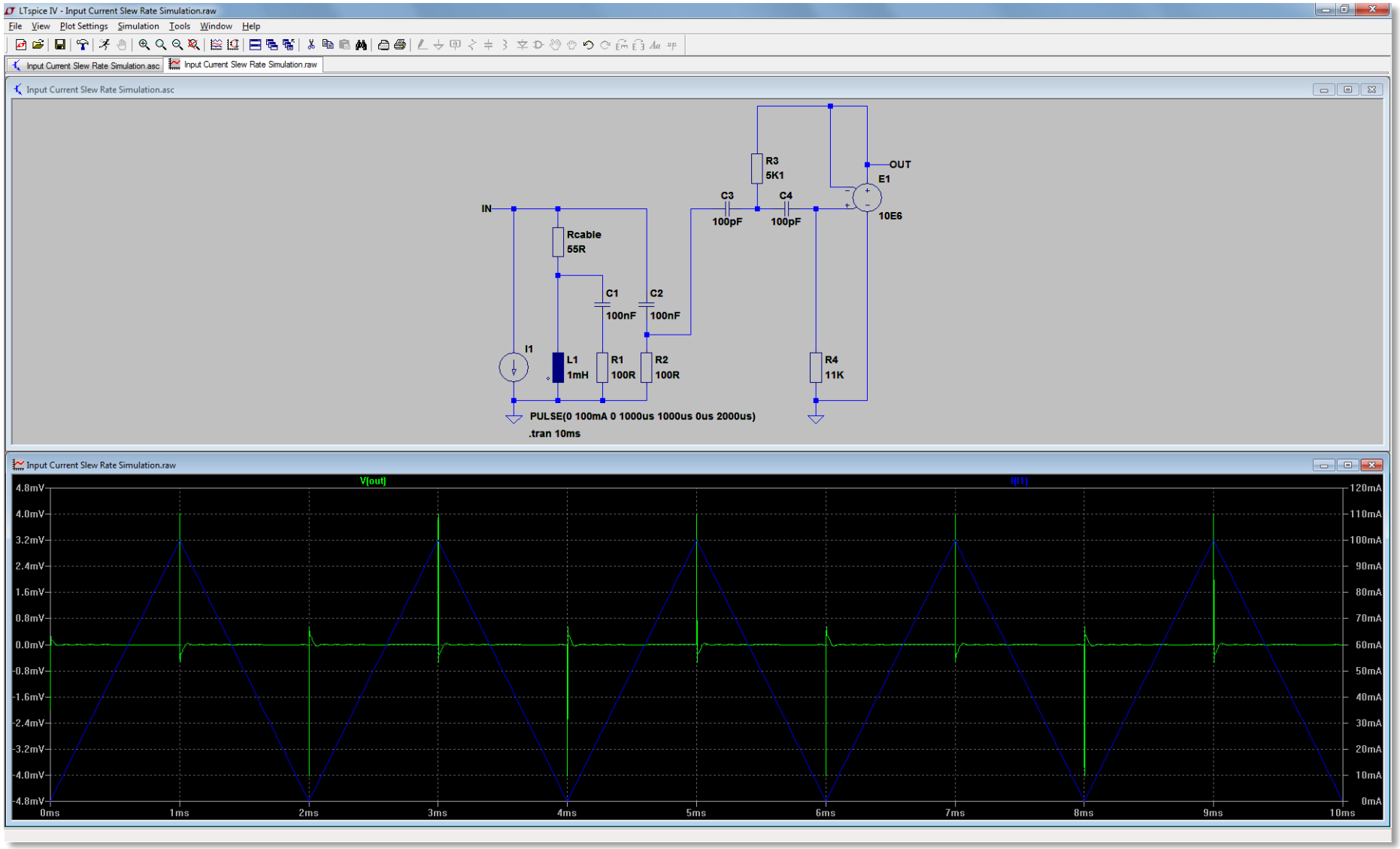
PSE Output Voltage Slew Rate Limitation



PD Input Current Slew Rate Limitation

- Clause 104 specifies in 104.5.6 a maximum input current slew rate of 1 A/ms for a PD intended to be used with a 100BASE-T1 PHY and a maximum input current slew rate of 10 A/ms for a PD intended to be used with a 1000BASE-T1 PHY.
- As the symbol rate of a 10BASE-T1L PHY is approx. 10 times lower than that of a 100BASE-T1 PHY and approx. 100 times lower than that of a 1000BASE-T1 PHY, it is suggested to specify a maximum input current slew rate (dI/dt) for the PD of **100 mA/ms**.
- The following slide shows a simulation for a PD input current slew rate of 100 mA/ms in combination with the 2nd order 200 kHz high pass filter as being implemented in the current FPGA based evaluation board for the 10BASE-T1L PHY.
- Applying a triangular waveform with a slew rate of ±100 mA/ms leads, after the 200 kHz high-pass filter, to spikes in the range of ± 4.0 mV, which seem to be acceptable (this is the worst case, as the slew rate directly changes from +100 mA/ms to -100 mA/ms and so on, without any time in between, therefore in practical implementations the spikes typically should be lower).
- Reducing the high-pass filter frequency to lower values would significantly increase the voltage of the spikes, so that the maximum allowed slew rate would need to be reduced even further.

PD Input Current Slew Rate Limitation



PHY Coupling Capacitors

- Clause 104 specifies a maximum input capacitance of the PD during classification of 200 nF (see table 104-7, item 6b).

- This value is also including the coupling capacitors between the PHY IC and the MDI.
- A minimum coupling capacitance of 200 nF in each line seems to be suitable for a 10BASE-T1L PHY, resulting in a 100 nF line-to-line capacitance.
- As the two wire system is being powered, at least the coupling capacitor connected to the positive signal line, can see a significant amount of DC bias.
- This DC bias can lead to a significant reduction in capacitance, depending on the dielectric, the voltage rating and the mechanical size of the capacitor.
- To prevent an unintended unbalance, ceramic capacitors with a relatively stable dielectric (e.g. X7R), a high enough voltage rating and size, with some headroom need to be chosen.
- Nevertheless the capacitors have to be designed in, so that they can compensate for the biasing effect and thus have to provide a higher typical capacitance.

- When choosing capacitors to compensate for the voltage biasing effect, it needs to be ensured, that these capacitors including tolerances do not provide a higher line-to-line capacitance than 200 nF (which means up to 400 nF per capacitor, if no other capacitors are in the circuit).

New PoDL Types/Power Classes

- The PoDL standard specifies four different PSE/PD types so far:

PSE/PD Type	Description
A	PSE/PD for 100BASE-T1 only
B	PSE/PD for 1000BASE-T1 only
C	PSE/PD for 100BASE-T1 and 1000BASE-T1
D	Not compatible PSE/PD

- To add the 10BASE-T1L PHY compatibility it seems to be reasonable to add two more types to the PoDL standard:

PSE/PD Type	Description
E	PSE/PD for 10BASE-T1L only
F	PSE/PD for 10BASE-T1L, 100BASE-T1(L)

- The maximum allowed link segment loop resistance needs to be adopted to fit to the higher link segment length and relevant power requirements (needs to be checked how this fits to the PD classification).
- Suggested is to define the loop resistance to allow for a maximum voltage drop across the cable of 40 % to 45 % of the minimum output voltage of the PSE.
- This would require additional power classes and likely tighter specified PSEs/PDs as the standard power classes only allow for a maximum of 30 % voltage drop across the cable.
- A fieldbus barrier e.g. has a supply voltage range of 16 to 32 V, while the minimum output voltage of the fieldbus power supply is 28 V, which leads to a maximum voltage drop across the cable of approx. 43 %.

Engineered Systems

- Engineered process industry systems will have to take all relevant parameters from Clause 104 to guarantee an interoperability between the PHY and the powering system.
- Nevertheless these applications typically have many other constraints as long cable runs, intrinsic safety, daisy-chain trunk topologies, and system wide power distribution.
- PoDL has been designed as a reliable powering system for point-to-point applications in a plug-and-play environment.
- Most of the additional requirements for process automation applications are out of the scope of PoDL and would add additional complexity to the standard, what also would burden other mass market applications.
- The PoDL silicon eco system would also need to be designed in a way that it would allow to add additional external safety measures (e.g. series resistors, so that the power dissipation within the IC may be limited in case of a failure) for the use in hazardous area applications.
- A completely discrete PoDL implementation, which could be necessary to implement the needed safety measures for intrinsic safety, likely would cause a significant amount of additional components for each port.

Summary

- An easy path for implementing a powered 10BASE-T1L structure would be to adopt the parameters which are required for PHY interoperability in the PoDL standard:
  - MDI Return Loss (tbd)
  - Maximum noise/ripple voltage (e.g. 100 mV_{pp})
  - Maximum in-band noise/ripple voltage (e.g. 10 mV_{pp})
  - Provide adopted corner frequencies for noise/ripple voltage measurement (e.g. f_1 = 3.18 kHz, f_2 = 100 kHz)
  - PSE output voltage slew rate (e.g. 2 V/ms)
  - PD input voltage slew rate (e.g. 2 V/ms)
  - PD input current slew rate (e.g. 100 mA/ms)
  - Adopt maximum loop resistance (e.g. 40 to 45 % maximum voltage drop across the cable)
  - Add new PoDL types (e.g. one for the 10BASE-T1L PHY and one universal type for 10/100BASE-T1(L))
- For point-to-point systems, which benefit from the PoDL features this allows an easy path to support the 10 MBit/s PHYs.
- For engineered systems including daisy-chain and multi-drop topologies, a good approach could be to take all relevant parameters from Clause 104, but do not implement the probing or classification sequences from PoDL (and just power up the devices, as it is known, what is there).
- For plug-and play point-to-point systems PoDL seems to be a good choice also for 10 MBit/s speeds.

Thank You