10BASE-T1L Low Power Idle (802.3cg D2.0)

NIALL FITZGERALD

15 AUGUST 2018

10BASE-T1L LPI (part 1)

Asymmetric LPI operation

- PHY enters LPI QUIET mode, and stops transmission, regardless of whether or not link partner PHY is also operating in LPI QUIET mode.
- No defined relationship between MASTER and SLAVE LPI refreshes. They are fully asynchronous, and timing of refresh events depends ultimately on time of LPI assertion at the PHYs' MIIs.

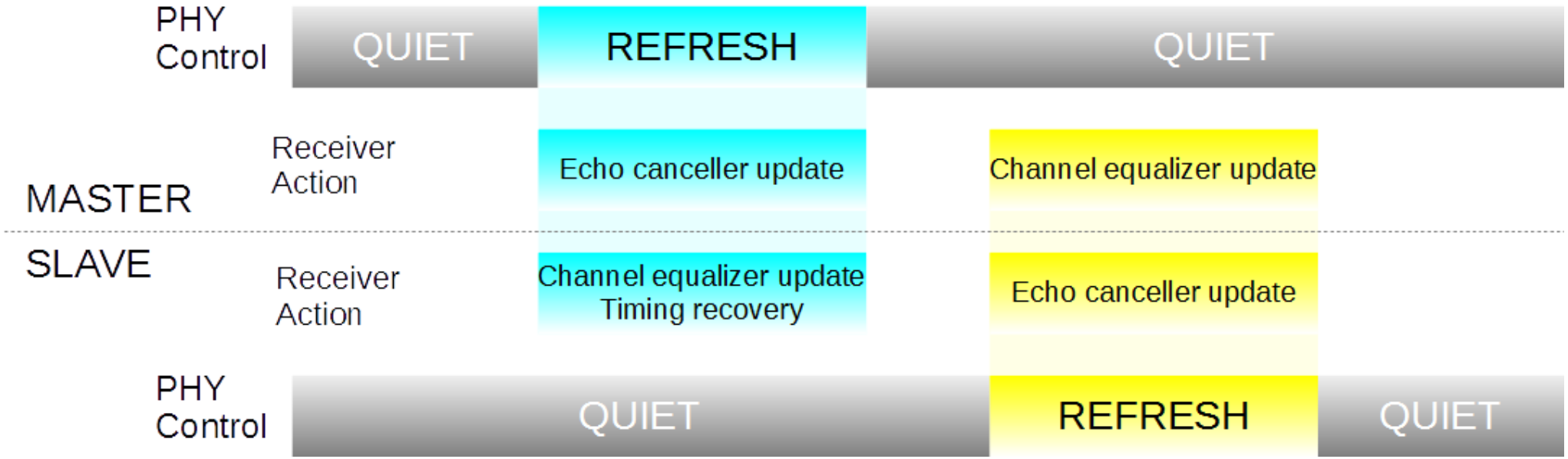
MASTER/SLAVE scheme for timing recovery

- SLAVE PHY must recover timing information from signal it receives from MASTER PHY, and uses recovered clock for its own transmission
- Asymmetric LPI operation implies that the MASTER could be in the LPI QUIET state while the SLAVE is transmitting data frames, so the SLAVE would have to transmit in the absence of receiving signals from the MASTER.

10BASE-T1L LPI (part 2)

PHY has to perform echo cancellation, channel equalization, and timing recovery (SLAVE)

- Equalizer coefficient update, and timing recovery, require reception of signal from link partner PHY. For LPI, this requires refresh from link partner PHY.
- Echo canceller coefficient update requires local transmission. For LPI, this requires local PHY refresh.
- Refresh means receiver activity in both PHYs.



10BASE-T1L LPI (part 3)

Refreshes from MASTER and SLAVE will be asynchronous

- Entry to refresh will be determined by when MAC asserts LPI at MII.
- Refreshes might wholly overlap, partially overlap, or be completely distinct (no overlap). PHY implementations will have to be able to handle all scenarios.

PHY energy savings could be better

- Time spent in refresh is 205 µs (lpi_refresh_timer); time spent in quiet is 2050 µs (lpi_quiet_timer).
- Ratio of refresh to quiet apparently 1/10.
- PHY receiver will be active 2/10 of time. Refreshes are asynchronous, unlikely to overlap, and refreshes require action from receivers in both PHYs.

1000BASE-T LPI Overview

1000BASE-T EEE specifies symmetric LPI functionality at the PHY level:

- The LPI QUIET state is only entered when LPI is requested on both sides.
- LPI request is still conveyed in idle signalling between PHYs, so LPI is fully asymmetric above the PHY layer.

In general, when one PHY is transmitting then so is the other.

- 1000BASE-T PHY knows LPI refreshes (UPDATE state) are to be used for update of both canceller coefficients and channel equalizer coefficients, as well as timing recovery for the SLAVE.
- If the SLAVE PHY is transmitting data frames, but the MASTER is not transmitting data frames, the MASTER will still be transmitting 1000BASE-T idle. The SLAVE can then keep timing recovery fully active.

When the LPI QUIET mode is entered, the 1000BASE-T EEE PHY can be quite aggressive in saving power.

- SLAVE timing recovery can be shut down
- The LPI wake-up process is intended to allow the SLAVE PHY to correct for any timing phase offset present after the time spent in LPI QUIET.

Fail-safe behaviour is built in to the LPI wake-up process

- Normally the LPI wake-up should complete within 16.5 us.
- If the LPI wake-up has not completed within 100 us, then the link is brought down.

1000BASE-T1 LPI Overview

MASTER/SLAVE timing scheme, and EEE defines asymmetric LPI.

- Shown here is Figure 97-11 of 1000BASE-T1.

- Adopts a staggered approach to LPI approaches; MASTER and SLAVE LPI refreshes do not coincide.
- This adds predictability regarding when refreshes occur

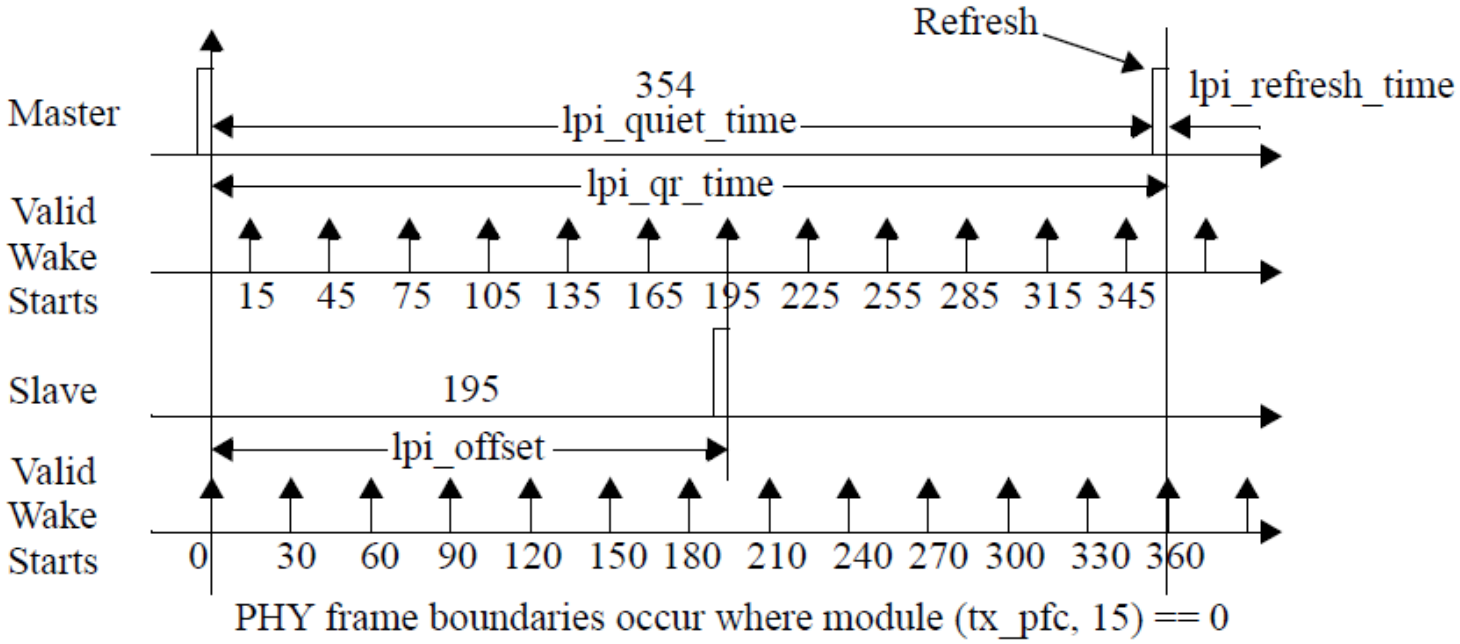


Figure 97–11—LPI signal timing

1000BASE-T1 LPI refresh monitor

1000BASE-T1 EEE must implement Clause 97.4.2.7 Refresh monitor function.

The refresh monitor is intended to detect when refreshes are not received as expected from the link partner. This would indicate:

- Link partner powerdown
- Cable disconnection

The Refresh monitor function causes the link to come down if refreshes are not received as expected for a defined period of time (4.32 ms for 1000BASE-T1 EEE).

Potential improvements to 10BASE-T1L LPI

- 10BASE-T1L asymmetric LPI needs refresh monitor on the receive side
- 10BASE-T1L asymmetric LPI might need additional specification of MASTER clock behaviour during LPI QUIET, so that SLAVE does not have to worry about MASTER frequency drifting during LPI QUIET
- 10BASE-T1L asymmetric LPI would benefit from adding more certainty regarding when LPI refreshes occur
- A 10BASE-T1L symmetric LPI scheme (similar to 1000BASE-T LPI) might be adopted

Thank you