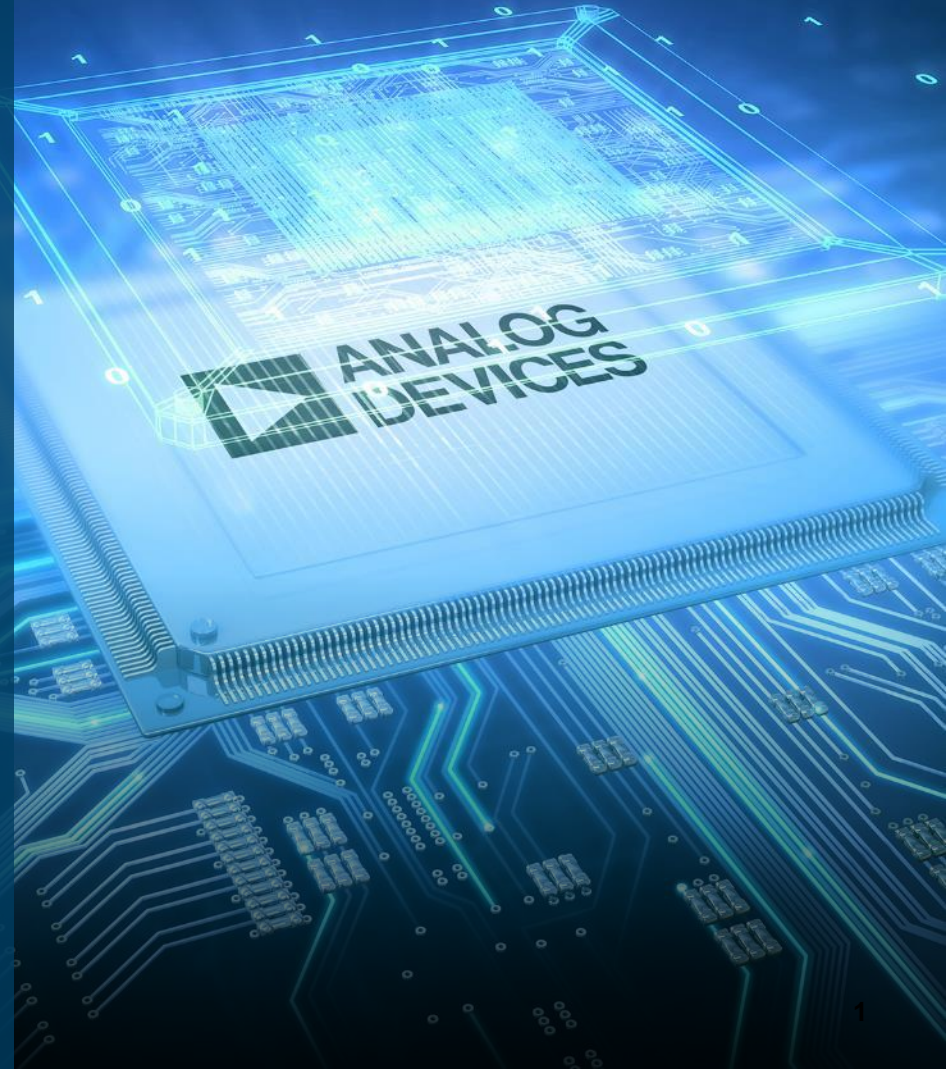




AHEAD OF WHAT'S POSSIBLE™

Simulations with Intrinsically Safe component values

OISÍN Ó CUANACHÁIN

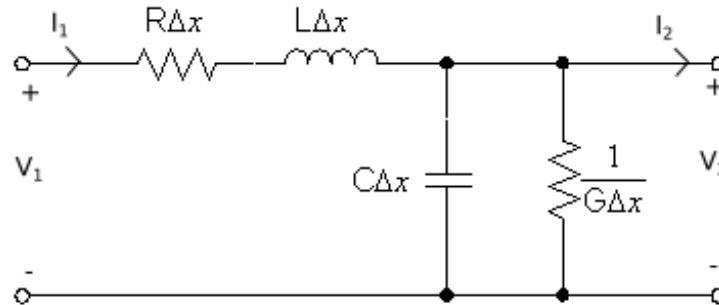


Background

- http://www.ieee802.org/3/cg/public/adhoc/0117_cg_adhoc_IntrinsicSafety_r01.pdf proposed some component values on the signal path to meet Objective 10: *'Do not preclude working within an Intrinsically Safe device and system as defined in IEC 60079'*
- This generated much discussion and it was suggested that PHY designers simulate the proposed circuit to verify that it was workable
- This slide deck summarizes the results of such simulations, specifically the simulations use:
 - The baseline Link Segment I.L. and R.L. limits from proposal http://www.ieee802.org/3/cg/public/Jan2017/diminico_01a_0117.pdf
 - The symbol rate, modulation, 4B3T coding proposals and cable delay from http://www.ieee802.org/3/cg/public/Jan2017/Graber_10SPE_10_0117.pdf
 - 200nF/line coupling capacitors and 100 Ohm resistors proposed for Intrinsic Safety from http://www.ieee802.org/3/cg/public/adhoc/0117_cg_adhoc_IntrinsicSafety_r01.pdf

Link Segment Model:

- Model starts with an incremental section of Lossy Transmission Line:



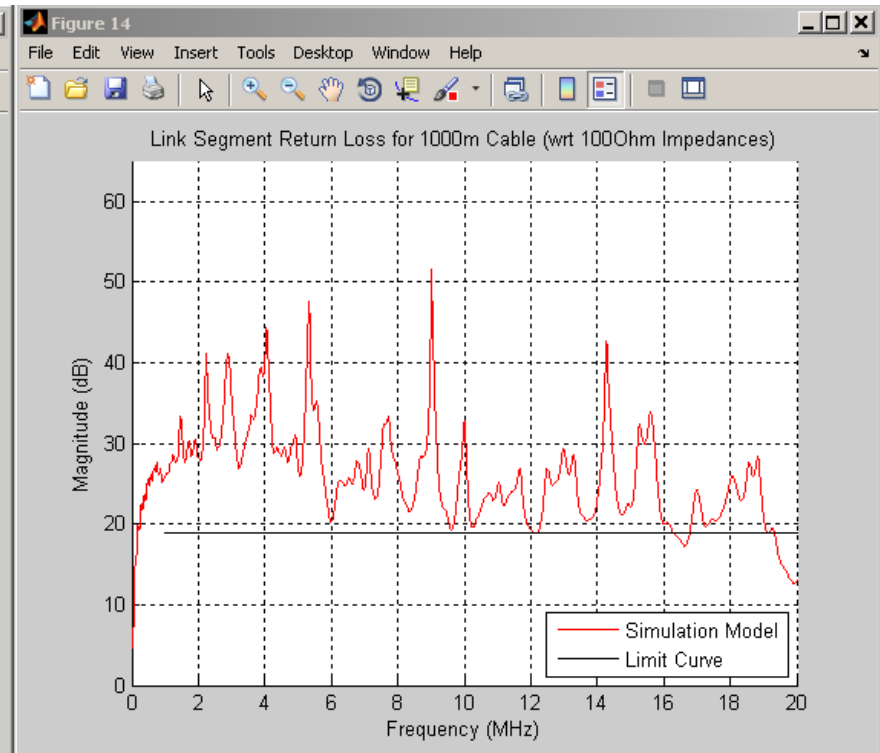
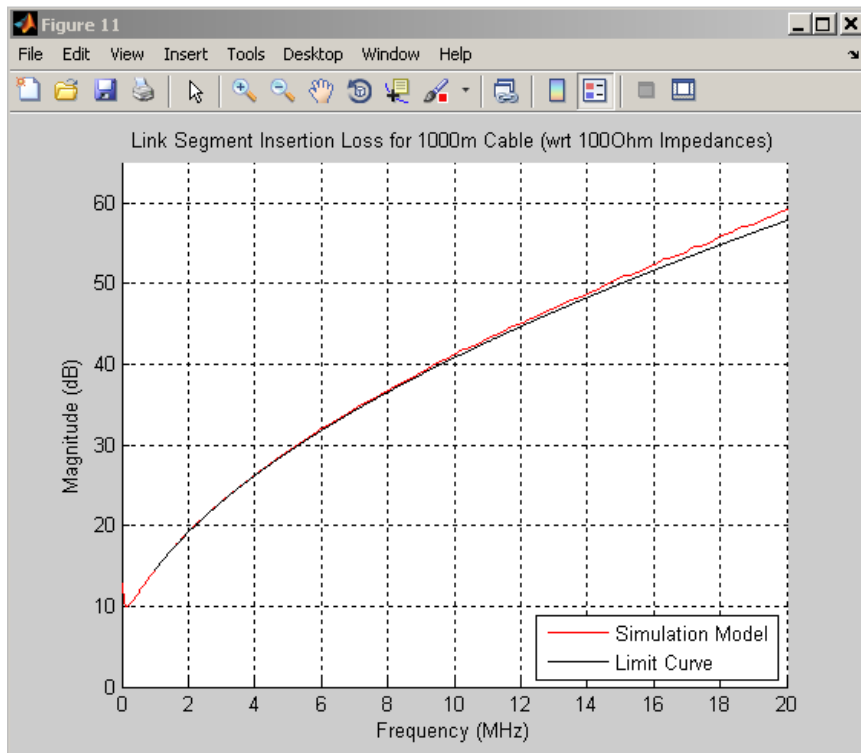
- Standard analysis shows that its behaviour is governed by Characteristic Impedance, Z_0 , and Propagation Constant γ , with the ABCD matrix being:

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} \cosh(\gamma\Delta x) & Z_0 \sinh(\gamma\Delta x) \\ 1/Z_0 \sinh(\gamma\Delta x) & \cosh(\gamma\Delta x) \end{pmatrix} \cdot \begin{pmatrix} V_2 \\ I_2 \end{pmatrix}$$

- Relate Z_0 and γ to proposed Insertion Loss constants and proposed propagation delay (5ns/m) in a similar fashion to Annex L of TIA-EIA-568-B2.
- Insertion Loss (f) $\leq 10 \cdot (1.23 \cdot \text{SQRT}(f) + 0.01 \cdot f + 0.2 / \text{SQRT}(f)) + 10 \cdot (0.02 \cdot \text{sqrt}(f))$ (dB)
- Return Loss (f) ≥ 19 dB [1(TBD) MHz to 20 (TBD) MHz]
- The entire model is then calculated by multiplying the ABCD matrices for a cascade of $\text{cable_length} / \Delta x$ such incremental elements with Z_0 varying about its nominal value according to a Gaussian random variable to model cable roughness which generates Structural Return Loss.

Link Segment Model:

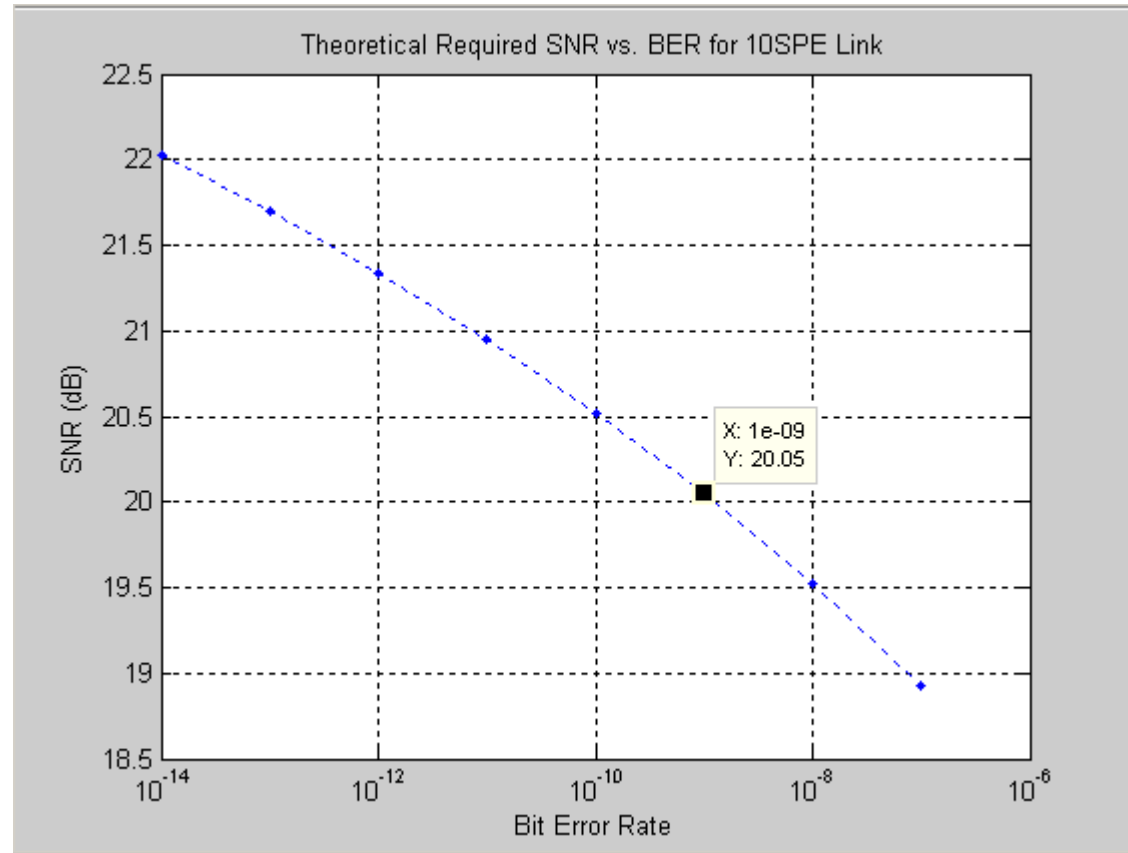
- This is then combined with source and load impedances and the open cct voltage transfer function is calculated at frequencies $0: \Delta f: \frac{f_s}{2}$ and the spectrum up to f_s is then completed by conjugate symmetry. Taking the IFFT then yields a Time Domain Impulse Response for use in simulations.
- Echo model is generated in the same fashion except that the S_{11} reflection coefficient is calculated instead of the Open Circuit Voltage transfer function.
- The result is a transmission line channel model tailored to approximate the proposed Limit Curves:



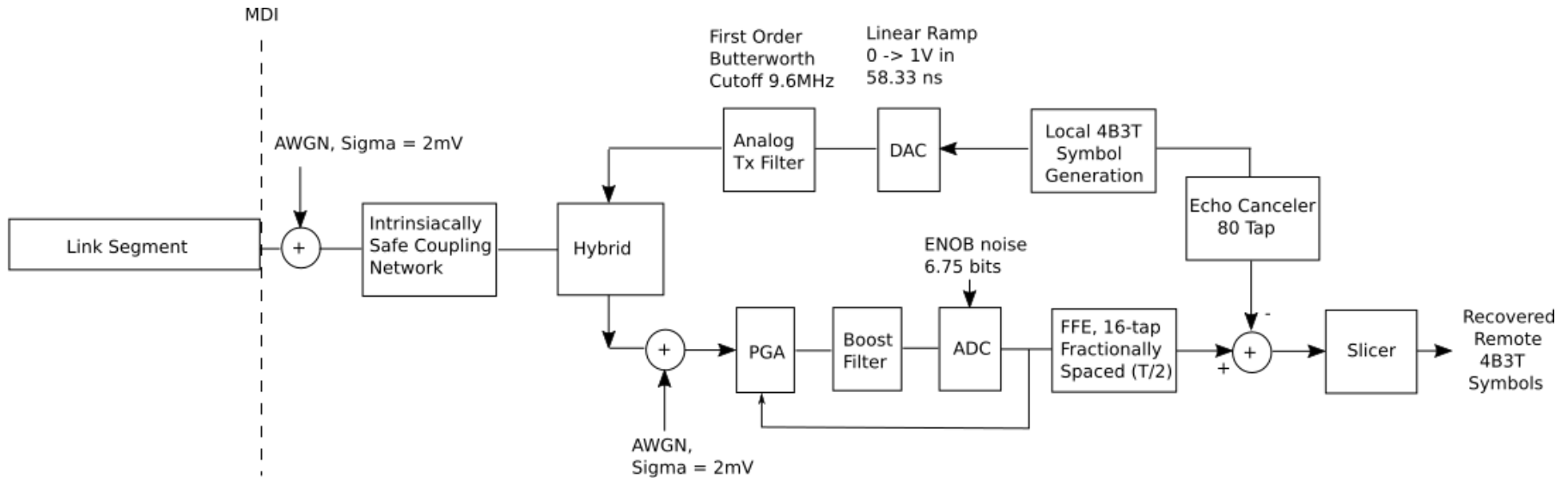
Modulation etc.:

- As proposed by http://www.ieee802.org/3/cg/public/Jan2017/Graber_10SPE_10_0117.pdf

- PAM-3
- 4B3T near DC-free line code => 1.333 bits/ baud
- 7.5MHz Tx clock
- For 1000m Link the BER objective is $1e-9$
- Using the above parameters I calculate a required SNR at the slicer of 20.05dB



Simulation Block Diagram

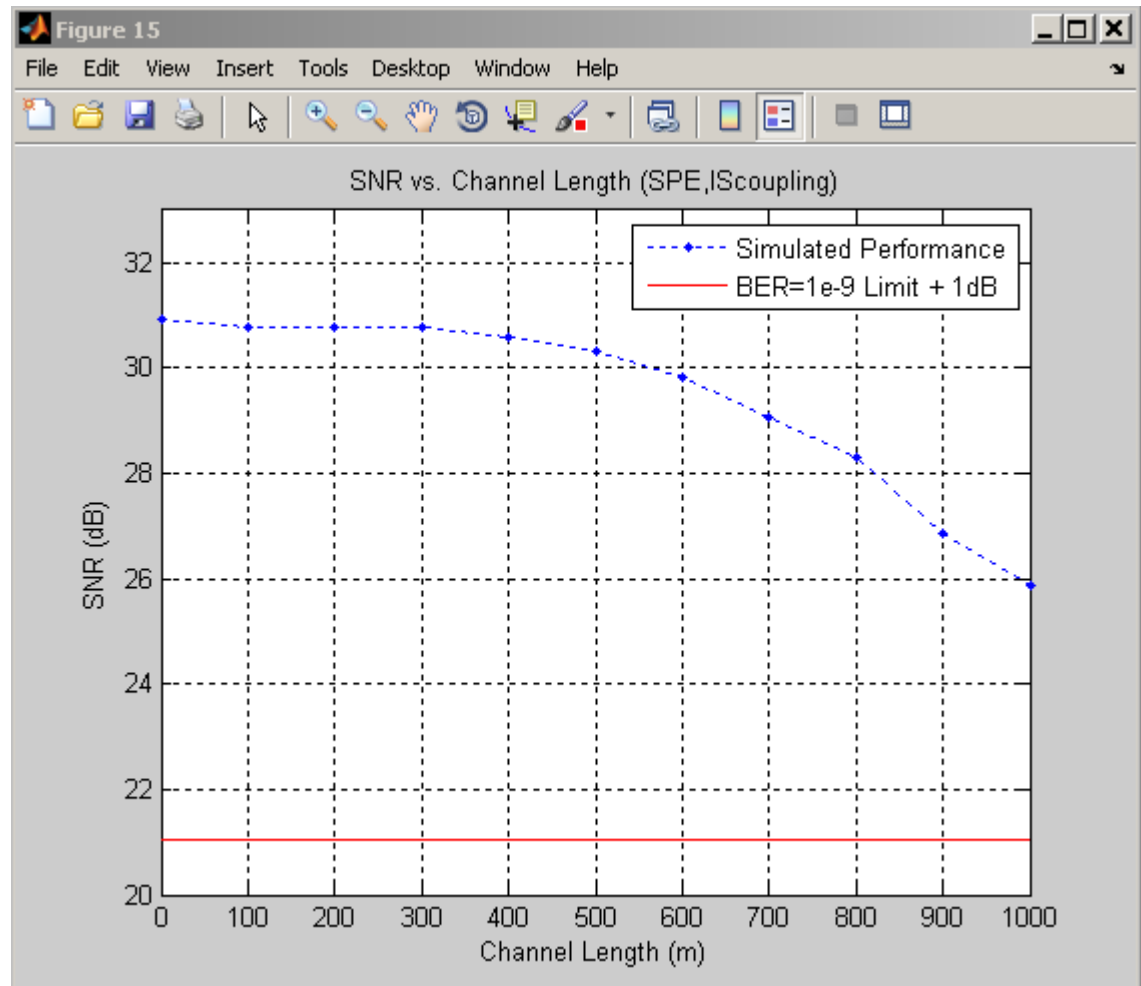


ADC: 8-Bit, 1V range, ENOB = 6.75 bits

* Note noise sources are specified in terms of the RMS voltage of the underlying analog noise signal. In the simulation these are sampled at the FFE rate (= 15Msps) giving noise PSD of -115.74 dBm/Hz per source.

PHY parameters and Results:

- 16-tap T/2 fractionally-spaced Equalizer
- 80-tap Echo Canceler
- 8-bit 1V range ADC
- PGA with 19.2dB range
- I.S. 50-Ohm per line termination resistors and 200nF per line coupling capacitors
- Margin of 1.0dB added to SNR target to allow for unmodelled implementation losses

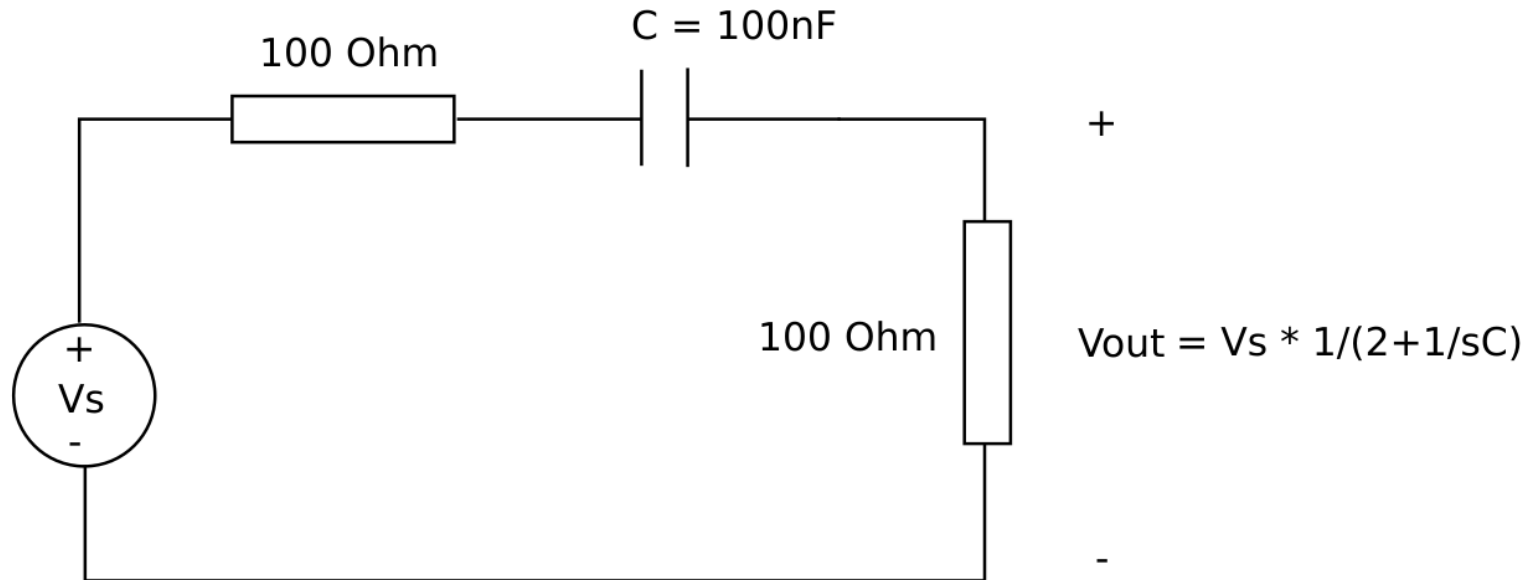


Discussion of Results

- As predicted by <http://www.ieee802.org/3/cg/email/msg00024.html>
- *'200 nF @ 1MHz < 1Ohm -> should not make a problem for the communication, but must be kept in mind'*
- Transfer function through this RC network is very benign and shouldn't degrade performance significantly however there may be a complication in how this is included in the standard.
- In recent 802.3 standards this response is specified via a Droop Spec:
 - 1000BaseT: **40.6.1.2.2 Maximum output droop** equivalent to highpass response with max allowed pole location at 100kHz
 - 100BaseT1: **96.5.4.1 Transmitter output droop** equivalent to highpass response with max allowed pole location at 190kHz
 - 1000BaseT1: **97.5.3.1 Maximum output droop** equivalent to highpass response with max allowed pole location at 1.4MHz

I.S. Coupling Highpass Response

Single-ended Equivalent Circuit for I.S. components



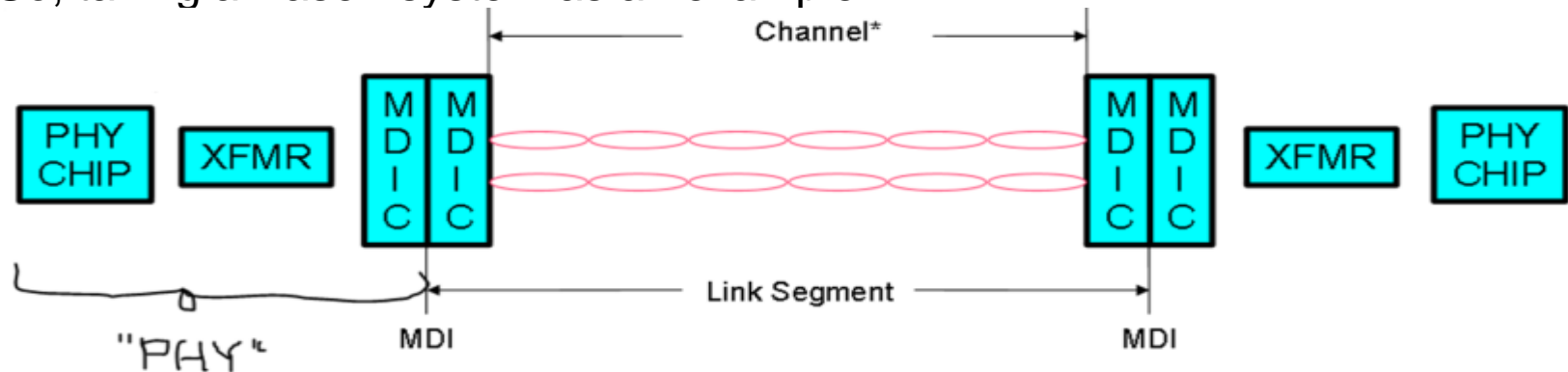
- This is just a simple highpass filter with pole at $1/(2RC) \Rightarrow$ for 100nF cap we have a pole at max frequency 7.957kHz
- As this is $<$ the max allowed pole location for any of the previous 3 quoted Droop Spec.s we could simply re-use one of these Droop specs and these would *not preclude* the I.S. resistor and capacitor requirement.

Interpretation of Objective 10

- Does this satisfy the I.S. requirements though ? It depends on the interpretation of Objective 10: 'Do not preclude working within an Intrinsically Safe device and system as defined in IEC 60079'
- Does this mean?
 - (i) Every transceiver chip intended for building an 802.3cg compliant PHY shall be able to accommodate external termination resistors 50Ohm/line and coupling capacitors 200nF/line
 - Or
 - (ii) It shall be possible to design a transceiver chip for building an 802.3cg-compliant PHY that can accommodate external termination resistors 50Ohm/line and coupling capacitors 200nF/line
- **Answer: It means (ii) above.** => a droop spec could be used to cover the I.S resistor/capacitor requirements however it must be noted that this could result in ***no silicon vendor producing a chip that can be used in an I.S. system (eg if they all elect to have on-chip termination).***
- My concern here is that people for whom I.S. is important may be taking interpretation (i) above and if this is what intended when introducing objective 10 then a Droop spec will not be adequate to cover these requirements.

Summary

- Simulations indicate the circuits proposed to ensure Intrinsic Safety do not pose any problems for system performance.
- There may however be some confusion about what our objective 10 means with this confusion centring on the meaning of the term 'PHY'
- As per Fig1-1 802.3-2015 (see slide 13) the PHY includes everything up to the MDI interface so that the entire signal path is comprised of the PHY + the link segment.
- So, taking a BaseT system as an example:



- So here the PHY includes the transceiver chip ('PHY chip') plus the transformer ('XFMR') plus the PCB traces etc up to the MDI interface

- Anything on the signal path and external to the PHY must be in the link segment
- My concern is that some contributors may be interpreting the PHY to be simply the transceiver IC. eg
http://www.ieee802.org/3/cg/public/adhoc/0117_cg_adhoc_IntrinsicSafety_r01.pdf:

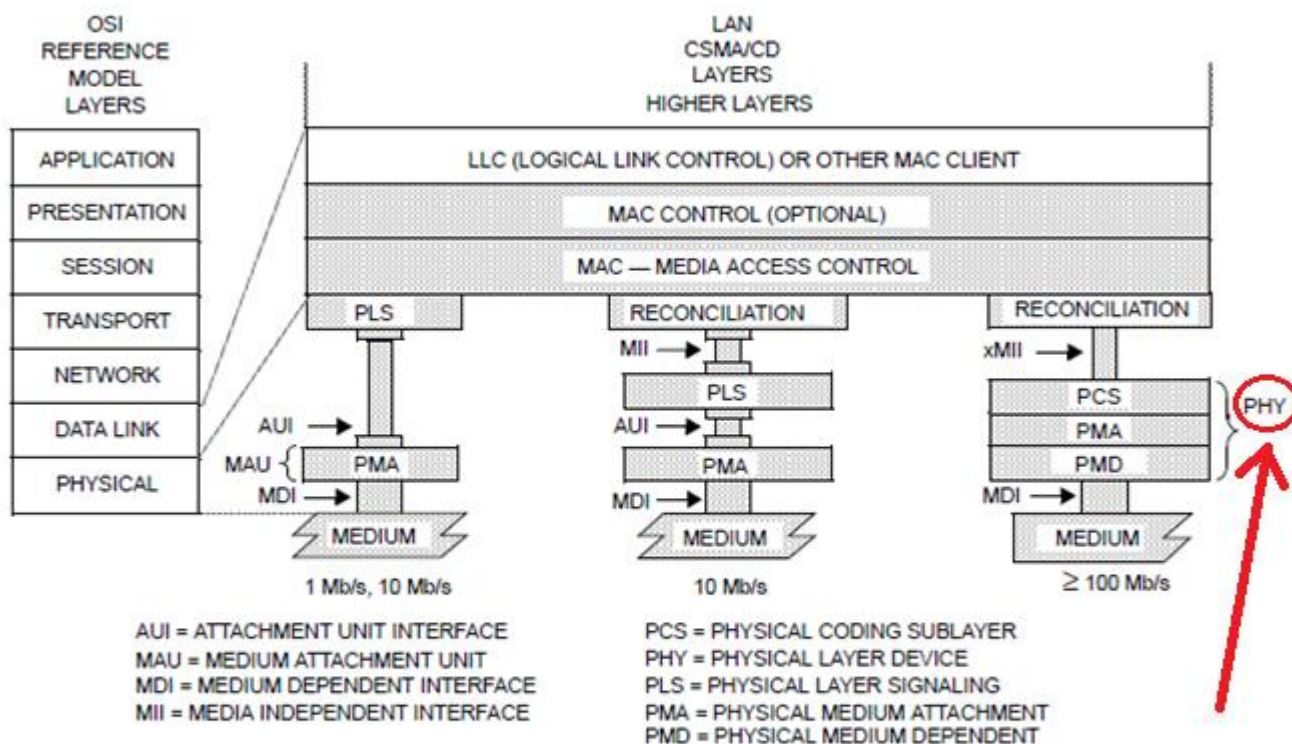
Baseline Proposal

Phy shall be able to work with:

- Optional Capacitive Coupling with Capacitors < 200 nF / Line
- Optional Signal Amplitude Reduction down to +/- 0.5 V
- Optional external Termination Resistors of 100 Ohms (= 50 Ohms / Line)

Fig1-1 802.3-2015

IEEE Std 802.3-2015
IEEE Standard for Ethernet
SECTION ONE

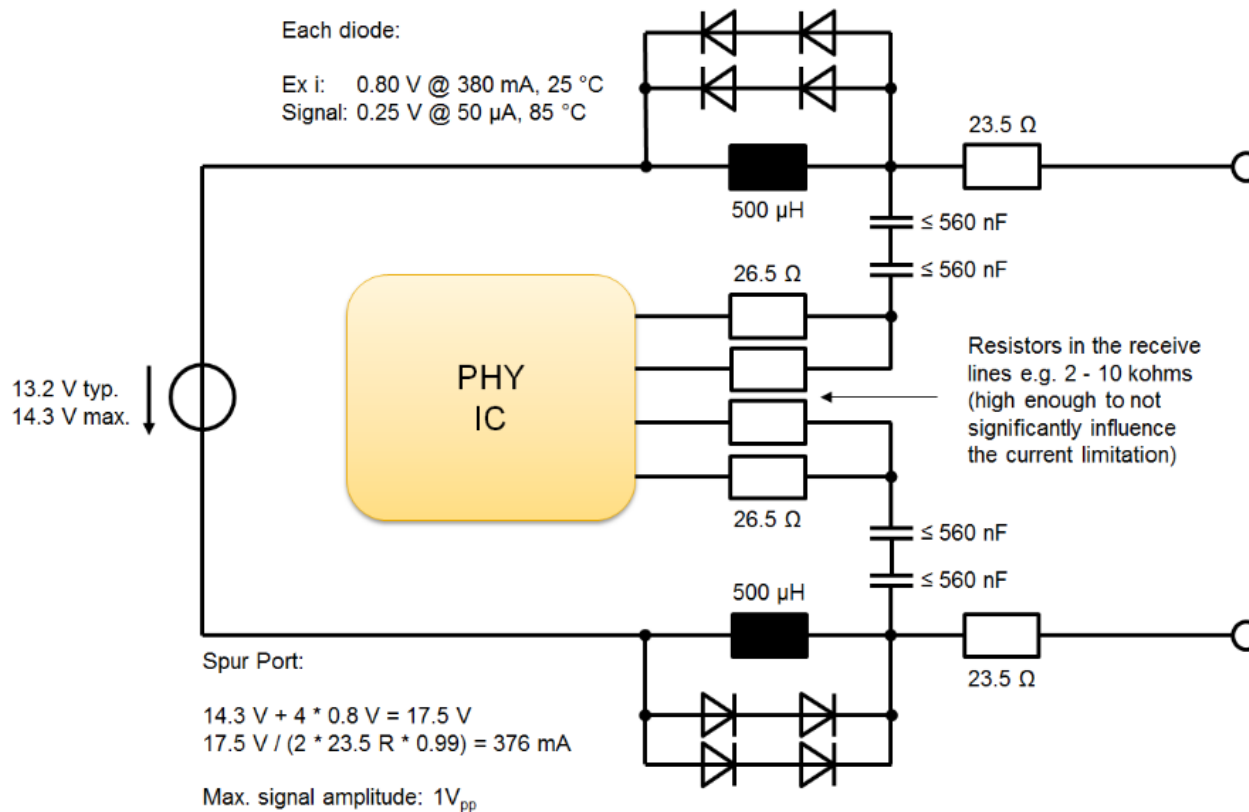


NOTE—In this figure, the xMII is used as a generic term for the Media Independent Interfaces for implementations of 100 Mb/s and above. For example: for 100 Mb/s implementations this interface is called MII; for 1 Gb/s implementations it is called GMII; for 10 Gb/s implementations it is called XGMII; etc.

Figure 1–1—IEEE 802.3 standard relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

Thank You

Exemplary Realisation



Baseline Proposal

Phy shall be able to work with:

- Optional Capacitive Coupling with Capacitors < 200 nF / Line
- Optional Signal Amplitude Reduction down to ± 0.5 V
- Optional external Termination Resistors of 100 Ohms (= 50 Ohms / Line)
- Optional capacitive coupling of cable shield on one or two ends of the cable (< 5 nF)

Remark: None of these features have to fulfill special reliability requirements. All safety relevant features have to be added by external circuits and are out of scope of this IEEE-project