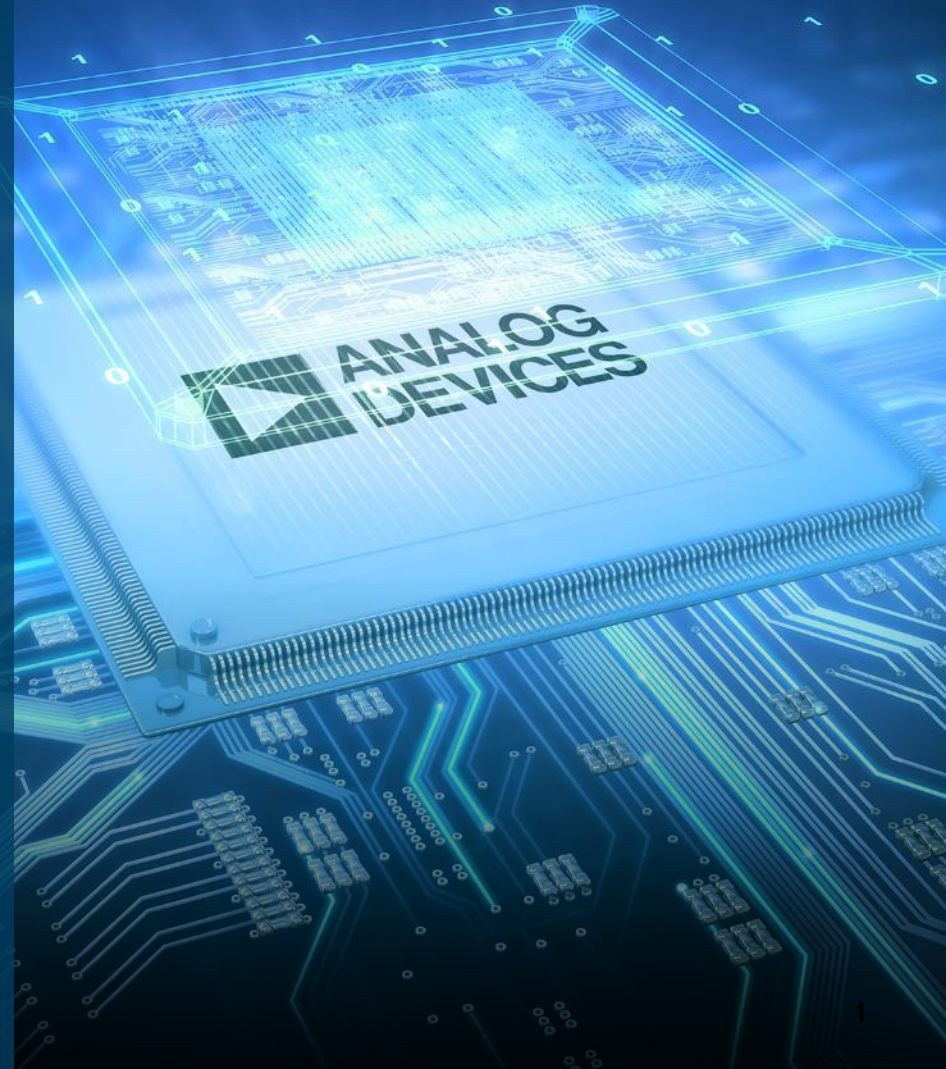




AHEAD OF WHAT'S POSSIBLE™

Simulations with Tonal Interference

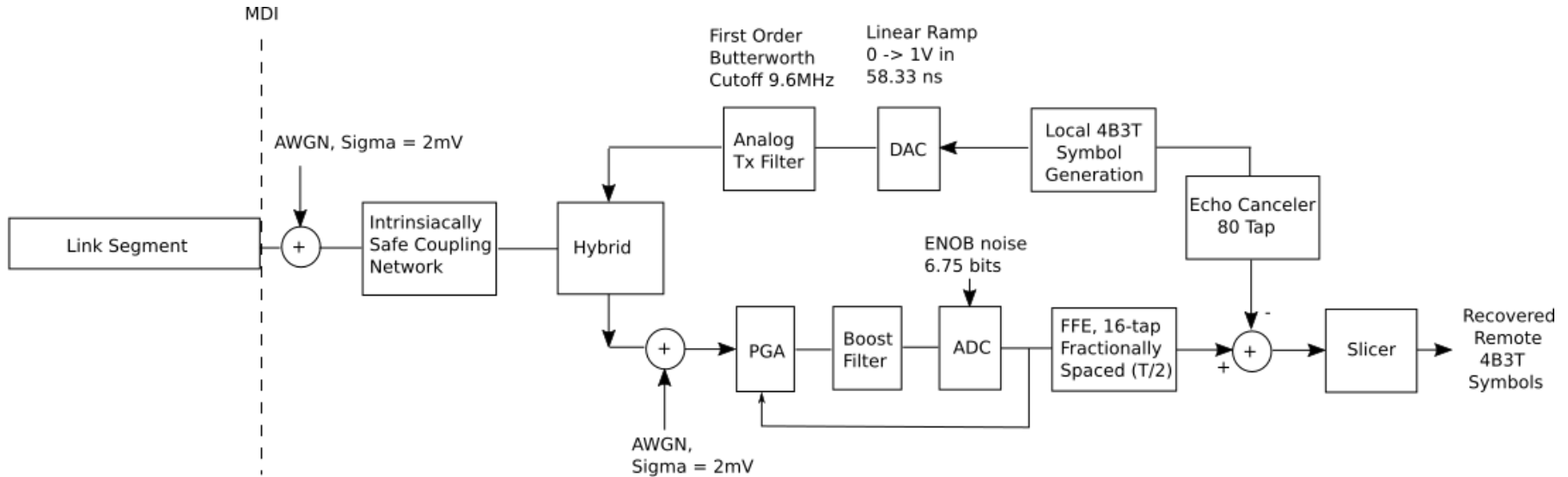
OISÍN Ó CUANACHÁIN



Background

- http://www.ieee802.org/3/cg/public/adhoc/ocuanachain_8023cg_02_0317.pdf presented the results of simulations using:
 - The baseline Link Segment I.L. and R.L. limits from proposal http://www.ieee802.org/3/cg/public/Jan2017/diminico_01a_0117.pdf
 - The symbol rate, modulation, 4B3T coding proposals and cable delay from http://www.ieee802.org/3/cg/public/Jan2017/Graber_10SPE_10_0117.pdf
 - 200nF/line coupling capacitors and 100 Ohm resistors proposed for Intrinsic Safety from http://www.ieee802.org/3/cg/public/adhoc/0117_cg_adhoc_IntrinsicSafety_r01.pdf
- The sim included two independent Additive White Gaussian Noise sources of PSD of -115.74 dBm/Hz per source (at 15Msps).
- Feedback was that Fieldbus typically assumes Tonal noise sources of 75mVpkpk
- This presentation summarizes the results of simulations with the existing AWGN noise sources and adding a new sinusoidal interferer signal whose Magnitude and Frequency are swept to assess the impact on performance.

Original Simulation Model:

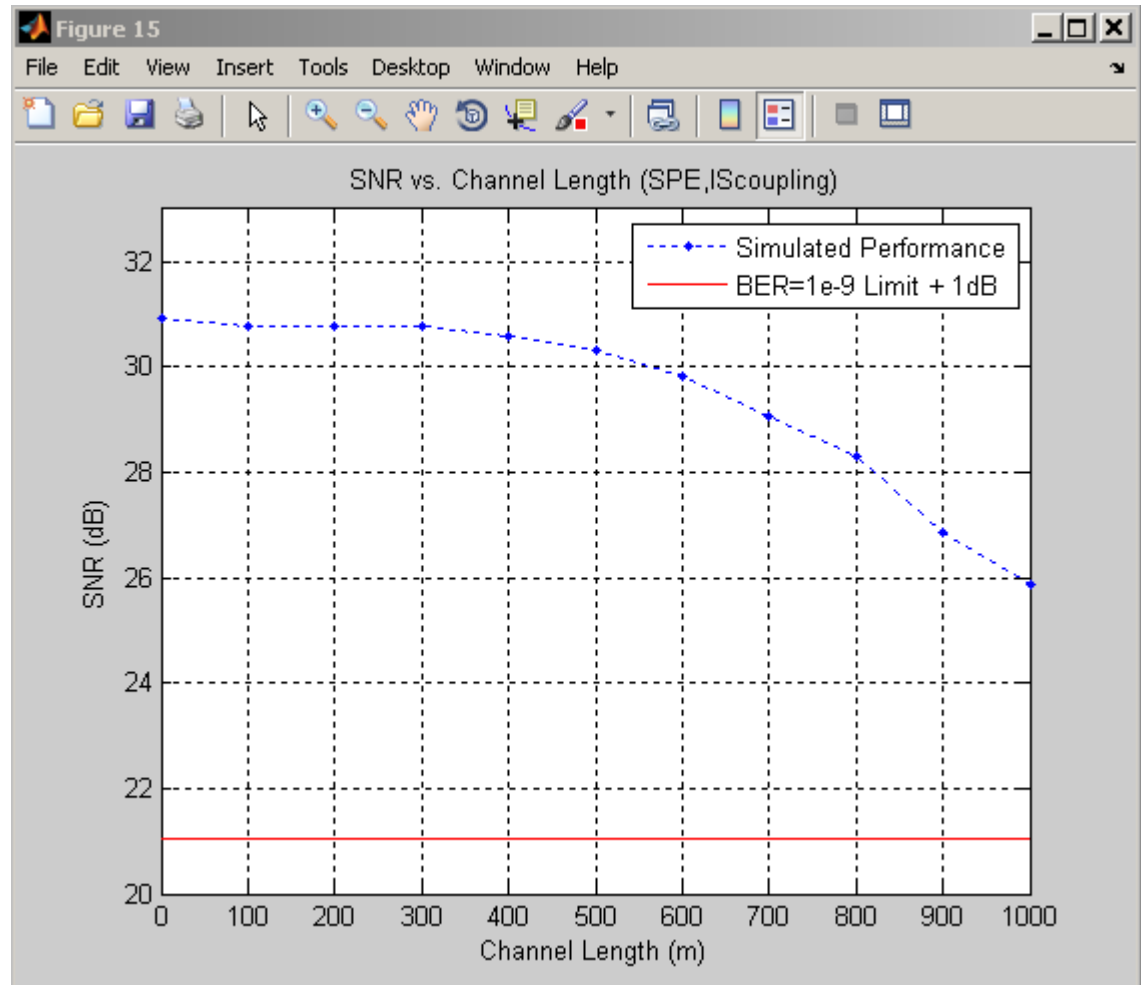


ADC: 8-Bit, 1V range, ENOB = 6.75 bits

*Note noise sources are specified in terms of the RMS voltage of the underlying analog noise signal. In the simulation these are sampled at the FFE rate (= 15Mps) giving noise PSD of -115.74 dBm/Hz per source.

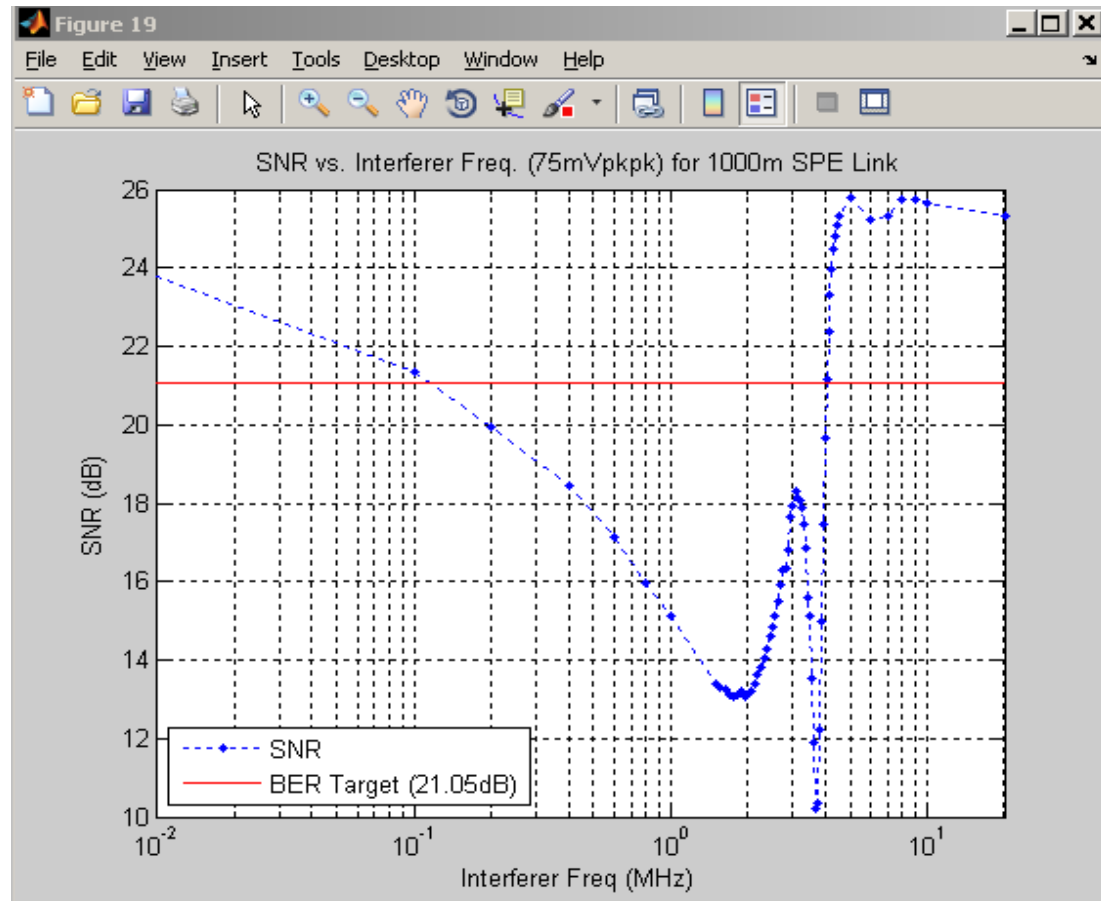
PHY parameters and Results:

- 16-tap T/2 fractionally-spaced Equalizer
- 80-tap Echo Canceler
- 8-bit 1V range ADC
- PGA with 19.2dB range
- I.S. 50-Ohm per line termination resistors and 200nF per line coupling capacitors
- Margin of 1.0dB added to SNR target to allow for unmodelled implementation losses



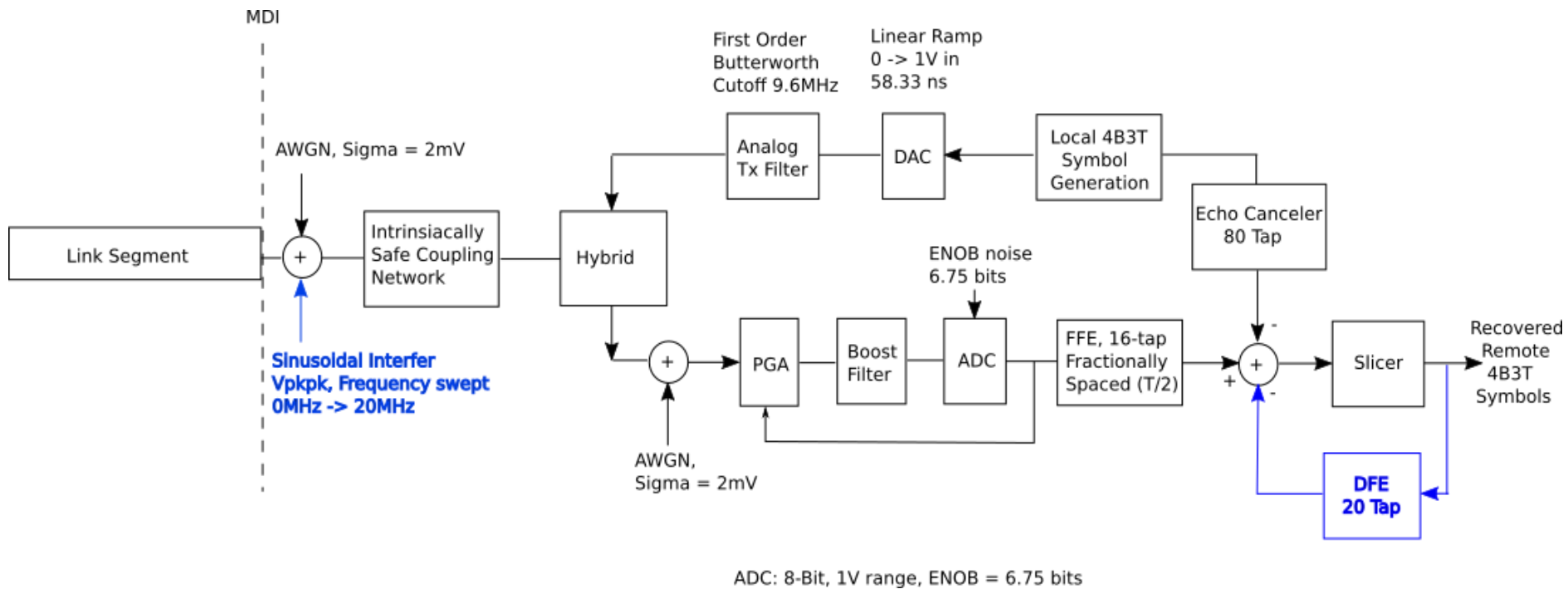
Adding Sinusoidal Interferer:

- Taking the 1000m channel, where the margin is smallest, a 75mVpkpk Sinusoidal Interferer is added and its Frequency is swept from 1kHz to 20MHz:



- Fail to meet SNR target for BER of 1e-9 for interferer frequency from ~100kHz -> ~4MHz

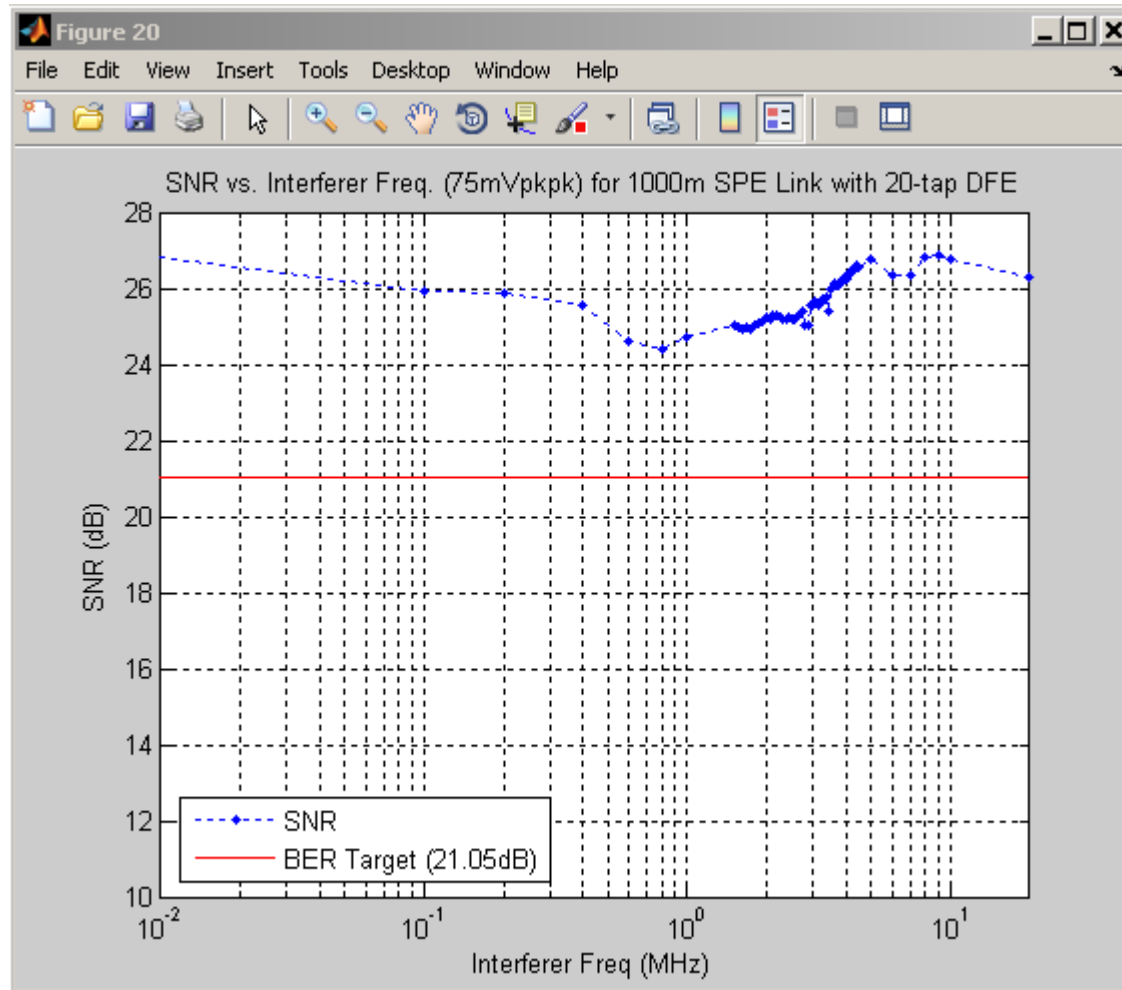
Add a 20-tap DFE to the receiver:



- Additions in **BLUE**

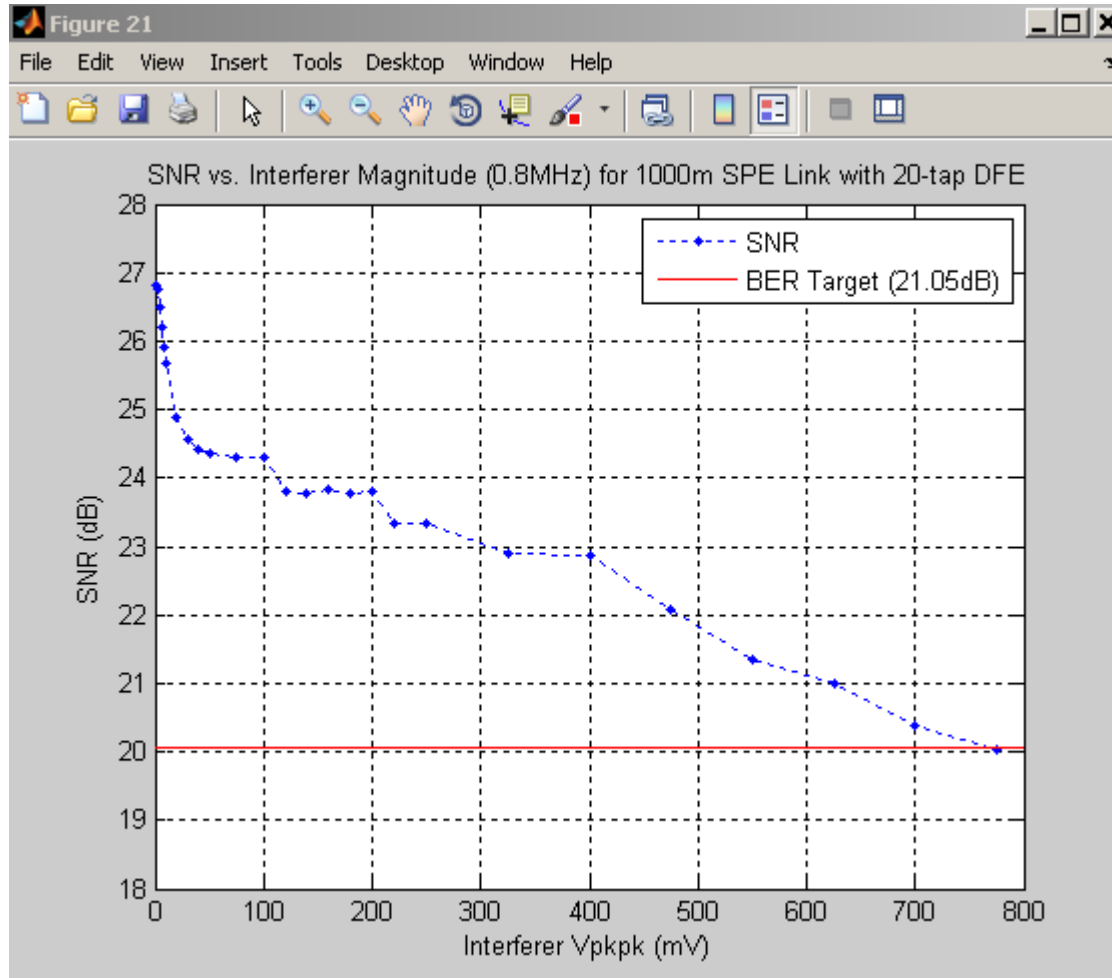
Performance at 1000m With 75mVpkpk Interferer

- The simulation results indicate that we should now meet the BER target with margin at all frequencies of interest:



Increasing the Magnitude of the Interferer

- 1000m Link with Interferer at worstcase frequency (0.8MHz) simulations indicate that we can hit the performance target even for Interferers significantly larger than 75mVpkpk:



Thank You

Reference