Cl **FM** *SC* **0** *P* **1** *L* # 175
den Besten, Gerrit NXP Semiconductors

Comment Type **TR** *Comment Status* **D** *late*

The clause title currently reads as: Physical Layer Specifications and Management Parameters for Greater Than 1 Gb/s Automotive Ethernet

SuggestedRemedy

Given that we will only specify 2.5/5/10Gbps in this clause, I recommend to replace "Greater than 1Gbps" with "2.5, 5, and 10 Gbps". If there will another Automotive Ethernet PHY beyond 1Gbps standardized in the future, it will get its own clause I expect.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
This name is required to be the name in the PAR, which it is.

Cl **FM** *SC* **0** *P* **2** *L* **3** # 176
den Besten, Gerrit NXP Semiconductors

Comment Type **ER** *Comment Status* **D** *late*

adds point-to-point 2.5 Gb/s Physical Layer
(PHY), 5 Gb/s Physical Layer (PHY) and 10 Gb/s Physical Layer (PHY) specifications and management
parameters for operation on automotive cabling in an automotive application.

SuggestedRemedy

adds 2.5Gbps, 5Gbps, and 10Gbps Physical Layer (PHY) specifications and management parameters for single balanced pair link segments and suitable for automotive applications

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
See Comment #164.

Cl **FM** *SC* **0** *P* **21** *L* **27** # 177
den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

2018comprehensive

SuggestedRemedy

2018 comprehensive (?)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
See comment #80.

Cl **1** *SC* **1.4.344a** *P* **22** *L* **34** # 178
den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

of1000 Mb/s

SuggestedRemedy

of 1000 Mb/s

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
See comment #108

Cl **30** *SC* **30** *P* **23** *L* **3** # 179
den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

[Notes for editors (not to be included in the published draft - not even D1.0!)□

SuggestedRemedy

Forgot to delete???

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
See comments #109 and #166.

Cl **44** *SC* **44.1.4.4** *P* **29** *L* **10** # 180
den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

64B/65B PCS

SuggestedRemedy

RS-FEC PCS (consistency with 10GBASE-T1)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
See comment #128.

Cl **44** *SC* **44.1.4.4** *P* **29** *L* **44** # 181

den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

on a single

SuggestedRemedy

over a single

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change: for transmission on a single
To: for transmission over a single

Cl **45** *SC* **45.2.1.192.1** *P* **33** *L* **16** # 182

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

1.2309.10:9

SuggestedRemedy

Wouldn't it better to out these bits at 7:6 instead (at start of lower byte) to allow reserved space in between for logical grouping of features in the future? In fact these bits are not really control but configuration bits.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Control bits and configuration bits are the same thing. Leaving the reserved block as one big block allows greater flexibility during draft development.

Cl **45** *SC* **45.2.1.192.1** *P* **33** *L* **30** # 183

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

Does a reset time of 0.5sec make sense given that the link start-up time should be within 100ms

SuggestedRemedy

Does 0.5s make sense? I would have expected a maximum value of 50ms rather than 500ms.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

A hard reset time of 0.5s is standard for ethernet PHYs in 802.3. Since that bit is a copy of a standard bit, which already has the reset time defined, changing the requirement for response would be problematic.

This is the same value as for 1000BASE-T1.

Cl **45** *SC* **45.2.1.192.3** *P* **34** *L* **5** # 184

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

"The data path of the MultiGBASE-T1 PMA, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or lowpower mode."

SuggestedRemedy

Is that really acceptable? I would expect a more tightly defined start-up time, like 100ms

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
See comment #82.

Cl **45** *SC* **45.2.1.194.1** *P* **36** *L* **9** # 185

den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

R.W

SuggestedRemedy

R/W

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change: R.W
To: R/W

Cl **45** *SC* **45.2.1.194.4** *P* **36** *L* **40** # 186

den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

up..

SuggestedRemedy

up.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
On page 36, line 45
Change: up..
To: up.

Cl **45** *SC* **45.2.1.197** *P* **38** *L* **20** # 187

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

This fine-grained SNR resolution seems overdone. Looking at other clauses with and SNR margin parameter (55,113,126), it seems that a 4 bit field with 0.5dB resolution is common.

SuggestedRemedy

Clause 113: "SNR_margin (4 bits). Represented by Octet 9<7:4>, which reports received decision point SNR margin in 1/2 dB steps. SNR_margin is relative to the SNR required for reception of LDPC-coded DSQ128 at an LDPC frame error ratio of less than 3.2 □ 10–9. The SNR_margin<7:4> four-bit values, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110 shall indicate the decision point SNR margin values of –1.5, –1, –0.5, 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5 dB, respectively. The value 0001 shall indicate a margin of –2 dB or less, and the value 1111 shall indicate 5 dB or more. Finally the value 0000 shall indicate that the SNR margin value is unknown."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

The resolution and range of measurement should be discussed. The resolution used here is the same used in all the MultiGBASE-T SNR margin registers for reporting. The 4 bit fields mentioned by the commenter are those reported during startup and are for a much coarser measurement done via infofields and optionally used by the PHY during startup, not for runtime monitoring.

Cl **45** *SC* **45.2.1.198** *P* **38** *L* **27** # 188

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

This fine-grained SNR resolution seems overdone. Looking at other clauses with and SNR margin parameter (55,113,126), it seems that a 4 bit field with 0.5dB resolution is common.

SuggestedRemedy

See previous comment

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Previous comment is #187

TFTD

The resolution and range of measurement should be discussed. The resolution used here is the same used in all the MultiGBASE-T SNR margin registers for reporting. The 4 bit fields mentioned by the commenter are those reported during startup and are for a much coarser measurement done via infofields and optionally used by the PHY during startup, not for runtime monitoring.

Cl **45** *SC* **45.2.1.199** *P* **38** *L* **34** # 189

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

This fine-grained signal power resolution seems overdone.

SuggestedRemedy

0.5dB resolution should be enough. Accuracy cannot be that high as analog front-end gain variability is not negligible.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The resolution and range of measurement should be discussed. The resolution used here is the same used in all the MultiGBASE-T power registers for reporting. The allowed range of transmit power is usually only 2 dB in the MultiGBASE-T PHYs, making 0.5 dB steps quite coarse. Currently there is only an upper bound on transmit power in 149.5.2.4, which makes it difficult to provide interoperable noise immunity. comments are invited to provide a lower bound in 149.5.2.4.

Cl **45** *SC* **45.2.3.72.2** *P* **40** *L* **31** # 190

den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

Was BASE-T1 intentionally strikes through here?

SuggestedRemedy

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Not a comment.

To answer the question, yes, it was changed so to say "transmitted by the PHY" without specifying the specific PHY.

Cl **45** *SC* **45.2.3.73** *P* **41** *L* **5** # 193

den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

"the remaining 4 octets are"

SuggestedRemedy

Replace by "there are 4 additional octets"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See Comment #87.

Cl **45** *SC* **45.2.3.73** *P* **41** *L* **6** # 191

den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

Reference to wrong registers 2328/2329 (which are reserved)

SuggestedRemedy

Should be 3.2318 and 2319

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See Comment #87.

Cl **45** *SC* **45.2.3.74** *P* **41** *L* **40** # 192

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

This bit shall self clear when register 3.2317 is read.

SuggestedRemedy

This condition is adapted by the paragraph below the table. Probably better to say: this bit shall self-clear on reading the last link partner AOM register. (and leave the more detailed explanation as is in the paragraph below).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change "This bit shall self clear when register 3.2317 is read" to "See 45.2.3.74.1 for self-clearing behavior". Note - this eliminates a 'duplicate shall', as well as provides the reference to the more complete behavior without relying on the names of the registers being the same.

Cl **45** *SC* **45.2.3.75** *P* **42** *L* **41** # 194

den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

"the remaining 4 octets are"

SuggestedRemedy

Replace by "there are 4 additional octets"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See Comment #87.

Cl **45** *SC* **45.2.3.75** *P* **42** *L* **41** # 195

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

"Register 3.2313.15
shall be cleared when register 3.2317 is read."

SuggestedRemedy

Confusing incomplete statement and redundant here as this belongs to the paragraph about register 2313. Suggest to remove this sentence.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This is for existing text in Clause 45. Removing the redundant text requires a Maintainance request which George Zimmerman will enter.

Cl **45** *SC* **45.2.3.77** *P* **43** *L* **48** # 196

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

"For MultiGBASE-T1 PHYs, register 3.2313.15 shall be
cleared when register 3.2321 is read."

SuggestedRemedy

Confusing incomplete statement and redundant here as this belongs to the paragraph about register 2313. Suggest to remove this sentence.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See Comment #86.

Cl **45** *SC* **45.2.3.78** *P* **44** *L* **21** # 198

den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

What is the reason to define new PCS control, status 1 and status 2 register, as they contain exactly the same fields as 1000BASE-T1. The OAM registers are reused (and extended). Why not do the same for these PCS registers?

SuggestedRemedy

Can we defined the PCS registers as BASE-T1 registers instead that can be reused for all speed grades?

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Commenter provides insuffficient information for remedy. At this time it is unknown whether the registers will remain identical to those in 1000BASE-T1. If the content remains the same as we approach working group ballot, commenter is invited to come with a proposal to merge the registers.

Cl **45** *SC* **45.2.3.78.1** *P* **44** *L* **44** # 197

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

"The control and management interface shall be restored to
operation within 0.5 s from the setting of bit 3.2322.15."

SuggestedRemedy

Does 0.5s make sense? I would have expected a maximum value of 50ms rather than 500ms.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

A hard reset time of 0.5s is standard for ethernet PHYs in 802.3. Since that bit is a copy of a standard bit, which already has the reset time defined, changing the requirement for response would be problematic.

Cl **45** *SC* **45.2.1.192.1** *P* **33** *L* **16** # 172

Wienckowski, Natalie General Motors

Comment Type **E** *Comment Status* **D** *late*

Typo in register number

SuggestedRemedy

Change 1.2304.10:9 to 1.2309.10:9

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.3** *P* **38** *L* **47** # 174
Wienckowski, Natalie General Motors

Comment Type **E** *Comment Status* **D** *late*

Editor's note for content added in D1.0 needs to be removed.

SuggestedRemedy

Remove Editor's note. The section was reviewed and other comments request updates to the text.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.3.80** *P* **46** *L* **44** # 207
Wienckowski, Natalie General Motors

Comment Type **E** *Comment Status* **D** *late*

Incorrect Register number in Table 45-244e

SuggestedRemedy

In table 45-244e, change 3.2306.x to 3.2324.x in all rows.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **78** *SC* **78.2** *P* **50** *L* **49** # 199
den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

What is the tolerance on these time values? There is zero margin between min and max.

SuggestedRemedy

As these are actually an integer number of symbol periods (or blocks or frames), it might be better to specify them that way, without tolerance window.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Jim Graba confirmed during D1.0 creation that these should be the same value.
"In 802.3bp we started Sleep if the last 80B/81B block in a frame was an LPI control character. This was William Lo's innovation 4 years ago. It reduced LPI chattering. Then Ts min and max are equal. See 802.3bp (1000BASE-T1) table 78-2."

I carried this forward to 802.3ch. So yes this means Ts min and max are equal.

However, Tq is not the same for both values for 1000BASE-T1.

Cl **125** *SC* **125.1.4** *P* **60** *L* **30** # 200
den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

"using 64B/65B encoding"

SuggestedRemedy

Shouldn't that be "Reed-Solomon" given that the BASE-T flavors mention LDPC?

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See Comment #145.

Cl **125** *SC* **125.1.4** *P* **60** *L* **38** # 201
den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

"using 64B/65B encoding"

SuggestedRemedy

Shouldn't that be "Reed-Solomon" given that the BASE-T flavors mention LDPC?

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See Comment #145.

Cl **149** *SC* **149.1.3.1** *P* **65** *L* **22** # 202

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

"the PCS receives four XGMII data octets provided by two transfers on the XGMII service interface on TXD<31:0>, and groups ..."

SuggestedRemedy

It seems that four should be eight in this sentence. Alternative it could read: "the PCS receives four data octets per XGMII transfer, and groups ..."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

The wording is correct as is (because it goes on to say "and groups two of them"), but is is awkward. Use the wording from clause 126 in 802.3-2018. Change "In the transmit direction, in normal mode, the PCS receives four XGMII data octets provided by two transfers on the XGMII service interface on TXD<31:0>, and groups two of them into 64-bit blocks (eight octets)." to "In the transmit direction, in normal mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers."

Cl **149** *SC* **149.1.3.4** *P* **66** *L* **50** # 203

den Besten, Gerrit NXP Semiconductors

Comment Type **E** *Comment Status* **D** *late*

"detect the presence of the other, validate link, and"

SuggestedRemedy

Sentence reads strange: "validate link" what does this mean here?

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

TFTD. Text is copied from Clause 97.

Cl **149** *SC* **149.1.5** *P* **67** *L* **35** # 204

den Besten, Gerrit NXP Semiconductors

Comment Type **T** *Comment Status* **D** *late*

"All 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHY implementations are compatible at the MDI and at the XGMII, if implemented."

SuggestedRemedy

This sentence suggests that a 2.5GBASE-T1 PHY implementation is compatible with a 10GBASE-T1 PHY implementation at MDI and XGMII. I expect this sentence was meant to state that compatility only applies for the same speed grade.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Commenter provides insufficient information for remedy. Compatibility does not mean interoperable. It means they use the same interfaces, which is what this subclause is about. Same wording is used in this subclause of clause 126 for 2.5G/5GBASE-T PHYs.

Cl **149** *SC* **149.3.2.3** *P* **92** *L* **8** # 206

Zimmerman, George CME:ADI,Aquantia,AP

Comment Type **T** *Comment Status* **D** *late*

LATE COMMENT - Informative descriptive text for the PCS Receive function is listed as "TBD"

SuggestedRemedy

Replace line 8 "Normal PCS Receive function operation TBD." with text in zimmerman_3ch_01_0119.pdf. Editorial license to highlight or remove highlighting, and adjust text per other decisions in this meeting.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **149** *SC* **149.4.5** *P* **131** *L* **2** # 173

Wienckowski, Natalie General Motors

Comment Type **E** *Comment Status* **D** *late*

Editor's note for content added in D1.0 needs to be removed.

SuggestedRemedy

Remove Editor's note, accpeting Figure 149-21

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.