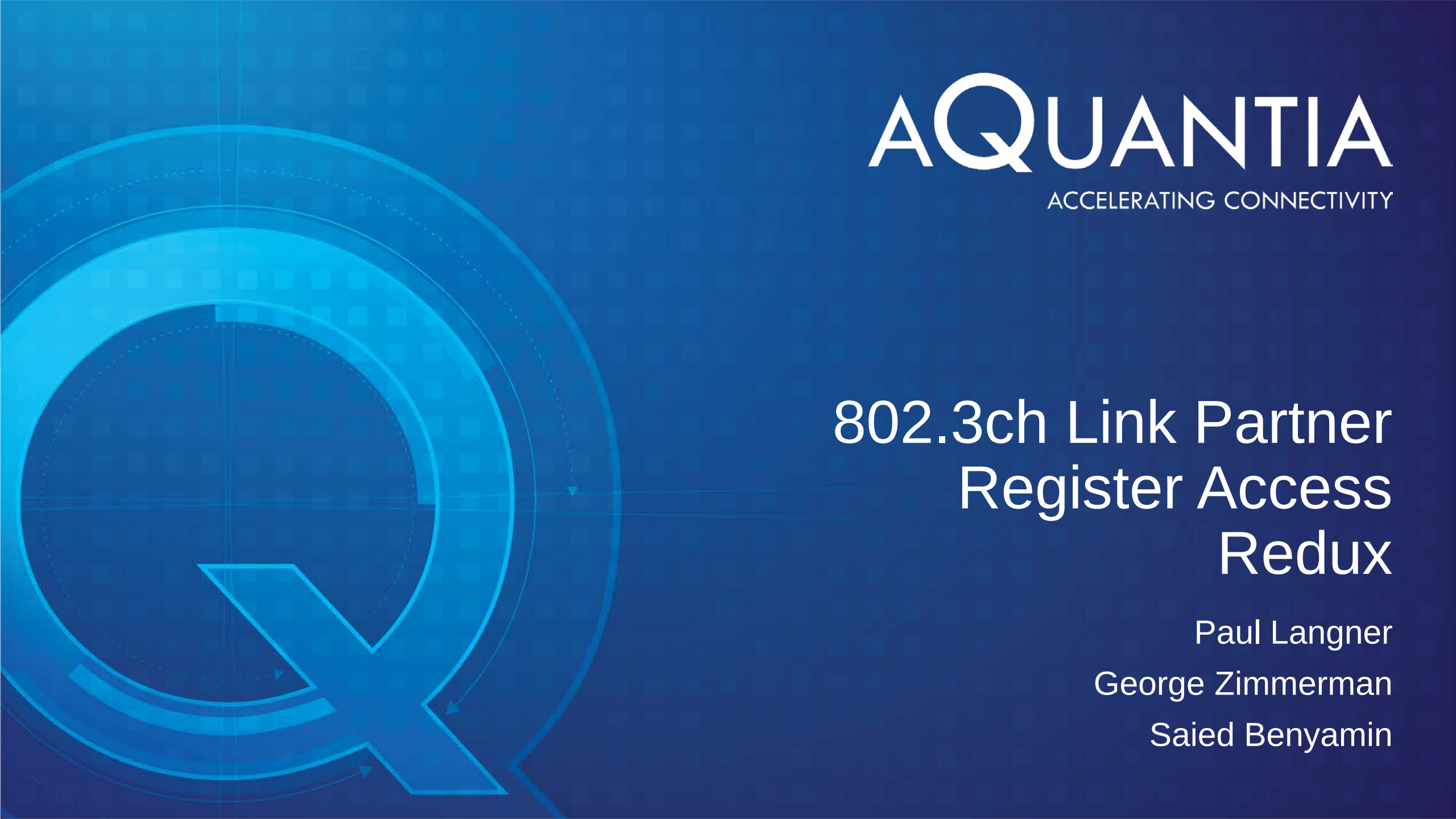

802.3ch Link Partner Register Access Redux

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Problem

- Construct a standard HW access mechanism that utilizes the 10 bit field “formerly known as OAM” that occurs once per 320ns in link mode and some less-frequent interval in EEE mode to allow reliable reading of link-partner MDIO registers within the noise environment
- Framework:
  - Noise environment is low-level Gaussian, with a 60-110ns burst every 100us
  - Data mode is protected with RS1024 (360, 326) with pseudo-noise (PN) scrambling so BER < 10^{-12} and scrambler takes care of spectral issues
    - Channel BW is 10-bits every 320 ns, so channel bit rate is 31.25 Mb/s
  - EEE mode is running unprotected with 10-bit field with a transmit interval of roughly every 32 frames and additive side-stream scrambler, so again no spectral issues
    - Channel BW is ~1/32 data mode = 10 bits every 10.24 us = ~0.975 Mb/s
    - Burst error environment can eliminate one 10-bit field, therefore need a code to protect against this, with a frame size less than 100us

Additional Tweak from Previous Presentation

- As was correctly pointed out, there can be only one information consumer per latching bit (i.e. you don't want contention between local and remote reads)
- Since there are a very limited number of latching bits defined in the register map (6 in total), the suggestion is:
  1. Remote reads do not affect latching bits in register space
  2. Shadow the latching bits in the remote status register (currently 11 free bits) where the remote read will clear the latching bits
  3. If desired shadow this register into the local space

PMA status	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL
PCS status	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
PCS status	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
PCS status	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
PCS status	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LH
PCS status	Latched block lock	1 = PCS has not lost block lock 0 = PCS has lost block lock	RO/LL

- Also changed "interrupt" to reflect OAM state change

Previous Presentation

Design Constraints

- Need to be able to send MMD, Address, and Command
  - Need a Transaction Number to distinguish read operations
  - Need an interrupt bit to reflect state changes in any OAM bits
    - Purpose is to avoid having to poll this status register
- Command list should include:
  - Idle
  - Read
  - Read response
- Error correction should be able to fix 10 bits in the frame, so need 2x 10bits for ECC

Proposed frame structure

1	4	4	5	16	20	= 50 bits
INT	Trans ID	CMD	MMD	Address	Parity	

- Need to align the link-partner register access with data mode RS frames
  - Need it to be a multiple of 10-bits: so given the above, we need a 5 x 10 frame with RS1024(5,3) ECC
  - Use incremental search to find frame, as there are only 5 starting positions
    - Disallow CMD = 0 as “all-zero” payload produces zero parity, and framing will not work
- Example read times:

1. Data Mode: Read request round-trip takes:
   - 320ns x 5 = 1.6us transmit + 0.5us decode + 3.2 us read register* + 320ns x 5 = 1.6us response = 6.9us
2. EEE Mode: Read request round-trip takes:
   - 320ns x 32 x 5 = 51.2uS transmit + 0.5us decode + 3.2 us read register + 320ns x 32 x 5 = 51.2us response = 106.1us

* Typical MDIO transaction time at 10 MHz = ~3.2us

Details

- INT = 1 indicates a bit in the OAM register changed state
- TRANS ID (transaction ID) is a 4 bit hardware counter that tracks requests and responses
  - Each PHY has its own rolling 4-bit counter and matches read transaction IDs against read-response transaction IDs
  - If a read-response not seen within TBD link partner register access frames, the read is re-issued
- CMD is a 4-bit field indicating the action for the register access frame
  - 0 = Invalid, 1 = Idle, 2 = Read
  - 3 = Read response, 4-15 = Reserved
- MMD is MMD to read
- Address is Address within the MMD to read

Link Partner Register Access Transactions

	1	4	4	5	16	20
Idle	INT	0	1	00	0000	Parity

	1	4	4	5	16	20
Read	INT	Req. trans ID	2	MMD	Address	Parity

	1	4	4	5	16	20
Read Response	INT	Req. trans ID	3	00	Data	Parity

Register Definitions

Link Partner Register Access Control Register 1:

- Bit 15: Read-Only: Link Partner Interrupt
  - When set indicates that bit in the OAM register changed state
- Bit 14 – Bit 13: Reserved
- Bit 12 – Bit 8: Read / Write: Link partner target MMD
  - The MMD to access in the link partner
- Bit 7 – Bit 2: Reserved
- Bit 1: R/W: Link partner access command
  - 0 = Read, 1 = Reserved
- Bit 0: R/W, Clear on Completion: Execute Command.
  - When set, this executes the command indicated in Bit 1 (read is only option), and is cleared by hardware when the command is complete – i.e. the read result is available for reading

Register Definitions (continued)

Link Partner Register Access Address:

- Bit 15 – Bit 0: Read / Write: Link partner target address
  - The address within the MMD specified to access in the link partner

Link Partner Register Access Data:

- Bit 15 – Bit 0: Read-Only: Link partner data
  - The data returned from the link partner as the result of a read command

Example Usage

Read Example:

1. Write “Link Partner Register Access Address” with desired address to read
2. Write “Link Partner Register Access Control Register 1” with the desired MMD in bits 12:8 and 1 in bit 0
3. Poll “Link Partner Register Access Control Register 1” bit 1 to clear
4. Read the result in “Link Partner Register Access Data”

Interrupt Example:

1. Periodically poll “Link Partner Register Access Control Register 1” bit 15*
2. Read link partner interrupt status register tree to find the source of the interrupt

* Or connect this bit into the local interrupt tree, so polling is not required

Thank you.