Delay Constraints

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Minimum Theoretical Delay

- Assuming circuits run with zero delay, the following delays are required by the Reed Solomon algorithm
- Transmit:
  - Need to buffer data to prevent underflow when transmitting the OAM symbol and parity symbols. Define t_t as the time required to transmit the OAM symbol and parity bits for one RS frame
- Receive:
  - Need to buffer entire RS frame before error correction. Define as t_r as the time required to receive one RS frame
- Let L = interleave (1, 2, 4) then the minimum delay due to algorithm
  - $L * (t_t + t_r)$

Additional Budget For Circuit Implementation Delays

- Allow budget of 200% of RS frame time for everything else (2.0 * t_r)
  - FEC error correction, signal processing, PCS/PMA delay, etc.
  - Should be plenty of time for all implementations of decoder (parallel, serial)

- Take L* (t_t + t_r) + 2.0 * t_r and round up to the nearest pause_quanta (512 bits)

Table 149–13—Delay Limits

Mode	Interleave	Bit times	Pause Quanta	ns
2.5GBASE-T1	1	10240	20	4096.0
5GBASE-T1	1	10240	20	2048.0
5GBASE-T1	2	13824	27	2764.8
10GBASE-T1	1	10240	20	1024.0
10GBASE-T1	2	13824	27	1382.4
10GBASE-T1	4	20480	40	2048.0

THANK YOU