PHY Control

William Lo, Axonne Inc.

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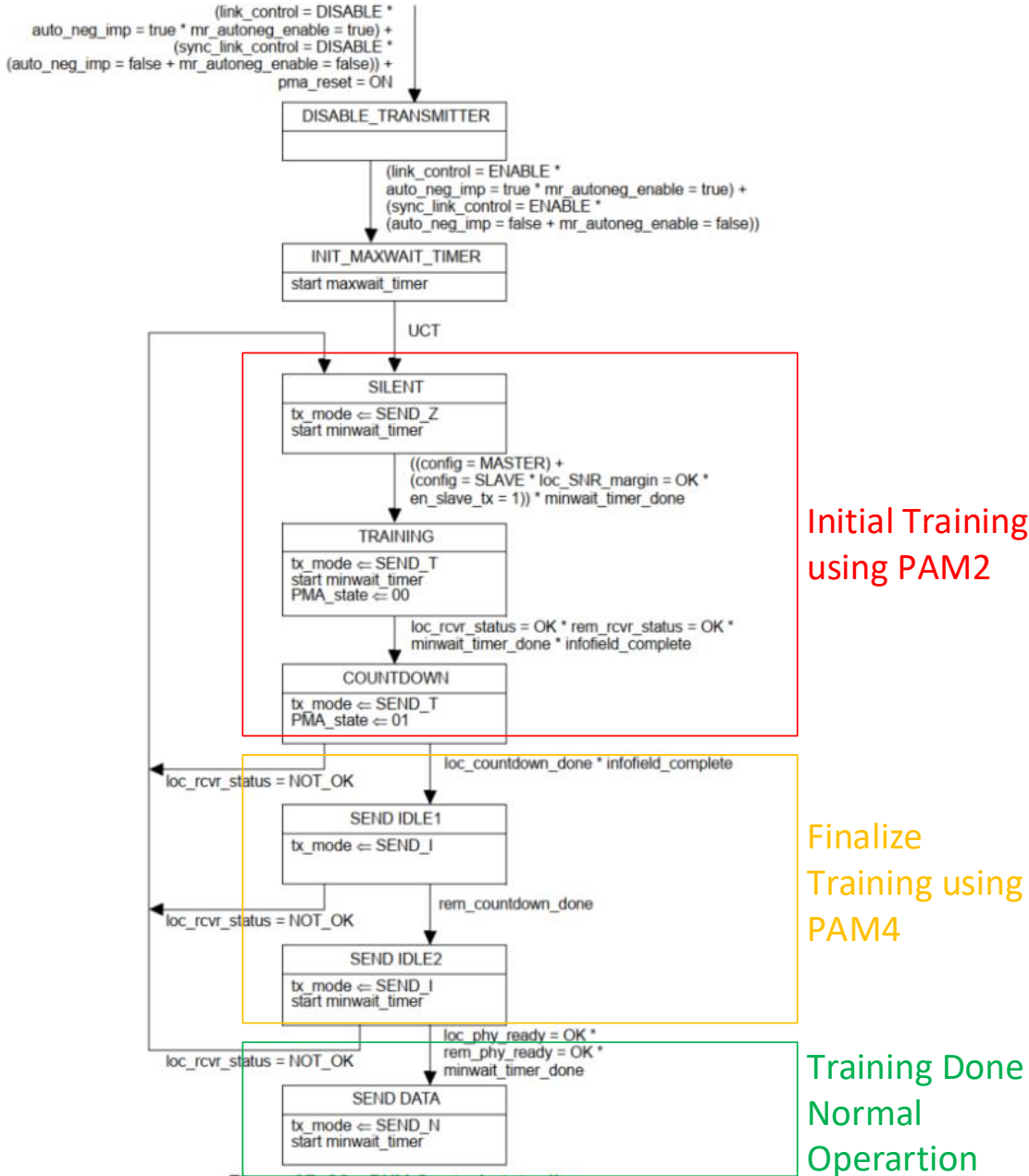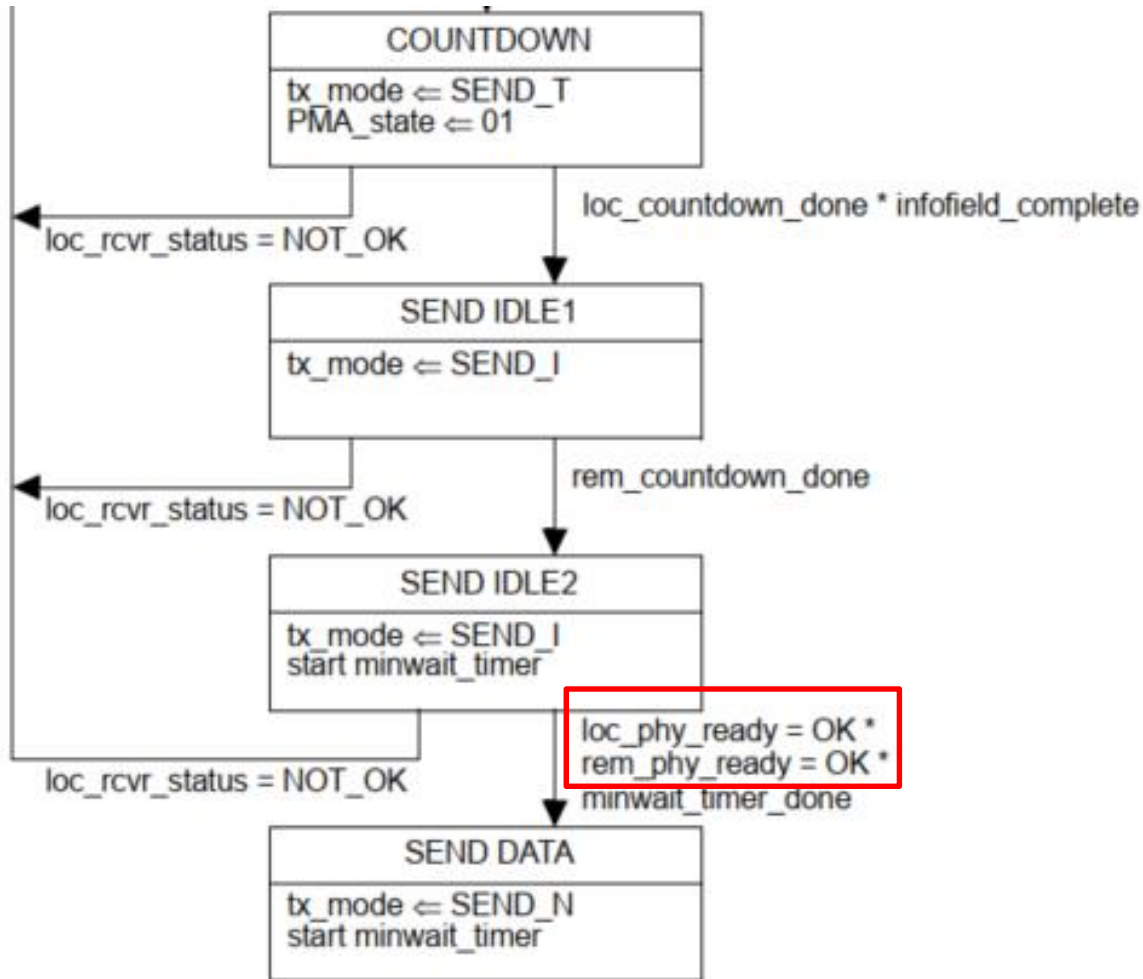
Steps in PHY Control

Figure 97–26—PHY Control state diagram

- 1000BASE-T1 PHY Control State Diagram without modifications.

- When finalizing training in PAM4 want to make sure we don't send data. Only send idles

loc_phy_ready and rem_phy_ready

- *_phy_ready from both PHYs must be OK to safely enter normal operation.
- Currently no way to exchange using 64/65 encoder as defined.

Proposal

- Define training idle control code in 64/65 encoder
- loc_phy_ready = NOT_OK send /TI/,   = OK send /I/

Control character	Notation	XGMII control codes	MGBASE-T1 control codes	MGBASE-T1 O code
idle	/I/	0x07	0x00	
training idle	/TI/	0x07	0x09	
LPI	/LI/	0x06	0x06	
start	/S/	0xFB	Encoded by block type field	
terminate	/T/	0xFD	Encoded by block type field	
error	/E/	0xFE	0x1E	
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
reserved0	/R/	0x1C	0x2D	
reserved1		0x3C	0x33	
reserved2	/A/	0x7C	0x4B	
reserved3	/K/	0xBC	0x55	
reserved4		0xDC	0x66	
reserved5		0xF7	0x78	
Signal ordered set	/Fsig/	0x5C	Encoded by block type field plus O code	0xF

THANK YOU