PHY Control

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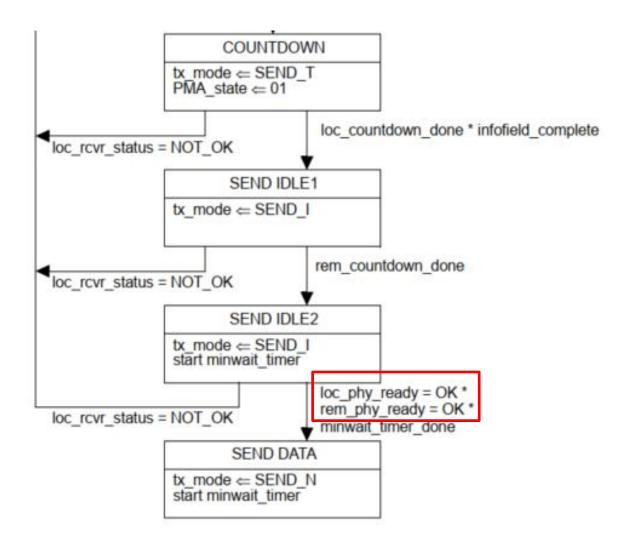
(link control = DISABLE * auto neg imp = true * mr autoneg enable = true) + (sync link control = DISABLE (auto neg imp = false + mr autoneg enable = false)) + DISABLE TRANSMITTER (link control = ENABLE * auto_neg_imp = true * mr_autoneg_enable = true) + (sync link control = ENABLE * (auto neg imp = false + mr autoneg enable = false)) INIT MAXWAIT TIMER start maxwait timer UCT SILENT tx mode ← SEND Z start minwait timer ((config = MASTER) + (config = SLAVE * loc SNR margin = OK * en slave tx = 1)) * minwait timer done **Initial Training** tx mode SEND T using PAM2 start minwait timer PMA state € 00 loc rcvr status = OK * rem rcvr status = OK * minwait timer done * infofield complete COUNTDOWN tx_mode ← SEND_T PMA state ← 01 loc countdown done * infofield complete loc rcvr status = NOT OK SEND IDLE1 **Finalize** Training using rem countdown done loc_rcvr_status = NOT_OK PAM4 SEND IDLE2 start minwait timer loc phy ready = OK * rem phy ready = OK loc rcvr status = NOT OK **Training Done** minwait timer done SEND DATA Normal tx_mode ← SEND_N start minwait timer Operartion Figure 97–26—PHY Control state diagram

Steps in PHY Control

- 1000BASE-T1 PHY Control State Diagram without modifications.
- When finalizing training in PAM4 want to make sure we don't send data. Only send idles



loc_phy_ready and rem_phy_ready



- *_phy_ready from both PHYs must be OK to safely enter normal operation.
- Currently no way to exchange using 64/65 encoder as defined.

Proposal

- Define training idle control code in 64/65 encoder
- loc_phy_ready = NOT_OK send /TI/, = OK send /I/

| Control character | Notation | XGMII control codes | MGBASE-T1 control codes | MGBASE-T1 O code |
|----------------------|--------------|------------------------|---|---------------------|
| idle | / I / | 0x07 | 0x00 | |
| training idle | /TI/ | 0x07 | 0x09 | |
| LPI | /LI/ | 0x06 | 0x06 | |
| start | / S / | 0xFB | Encoded by block type field | |
| terminate | /T/ | 0xFD | Encoded by block type field | |
| error | /E/ | 0xFE | 0x1E | |
| Sequence ordered set | /Q/ | 0x9C | Encoded by block type field plus O code | 0x0 |
| reserved0 | /R/ | 0x1C | 0x2D | |
| reserved1 | | 0x3C | 0x33 | |
| reserved2 | /A/ | 0x7C | 0x4B | |
| reserved3 | /K/ | 0xBC | 0x55 | |
| reserved4 | | 0xDC | 0x66 | |
| reserved5 | | 0xF7 | 0x78 | |
| Signal ordered set | /Fsig/ | 0x5C | Encoded by block type field plus O code | 0xF |

THANK YOU

