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FEC/Framing/Modulation for 10GBASE-T1 PHY

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Decision Factors for Selection of 10G PHY proposals

- We've focused so far on modulation only, but modulation doesn't make the whole PHY

  - The top factor in modulation selection is the target performance feasibility

    - Do the selected modulations deliver the target performance (Data rate & BER) over the target medium?

    - Presentations from May 2018 show 2 and 2.5b/symbol give best performance

  - Simulations show similar SNR performance between PAM proposals

    - PAM-4 best for in-band NBI and impulse immunity in this range: (Tu, Pandey, Souvegnier agree)

    - We've seen this before: < 1 dB differences lie in implementation, mapping to framing & coding

- Next decision factors power & cost:

  - Modulations proposed have similar complexity – everyone has a favorite for different reasons

    - None are saying the differences are large

  - Re-use of existing Ethernet technology impacts power & cost as well

- This presentation discusses an approach to Framing & Coding relative to noise and modulation

PAM modulations are close in performance

10G PHY: Salz SNR Analysis – 15m Cable

15m Cable	PAM2	PAM3	PAM4	PAM5	PAM6	PAM8	PAM16
Baud Rate (GBaud)	11.2	7.5	5.6	5.0	4.5	3.7	2.8
Nyquist Freq. (GHz)	5.6	3.75	2.8	2.5	2.2	1.8	1.4
IL@Nyquist (dB)	46.9	35.7	29.7	27.5	25.7	22.9	19.3
RL@Nyquist (dB)	12.0	12.0	12.5	13.0	13.5	14.2	15.3
Ideal SNR Margin (dB)	14.3	18.5	19.3	19.1	18.6	17.5	13.7
Echo cancellation (dB)	17.0	24.3	26.9	28.2	28.8	29.5	30.0

Pandey_3ch_01c_0518.pdf

NXP

Effect of ADC Power vs. ENOB on 10Gbps SNR Margin

SNR Margin vs. Baud Rate for ADC with Fixed Power
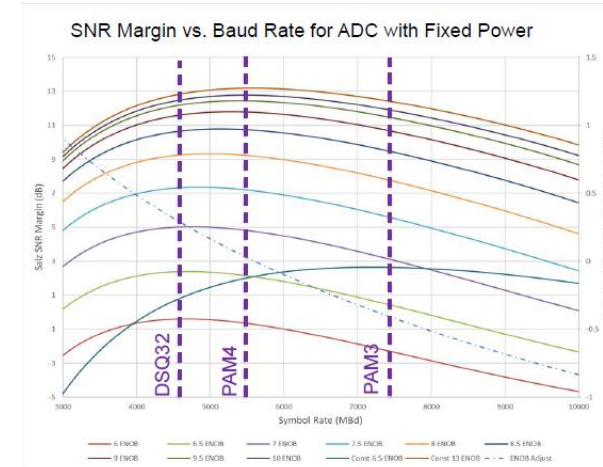
- ADC with Constant Power
  → Higher ENOB with Lower Baud
  $ENOB2 = ENOB1 + \log_2(Baud1/Baud2)$
  PAM3: 6.1ENOB → PAM4: 6.5ENOB
  → DSQ32: 6.8ENOB
- → ADC power fixed at 6.5ENOB/5.5Gbaud

	DSQ32	PAM4	PAM3
SNR Margin:	2.2dB	2.1dB	0.6dB

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Farjadrad_3ch_01_0518.pdf

SNR Margin to Uncoded SER

| Modulation	Bits/Sym	Symbol Rate (MBaud)	Uncoded SNR @1e-12 SER (dB)	Cat8 Salz SNR (dB)	Cat7a Salz SNR (dB)	Cat8 Margin (dB)	Cat7a Margin (dB)
3B2T	3/2	7500	21.8	30.3	24.4	8.5	2.6
DSQ-8	3/2	7500	21.1	30.3	24.4	9.2	3.3
PAM-4	2/1	5625	24.0	34.6	29.1	10.6	5.1
32-Cross	5/2	4500	27.1	37.5	32.3	10.4	5.2
DSQ-32	5/2	4500	27.3	37.5	32.3	10.2	5.0
PAM-8	3/1	3750	30.4	39.6	34.6	9.2	4.2
DSQ-128	7/2	3200	33.4	41.3	36.5	7.9	3.1

Souvignier_3ch_01c_0518.pdf

- Presentations from multiple PHY vendors agree, SNR analyses for PAM4, DSQ or Cross 32 and PAM5 are well within 1dB of each other.
  - Implementation losses will dominate
  - Higher density constellations are more vulnerable to RF interference and implementation noise contributions

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Automotive Error Sources

- Narrowband RF Interference
  - Single tones: 1 MHz – 5 GHz at 100V/m (ISO 11452-2)

- Alien crosstalk/channel AWGN
  - Negligible, dominated by receiver noise

- Burst Error Sources
  - Transient Impulse (ISO 7637-3)
    - Duration <50nsec and Period > 100us, similar to Chini_Tazebay_3bp_01a_0114.pdf
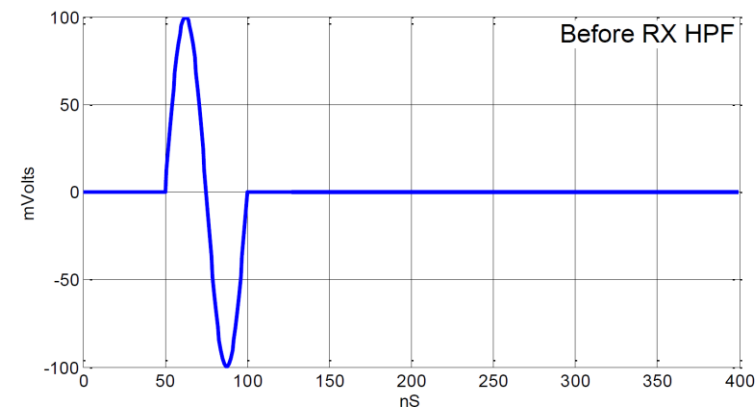
NBI Immunity Simulation Results
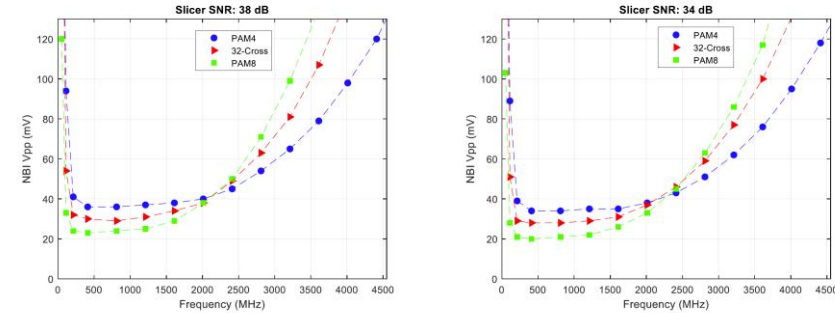
- At lower frequencies, NBI immunity increased by ~2.5dB each from PAM8 to 32-Cross to PAM4
- At higher frequencies, denser constellations have superior immunity due to lower bandwidth and analog low pass filtering
- IEEE 802.3ch Task Force– May 2018.

Chini_Tazebay_3bp_01a_0114.pdf

Transient Noise Model at Receiver

- One cycle of a 20MHz sinusoidal signal with magnitude of 100mV is suggested for system analysis of transient noises.

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Narrowband RF Interference

- ## RF Interference Coupling to Differential Pairs
  - BCI 1MHz – 400MHz (ISO11452-2/ OEM specs)
    - BCI used to cover lower frequencies
  - ALSE 80MHz - 5GHz (ISO11452-2/ OEM specs)
    - Use actual antenna radiating an electric field at the cable
    - ISO spec defines an electric field up to 100V/m at the cable
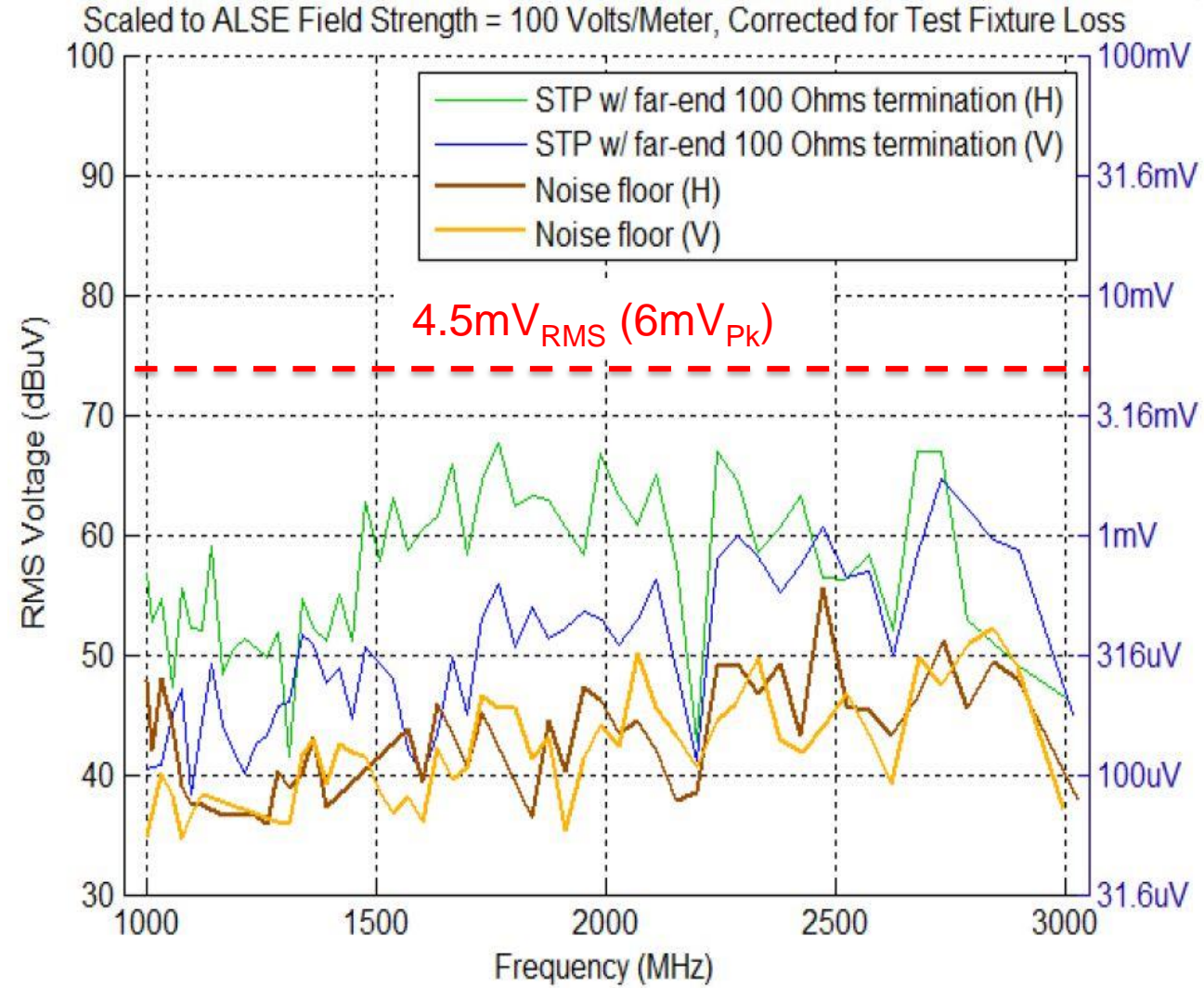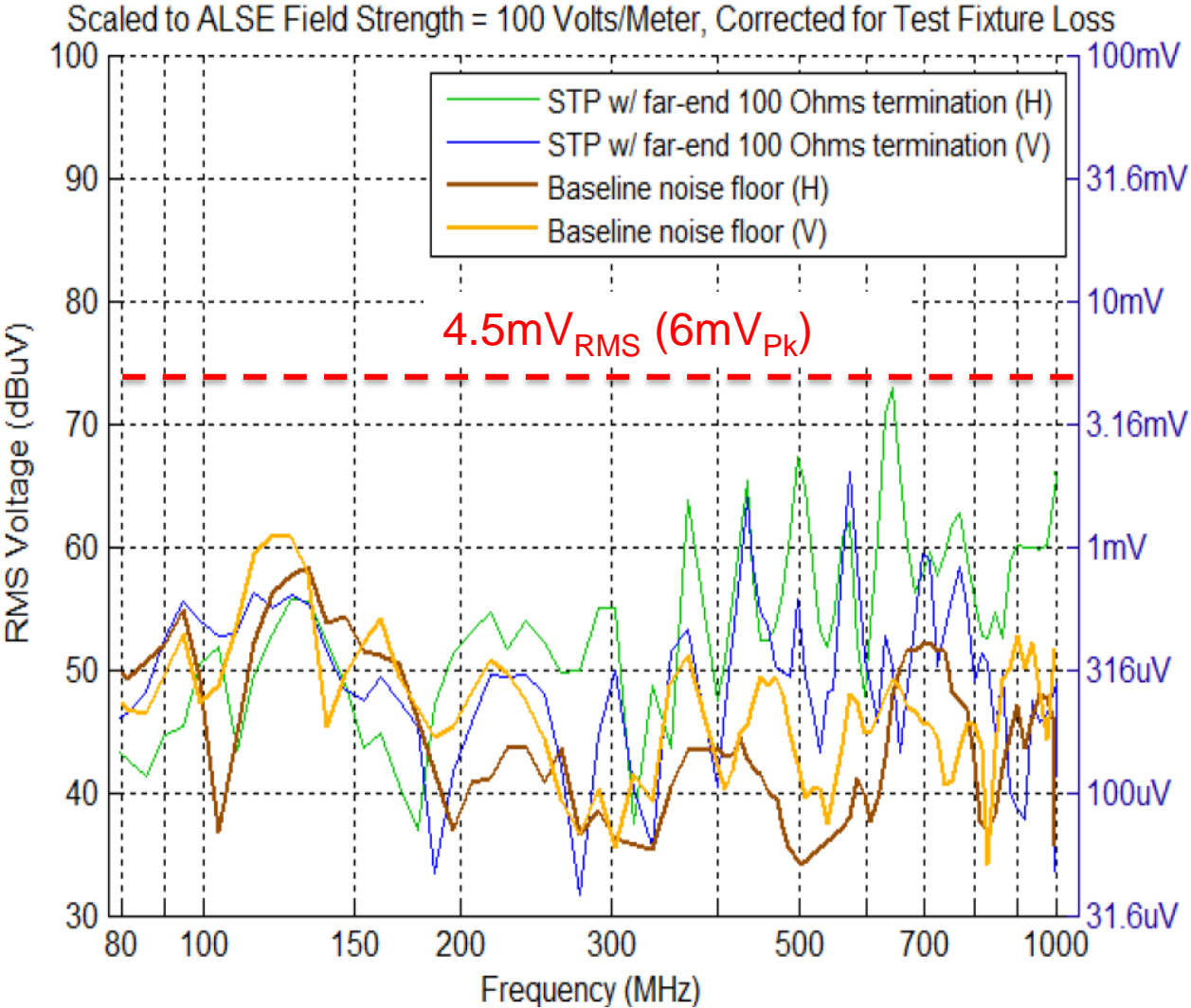 - Several worst-case frequencies within 1MHz - 5GHz selected for analysis

Table C.1 — Suggested test severity levels

Test severity level	Value V/m
I	25
II	50
III	75
IV	100
V	Specific value agreed between the users of this part of ISO 11452, if necessary

Table C.2 — Frequency bands

Frequency band	Frequency range MHz
F1	> 80 to ⩽ 400
F2	> 400 to ⩽ 1 000
F3	> 1 000 to ⩽ 10 000
F4	> 10 000 to ⩽ 18 000

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ALSE RFI Measurements for STP cable with H-MTD

Scaled to ALSE Field Strength = 100 Volts/Meter, Corrected for Test Fixture Loss

Left chart legend:
- STP w/ far-end 100 Ohms termination (H)
- STP w/ far-end 100 Ohms termination (V)
- Baseline noise floor (H)
- Baseline noise floor (V)

$4.5 mV_{RMS}$ ($6 mV_{Pk}$)

Right chart legend:
- STP w/ far-end 100 Ohms termination (H)
- STP w/ far-end 100 Ohms termination (V)
- Noise floor (H)
- Noise floor (V)

$4.5 mV_{RMS}$ ($6 mV_{Pk}$)

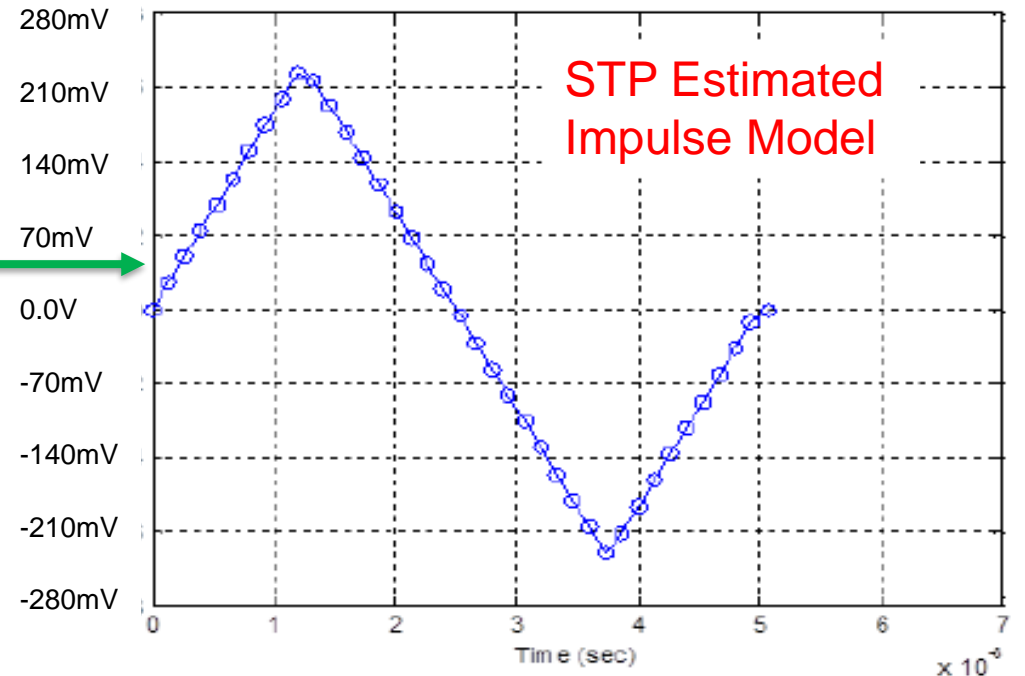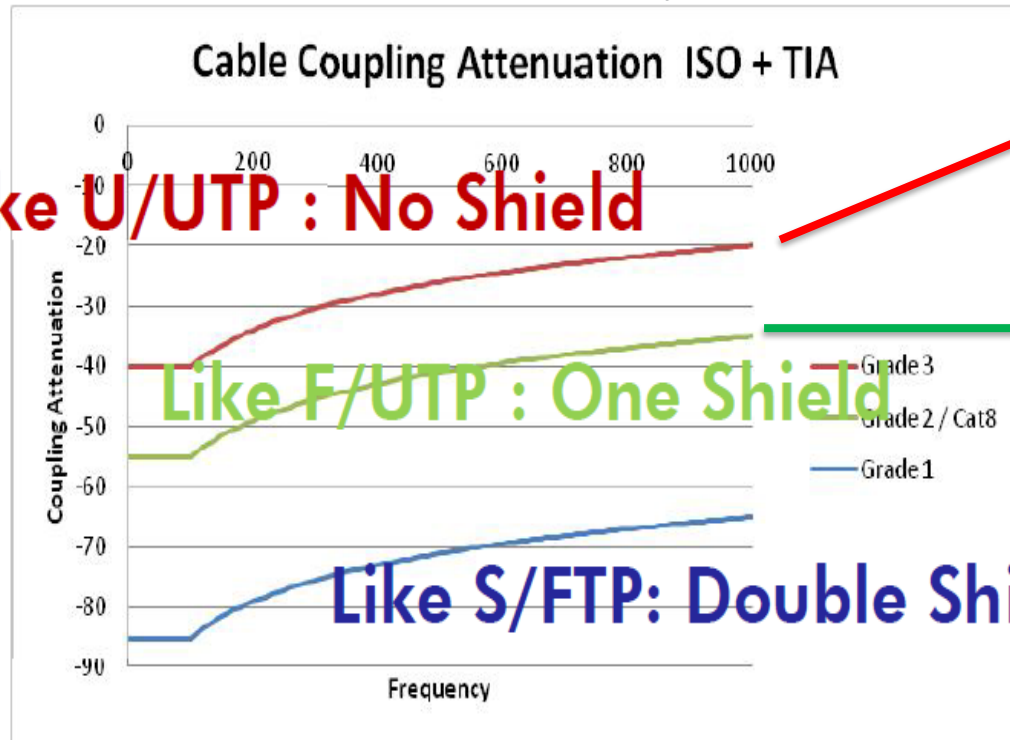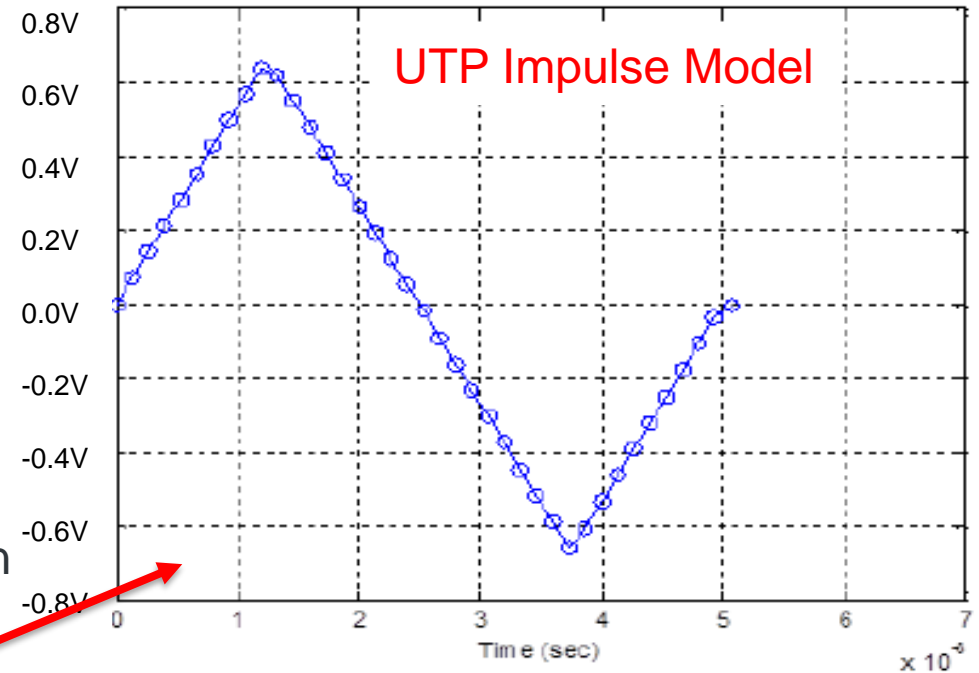# RFI Induced Differential Voltage at PHY Input
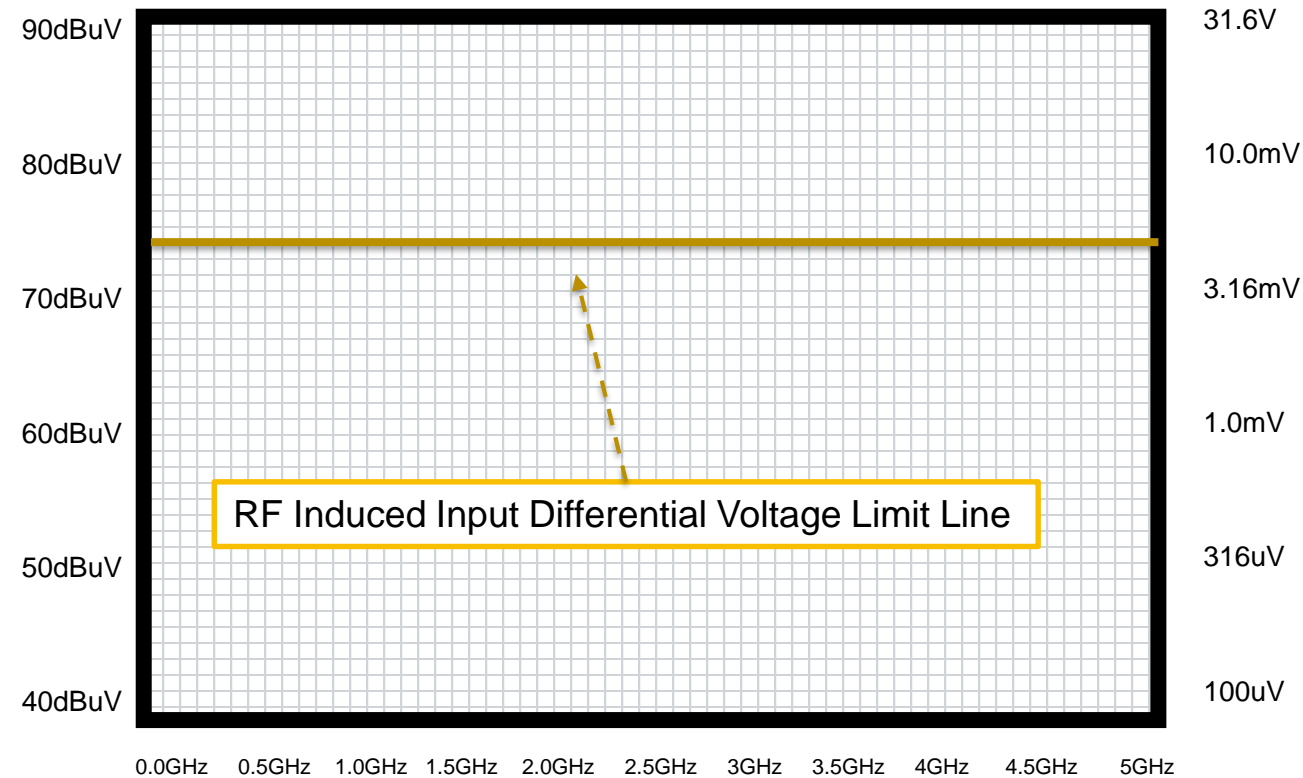
- The limit line used for the differential voltage magnitude at the PHY input induced by the RF fields coupled to the STP cable, which was used for the analysis

$$RF.Coupled.Input.Diff \leq 4.5mV_{RMS} \ (6.0mV_{Pk})$$
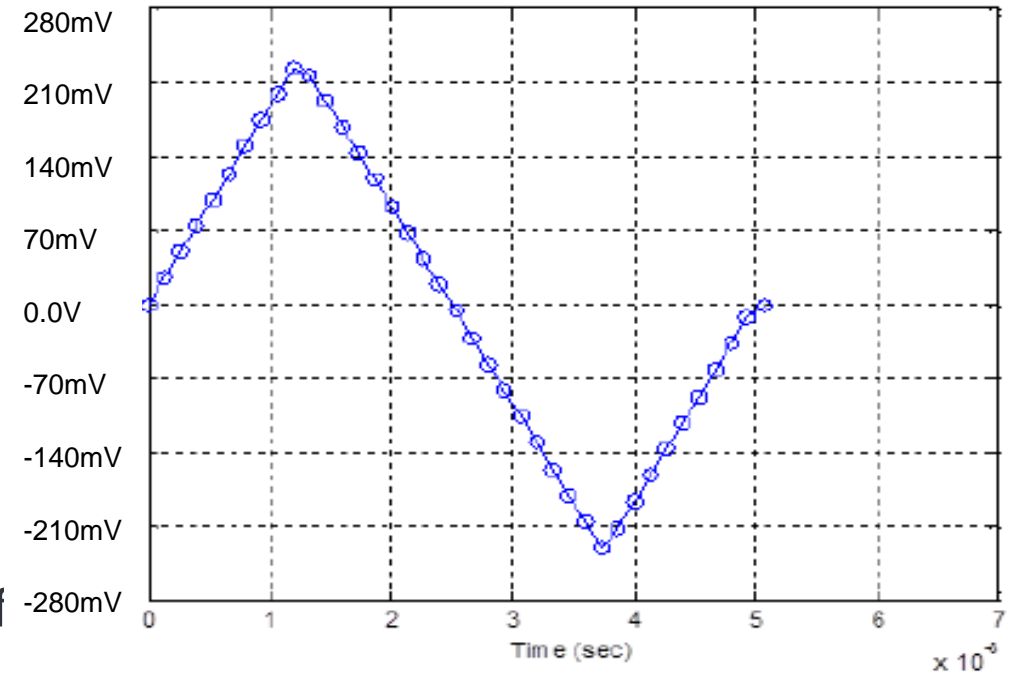
Burst Error Source

- ## Transient Impulse (ISO 7637-3)
  - Caused by Engine spark plus, etc
  - Triangular impulse: Duration < 50nsec, Freq. < 10KHz
  - Coupled magnitude estimated based on 1000BASE-T1
    - Took into account the coupling attenuation difference between STP and UTP (Conservatively assumed 10dB delta)

rossbach_0513_40GBT.pdf

Cable Coupling Attenuation ISO + TIA

Like U/UTP : No Shield
Like F/UTP : One Shield
Like S/FTP: Double Shield

Grade 3
Grade 2 / Cat8
Grade 1

UTP Impulse Model

STP Estimated Impulse Model

Burst Error Source

- ## Transient Impulse
  - Triangular impulse: Duration < 50nsec, Freq. < 10KHz
  - One impulse affects several symbols in a row
  - Example in 10Gbps PAM4
    - Can corrupt up to 280 symbols in 10Gbps PAM4
    - Can lead to BER ~1E-4 without FEC
  - The shorter the symbol period, the higher the number of affected symbols
  - The higher the PAM levels, the higher susceptibility the symbols get corrupted
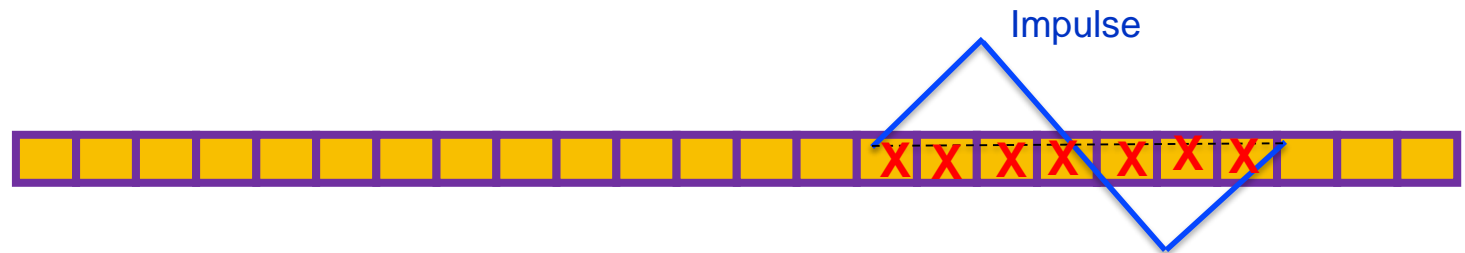
FEC Design Considerations

- Two major source of noise in automotive are
  - Large RFI Noise → Need to heavy DFE instead of linear equalization → Large burst error
  - Large Transient Impulses → Large burst errors
- Above considerations makes Reed-Solomon a right choice for FEC coding
  - Reed Solomon Codes: RS(N, M, K) → Each RS-Symbol consists of K bits
    - Frame = N x K bits (N < 2^K), Data = M x K bits
    - Coding Overhead = (N-M)/M → Corrects = (N-M)/2 RS-Symbols
    - To stay error free → RS Symbol Error Rate < (N-M)/2M
- Improving FEC Error Correction Performance
  - Higher coding overhead helps reduce all error types: Random, Burst, RFI,
    - Higher correction per frame → Higher coding overhead → Higher baud rate!
  - Code Interleaving further help with Burst errors → Increases latency

Basic Ethernet PCS structure (post-Gigabit Era)

- Take XGMII interface
  - Data and control words
- Transcode to new, blocked bit stream
  - 64/66b, 64/65b, 256/257b, 512/513b...
- Add FEC on top of blocking
- Map to PAM levels
  - Match block rates to use recovered efficiency to include FEC and match clock rates to be easily generated

- Lots of work going on in 802.3 for PAM-4 – we can look to other groups to borrow
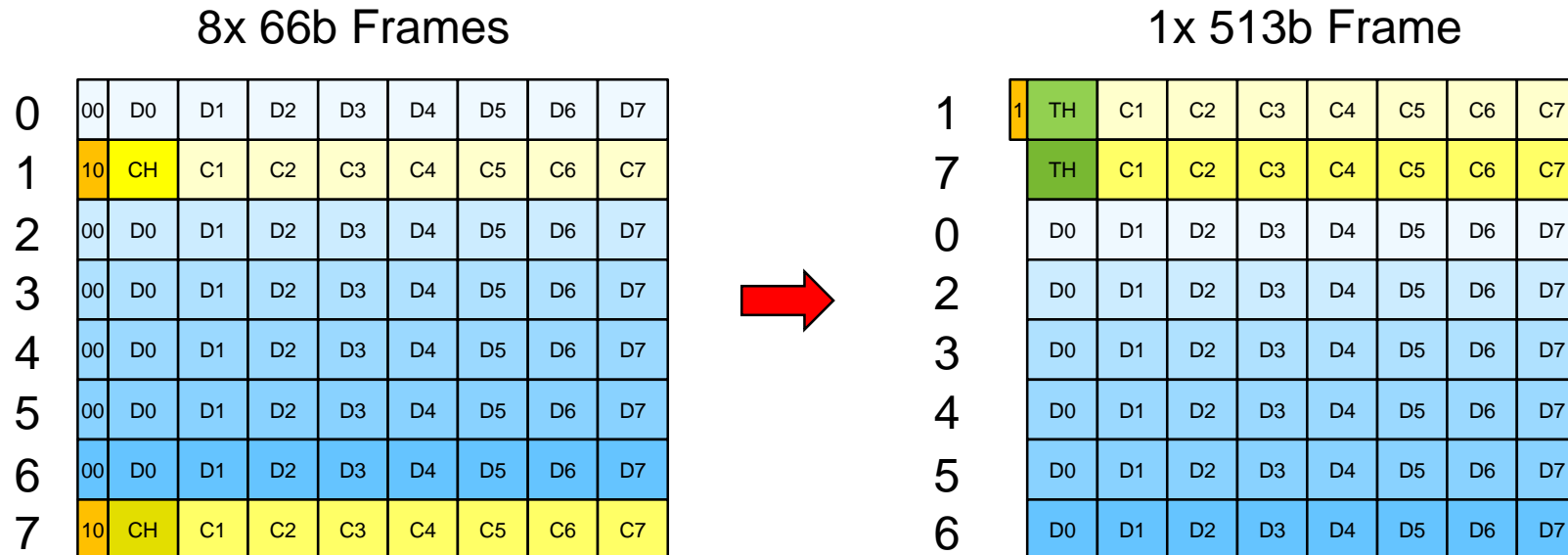
Basic Idea: 64B66 Compression

- The 01/10 frame marker used in 64B66 was driven by the noise model of the 10GBASE-R optical channel which was dominated by shot noise, and by the still reasonable 33/32 speed-up allowing a single PLL implementation of the CDR

- The 64/66B PCS of 10GBASE-R only uses 15 block field types to transport all of the Start-of-Frame, End-of-Frame, and Ordered Set information

  – Result is that there are ways to compress this PCS, as burning 2-bits in 66 to convey this information is not very efficient

Figure 49–7—64B/66B block formats

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More efficiency: 512/513b transcoding

- 512/513b coding takes 8x 64/66b blocks (8x XLGMII transfers) and transports them with fewer total bits by virtue of combining the individual control/data frame bits

- For example, collect all 66b control frames within the block of 8x 66b frames and puts them at the beginning of the block, and the data frames at the end of the block

8x 66b Frames

0	00	D0	D1	D2	D3	D4	D5	D6	D7
1	10	CH	C1	C2	C3	C4	C5	C6	C7
2	00	D0	D1	D2	D3	D4	D5	D6	D7
3	00	D0	D1	D2	D3	D4	D5	D6	D7
4	00	D0	D1	D2	D3	D4	D5	D6	D7
5	00	D0	D1	D2	D3	D4	D5	D6	D7
6	00	D0	D1	D2	D3	D4	D5	D6	D7
7	10	CH	C1	C2	C3	C4	C5	C6	C7

1x 513b Frame

1	1	TH	C1	C2	C3	C4	C5	C6	C7
7		TH	C1	C2	C3	C4	C5	C6	C7
0		D0	D1	D2	D3	D4	D5	D6	D7
2		D0	D1	D2	D3	D4	D5	D6	D7
3		D0	D1	D2	D3	D4	D5	D6	D7
4		D0	D1	D2	D3	D4	D5	D6	D7
5		D0	D1	D2	D3	D4	D5	D6	D7
6		D0	D1	D2	D3	D4	D5	D6	D7

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Possible Transcoding

- Choice of PCS layer is tightly tied to RS FEC choice, which in turn is tied to symbol rate on line

  - Goal is to have an integral number of 64B66 frames in an RS FEC frame

  - RS FEC frame line rate should be a simple multiple of the bit rate so both can be synthesized with a single PLL

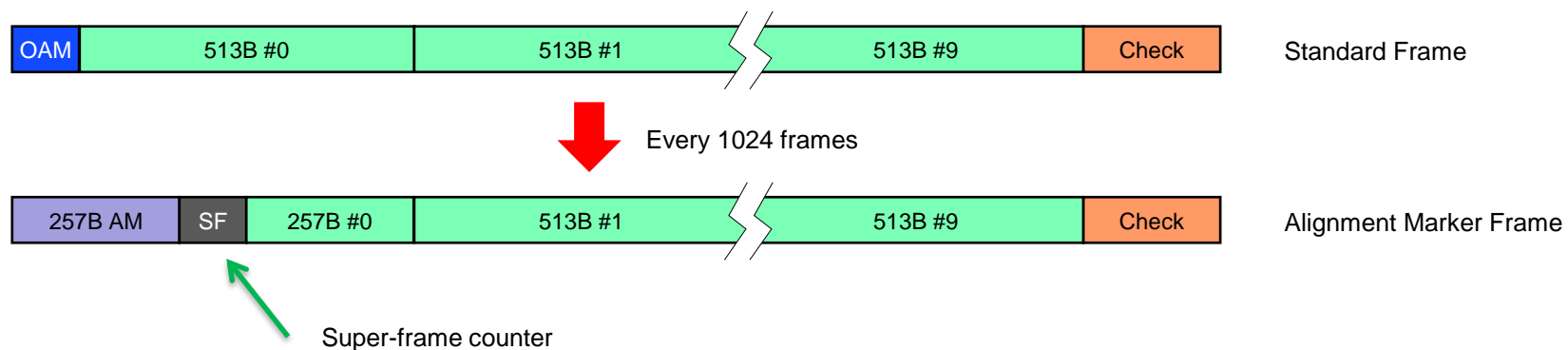   - for instance 64B66 has a 33/32 ratio between line rate and bit rate (NRZ so symbol rate = bit rate)

- Given the minimum FEC frame size requirements presented later in this presentation as being RS1024(564, 514) the most reasonable multiple of line-rate to bit-rate is 9/8*, which gives RS1024 (576,514) as the line code

  - RS FEC payload is 5140 bits long = 20x 256B257 frames or 10x 512B513 + 10-bit OAM

    - The latter is more optimal as it provides identical capacity as 20x 256B257 frames but also allows OAM signaling as per 1000BASE-T1

Scrambled Payload

| 62 Check | OAM | 513B #0 | 513B #1 | 513B #9 | 62 Check | OAM |

RS1024 (576, 514) frame
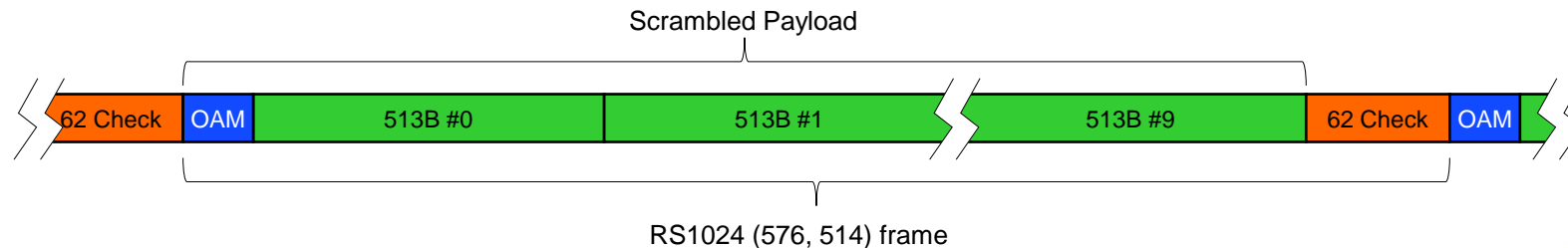
* 5760/5120 = 9/8

Possible Transcoding (continued)

- Using this frame allows reuse of the Clause 134 framing and training machinery which sends one 257B long alignment marker every 1024 RS frames

- Alternatively, for the 512B513-based frame the 10-bit OAM field and 1st 513B block can be replaced with the alignment marker 257B block, one normal 257B block, and a 9-bit field, like a superframe counter.

OAM	513B #0	513B #1	513B #9	Check	Standard Frame

Every 1024 frames

| 257B AM	SF	257B #0	513B #1	513B #9	Check	Alignment Marker Frame

Super-frame counter

Reed Solomon code complexity, latency and cost

- RS code choices from Tu:
  - m=10: GF(2^10) RS codes – cover ~50ns burst, latency ~ 10000BT
    - Tu cites concern over DFE error propagation
  - m=11: GF(2^11) RS codes – cover ~98ns burst, extra complexity, latency ~ 20000-21000 BT
  - m=12: GF(2^12) RS codes – cover ~160ns burst, more complexity, latency ~ 21000-32000 BT
- Complexity of RS decoders grows exponentially in m or faster
- Code latency grows exponentially in m, dominates the packet size (10000BT = 1250bytes), 5x the code latency of 10GBASE-T!
  - Fixed even if we DON'T have heavy impulse interference
  - High-speed interconnects will be performance limited by latency
- Traditionally, long bursts, code complexity and ability to vary latency are managed by interleaving – not by growing the code

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Interleaving

- x2 Interleaving takes 2x RS frames and commutates symbols before transmission
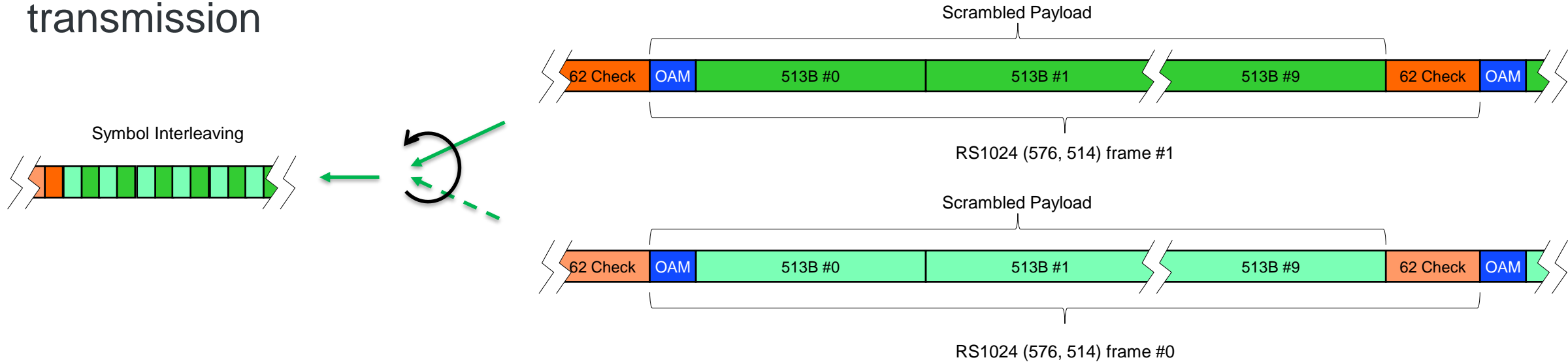
- x4 Interleaving takes 4x RS frames and commutates symbols before transmission

- The point of interleaving is to distribute a burst error across a group of interleaved frames, each which can fix the portion distributed to it

  – Design is a trade-off between the length of the burst, and how often it occurs

  – Smaller fields yield simpler RS codes, but they can correct less and are shorter

Possible interleave and performance

- Burst length can be met either by a large-GF RS code or by a shorter RS code with interleaving

  - Large GF codes fix the coding latency for all applications…

  - Shorter GF codes + interleaving make latency programmable.

    - Not much value going to RS(288, 258, 9) or shorter as these would need > L=2 interleaving

- Large GF codes increase complexity

- RS (576, 514, 10) with L = 1 or 2 appear good candidates

  - L=2 meets burst error criterion as defined

  - Could support greater interleaving as well if necessary

PHY1 FEC Simulation Results

10Gbps PAM4	Interleave L=	# of Tests	Output BER	Output FER
RS(288,258,9)	1	>1E+10	1.7E-10	2.72E-9
	2	>1E+10	1.4E-11	2.35E-9
RS(564,514,10)	1	>1E+10	2.37E-13	5.14E-9
	2	>1E+10	0	0
RS(576,514,10)	1	>1E+10	0	0
	2	>1E+10	0	0

2.5G/5Gbps PAM2	Interleave L=	# of Tests	Output BER	Output FER
RS(288,258,9)	1	>1E+10	0	0
	2	>1E+10	0	0
RS(564,514,10)	1	>1E+10	0	0
	2	>1E+10	0	0
RS(576,514,10)	1	>1E+10	0	0
	2	>1E+10	0	0

Simulation including error events:
- Automotive Transient impulse
  - +/-0.2V, 50n Triangular
  - Occurring every 100us

- Different Narrowband RFI tones
  - Different Sinewaves with $4.5mV_{RMS}$

- DFE error propagation
  - 1-Tap DFE

- Practical PHY limited SNR
  - SNR=~18.5dB at Slicer

Conclusion

- Accelerate 802.3ch standard by borrowing from other 802.3 efforts where possible

- PAM-4 offers good performance, compatibility to 802.3 standards, reuse and low complexity

- 2^{10} RS codes with interleaving meet error correction requirement while managing complexity and latency

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BCI Measurements for STP Cable with Grounded & Float Shield For RF Ingress for Frequencies <400MHz

STP cable assembly 2.0 m

IEEE 802.3ch: mueller_3ch_01_1117.pdf

4.5mV$_{RMS}$

Legend:
- Probe position 450 mm GND GND
- Probe position 450 mm float float
- Probe Position 150 mm GND GND
- Probe Position 150 mm float float

Axis labels: differential noise [mV] vs frequency [MHz]