aQuantia

ACCELERATING CONNECTIVITY

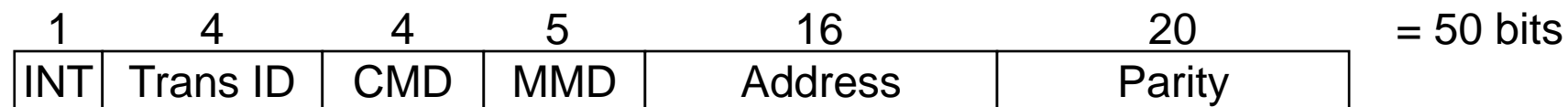# 802.3ch Link Partner Register Access

Dr. Paul Langner

Problem

- Construct a standard HW access mechanism that utilizes the 10 bit field "formerly known as OAM" that occurs once per 320ns in link mode and some less-frequent interval in EEE mode to allow reliable reading of link-partner MDIO registers within the noise environment

- Framework:

  - Noise environment is low-level Gaussian, with a 60-110ns burst every 100us

  - Data mode is protected with RS1024 (360, 326) with pseudo-noise (PN) scrambling so BER < 10^{-12} and scrambler takes care of spectral issues

    - Channel BW is 10-bits every 320 ns, so channel bit rate is 31.25 Mb/s

  - EEE mode is running unprotected with 10-bit field with a transmit interval of roughly every 32 frames and additive side-stream scrambler, so again no spectral issues

    - Channel BW is ~1/32 data mode = 10 bits every 10.24 us = ~0.975 Mb/s

    - Burst error environment can eliminate one 10-bit field, therefore need a code to protect against this, with a frame size less than 100us

Design Constraints

- Need to be able to send MMD, Address, and Command
  - Need a Transaction Number to distinguish read operations
  - Need an interrupt bit to reflect the state of the interrupt pin
- Command list should include:
  - Idle
  - Read
  - Read response
- Error correction should be able to fix 10 bits in the frame, so need 2x 10bits for ECC

Proposed frame structure

1	4	4	5	16	20	
INT	Trans ID	CMD	MMD	Address	Parity	= 50 bits

- Need to align the link-partner register access with data mode RS frames
  - Need it to be a multiple of 10-bits: so given the above, we need a 5 x 10 frame with RS1024(5,3) ECC
  - Use incremental search to find frame, as there are only 5 starting positions
    - Disallow CMD = 0 as "all-zero" payload produces zero parity, and framing will not work

- Example read times:

1. Data Mode: Read request round-trip takes:
   - 320ns x 5 = 1.6us transmit + 0.5us decode + 3.2 us read register* + 320ns x 5 = 1.6us response = 6.9us

2. EEE Mode: Read request round-trip takes:
   - 320ns x 32 x 5 = 51.2uS transmit + 0.5us decode + 3.2 us read register + 320ns x 32 x 5 = 51.2us response = 106.1us

* Typical MDIO transaction time at 10 MHz = ~3.2us

AQUANTIA

Details

- INT = 1 indicates the link-partner has an interrupt
- TRANS ID (transaction ID) is a 4 bit hardware counter that tracks requests and responses
  - Each PHY has its own rolling 4-bit counter and matches read transaction IDs against read-response transaction IDs
  - If a read-response not seen within TBD link partner register access frames, the read is re-issued
- CMD is a 4-bit field indicating the action for the register access frame
  - 0 = Invalid, 1 = Idle, 2 = Read
  - 3 = Read response, 4-15 = Reserved
- MMD is MMD to read
- Address is Address within the MMD to read

Link Partner Register Access Transactions

Idle

1	4	4	5	16	20
INT	0	1	00	0000	Parity

Read

1	4	4	5	16	20
INT	Req. trans ID	2	MMD	Address	Parity

Read Response

1	4	4	5	16	20
INT	Req. trans ID	3	00	Data	Parity

aQuantia | 6

Register Definitions

Link Partner Register Access Control Register 1:

- Bit 15: Read-Only: Link Partner Interrupt
  - When set indicates that the link-partner interrupt is set. In order to clear this, the source of the link-partners interrupts must be cleared or masked
- Bit 14 – Bit 13: Reserved
- Bit 12 – Bit 8: Read / Write: Link partner target MMD
  - The MMD to access in the link partner
- Bit 7 – Bit 2: Reserved
- Bit 1: R/W: Link partner access command
  - 0 = Read, 1 = Reserved
- Bit 0: R/W, Clear on Completion: Execute Command.
  - When set, this executes the command indicated in Bit 1 (read is only option), and is cleared by hardware when the command is complete – i.e. the read result is available for reading

Register Definitions (continued)

Link Partner Register Access Address:

- Bit 15 – Bit 0: Read / Write: Link partner target address
  - The address within the MMD specified to access in the link partner

Link Partner Register Access Data:

- Bit 15 – Bit 0: Read-Only: Link partner data
  - The data returned from the link partner as the result of a read command

Example Usage

Read Example:

1. Write "Link Partner Register Access Address" with desired address to read

2. Write "Link Partner Register Access Control Register 1" with the desired MMD in bits 12:8 and 1 in bit 0

3. Poll "Link Partner Register Access Control Register 1" bit 1 to clear

4. Read the result in "Link Partner Register Access Data"

Interrupt Example:

1. Periodically poll "Link Partner Register Access Control Register 1" bit 15*

2. Read link partner interrupt status register tree to find the source of the interrupt

* Or connect this bit into the local interrupt tree, so polling is not required

AQUANTIA |