

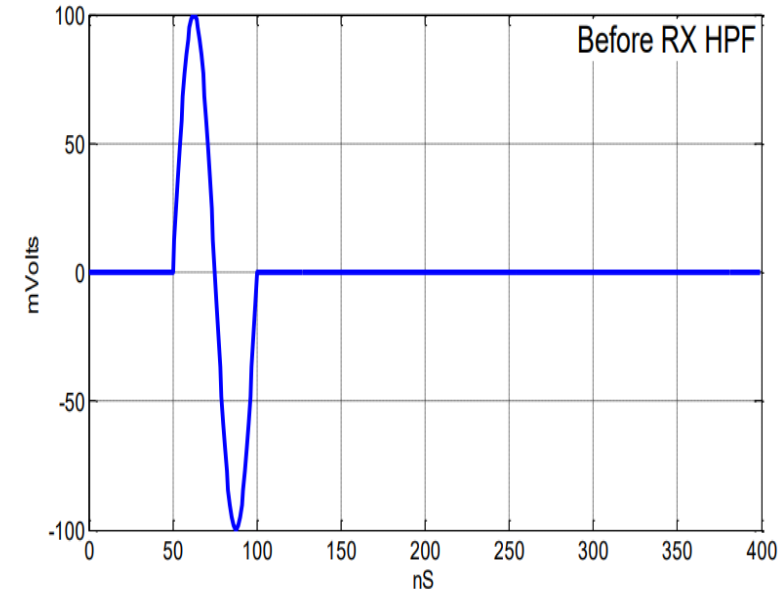
Transcode, FEC & Interleaver Optimization

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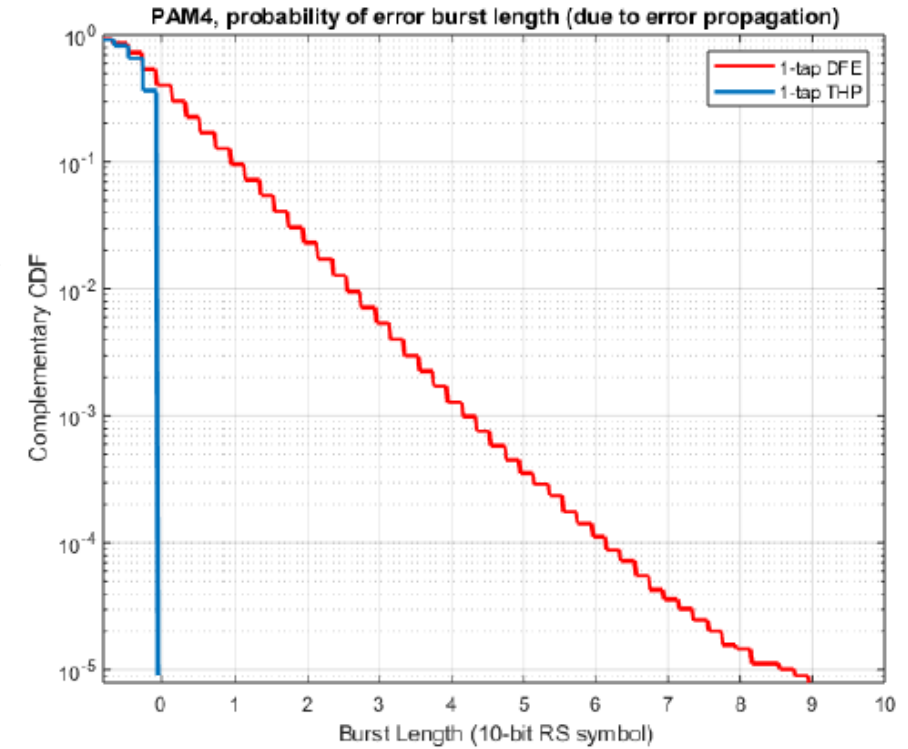
Review of 1000BASE-T1 FEC Requirement

- Protected error burst = 176 nsec
 - 50nsec transient noise + DFE error propagation + random errors
- Transient noise model
 - Based on ISO 7637-3
 - Measured with 2m UTP cable
 - 50nsec duration
 - “One cycle of a 20MHz sinusoidal signal with magnitude of 100mV”
 - http://www.ieee802.org/3/bp/public/jan14/Chini_Tazebay_3bp_01a_0114.pdf
- DFE assumed in FEC analysis
 - No pre-coder
 - Simulated DFE error propagations after burst errors may last over 75 PAM3 symbols (100nsec)



802.3ch FEC Requirements

- STP cable only
 - Transient noise amplitude will be lower than measured on UTP cables
- Optional fixed pre-coder
 - Proposed in http://www.ieee802.org/3/ch/public/adhoc/southern_3ch_01_0818.pdf
 - DFE error propagations may be avoided, or substantially reduced
- Prior study
 - http://www.ieee802.org/3/ch/public/jul18/farjarad_3ch_01d_0718.pdf
 - Assumed 1-tap DFE and 10dB lower transient noise levels due to STP
 - Simulation showed 10G burst error length between 22nsec to 28nsec
- **A reasonable target is <~60nsec burst error protections**
 - Transient noise + random errors + some margin
 - 2.5G = 50nsec + 14 PAM4 symbols
 - 5G = 50nsec + 28 PAM4 symbols
 - 10G = 50nsec + 56 PAM4 symbols
 - DFE error propagations controlled by, e.g., optional fixed pre-coder



10Gbps PAM4	Interleave L=	# of Tests	Output BER	Output FER
RS(288,258,9)	1	>1E+10	1.7E-10	2.72E-9
	2	>1E+10	1.4E-11	2.35E-9
RS(564,514,10)	1	>1E+10	2.37E-13	5.14E-9
	2	>1E+10	0	0
RS(576,514,10)	1	>1E+10	0	0
	2	>1E+10	0	0

Updated FEC Candidates for 2.5G

Code Option	RS N	RS K	RS N-K	frame nsec	Correctio n nsec	latency nsec	# OAM symbols	# Data symbols	PCS i/p P bits	PCS o/p P+1 bits	# PCS blocks
A8	288	261	27	1024.00	46.22	1123.56	1	260	64	65	40
A9	360	326	34	1280.00	60.44	1404.44	1	325	64	65	50
A10	432	391	41	1536.00	71.11	1685.33	1	390	64	65	60
A11	504	456	48	1792.00	85.33	1966.22	1	455	64	65	70
A1	576	521	55	2048.00	96.00	2247.11	1	520	64	65	80
A2	648	586	62	2304.00	110.22	2528.00	1	585	64	65	90
A3	720	651	69	2560.00	120.89	2808.89	1	650	64	65	100
A4	792	716	76	2816.00	135.11	3089.78	1	715	64	65	110
B1	576	517	59	2048.00	103.11	2261.33	1	516	128	129	40
B2	720	646	74	2560.00	131.56	2826.67	1	645	128	129	50
B3	864	775	89	3072.00	156.44	3392.00	1	774	128	129	60
B4	1008	904	104	3584.00	184.89	3957.33	1	903	128	129	70
C1	576	515	61	2048.00	106.67	2268.44	1	514	256	257	20
C2	864	772	92	3072.00	163.56	3402.67	1	771	256	257	30
D1	576	514	62	2048.00	110.22	2272.00	1	513	512	513	10

- Code “A9” is proposed for 2.5G
 - Corrects up to 60nsec of burst errors
 - Consists of 50 64B/65B PCS blocks + 1 OAM + 34 parity check symbols

Updated FEC Candidates for 5G

Code Option	RS N	RS K	RS N-K	frame nsec	Correctio n nsec	latency nsec	# OAM symbols	# Data symbols	PCS i/p P bits	PCS o/p P+1 bits	# PCS blocks
A8	288	261	27	512.00	23.11	561.78	1	260	64	65	40
A9	360	326	34	640.00	30.22	702.22	1	325	64	65	50
A10	432	391	41	768.00	35.56	842.67	1	390	64	65	60
A11	504	456	48	896.00	42.67	983.11	1	455	64	65	70
A1	576	521	55	1024.00	48.00	1123.56	1	520	64	65	80
A2	648	586	62	1152.00	55.11	1264.00	1	585	64	65	90
A3	720	651	69	1280.00	60.44	1404.44	1	650	64	65	100
A4	792	716	76	1408.00	67.56	1544.89	1	715	64	65	110
B1	576	517	59	1024.00	51.56	1130.67	1	516	128	129	40
B2	720	646	74	1280.00	65.78	1413.33	1	645	128	129	50
B3	864	775	89	1536.00	78.22	1696.00	1	774	128	129	60
B4	1008	904	104	1792.00	92.44	1978.67	1	903	128	129	70
C1	576	515	61	1024.00	53.33	1134.22	1	514	256	257	20
C2	864	772	92	1536.00	81.78	1701.33	1	771	256	257	30
D1	576	514	62	1024.00	55.11	1136.00	1	513	512	513	10

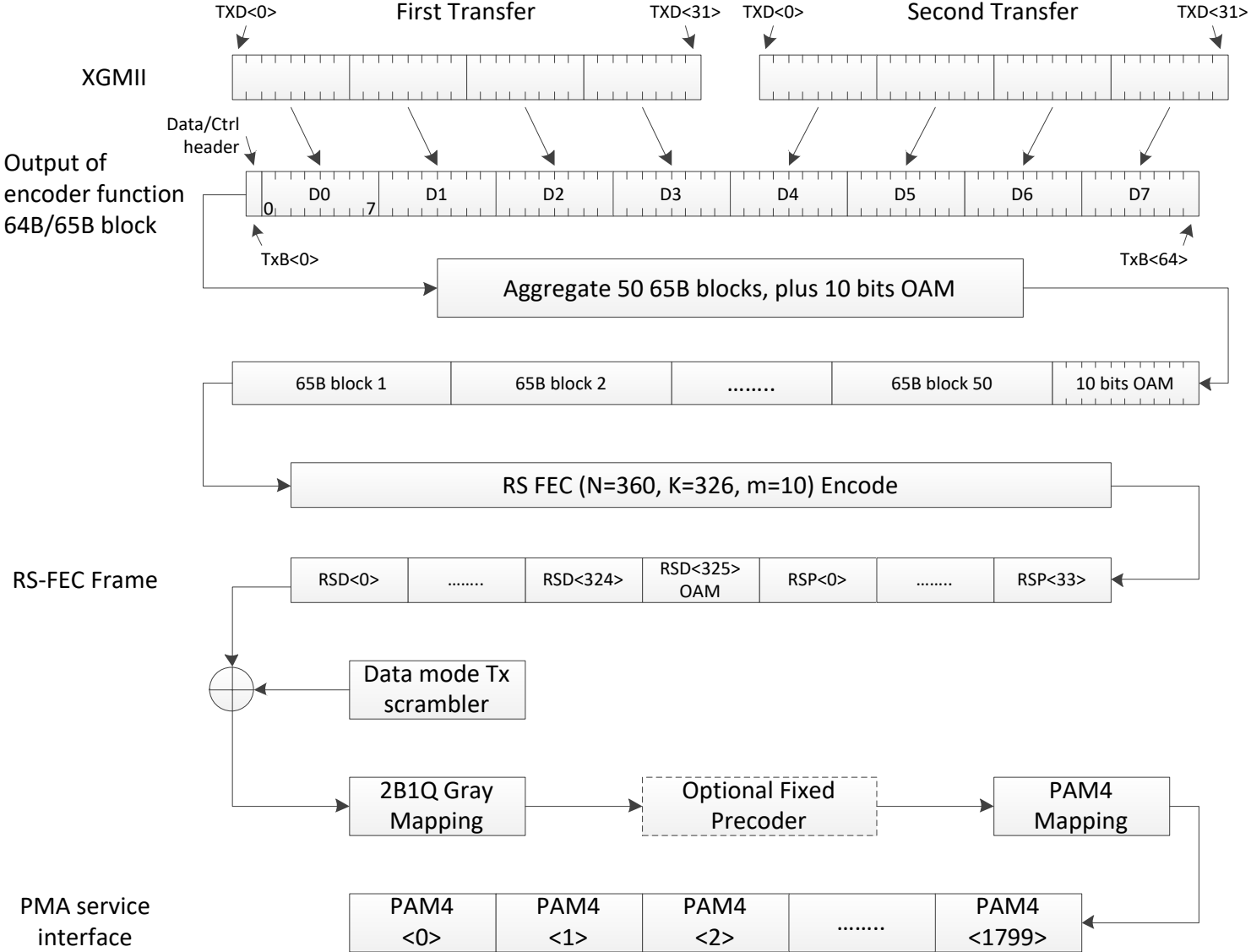
- Code “A9” with interleaver **L=2** is proposed for 5G
 - Intrinsic latency = $2 \times 702.22 \text{ nsec} = 1404.44 \text{ nsec}$
 - Corrects up to 60nsec of burst errors

Updated FEC Candidates for 10G

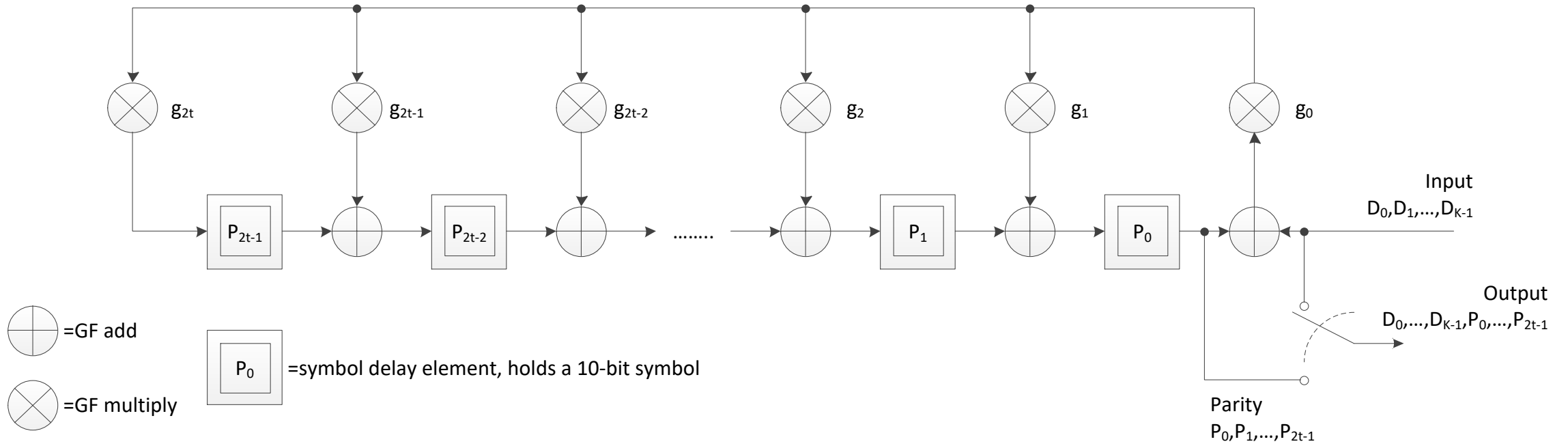
Code Option	RS N	RS K	RS N-K	frame nsec	Correctio n nsec	latency nsec	# OAM symbols	# Data symbols	PCS i/p P bits	PCS o/p P+1 bits	# PCS blocks
A8	288	261	27	256.00	11.56	280.89	1	260	64	65	40
A9	360	326	34	320.00	15.11	351.11	1	325	64	65	50
A10	432	391	41	384.00	17.78	421.33	1	390	64	65	60
A11	504	456	48	448.00	21.33	491.56	1	455	64	65	70
A1	576	521	55	512.00	24.00	561.78	1	520	64	65	80
A2	648	586	62	576.00	27.56	632.00	1	585	64	65	90
A3	720	651	69	640.00	30.22	702.22	1	650	64	65	100
A4	792	716	76	704.00	33.78	772.44	1	715	64	65	110
B1	576	517	59	512.00	25.78	565.33	1	516	128	129	40
B2	720	646	74	640.00	32.89	706.67	1	645	128	129	50
B3	864	775	89	768.00	39.11	848.00	1	774	128	129	60
B4	1008	904	104	896.00	46.22	989.33	1	903	128	129	70
C1	576	515	61	512.00	26.67	567.11	1	514	256	257	20
C2	864	772	92	768.00	40.89	850.67	1	771	256	257	30
D1	576	514	62	512.00	27.56	568.00	1	513	512	513	10

- Code “A9” with interleaver **L=4** is proposed for 10G
 - Intrinsic latency = $4 \times 351.11 \text{ nsec} = 1404.44 \text{ nsec}$
 - Corrects up to 60nsec of burst errors

PCS Transmit w/o Interleaving

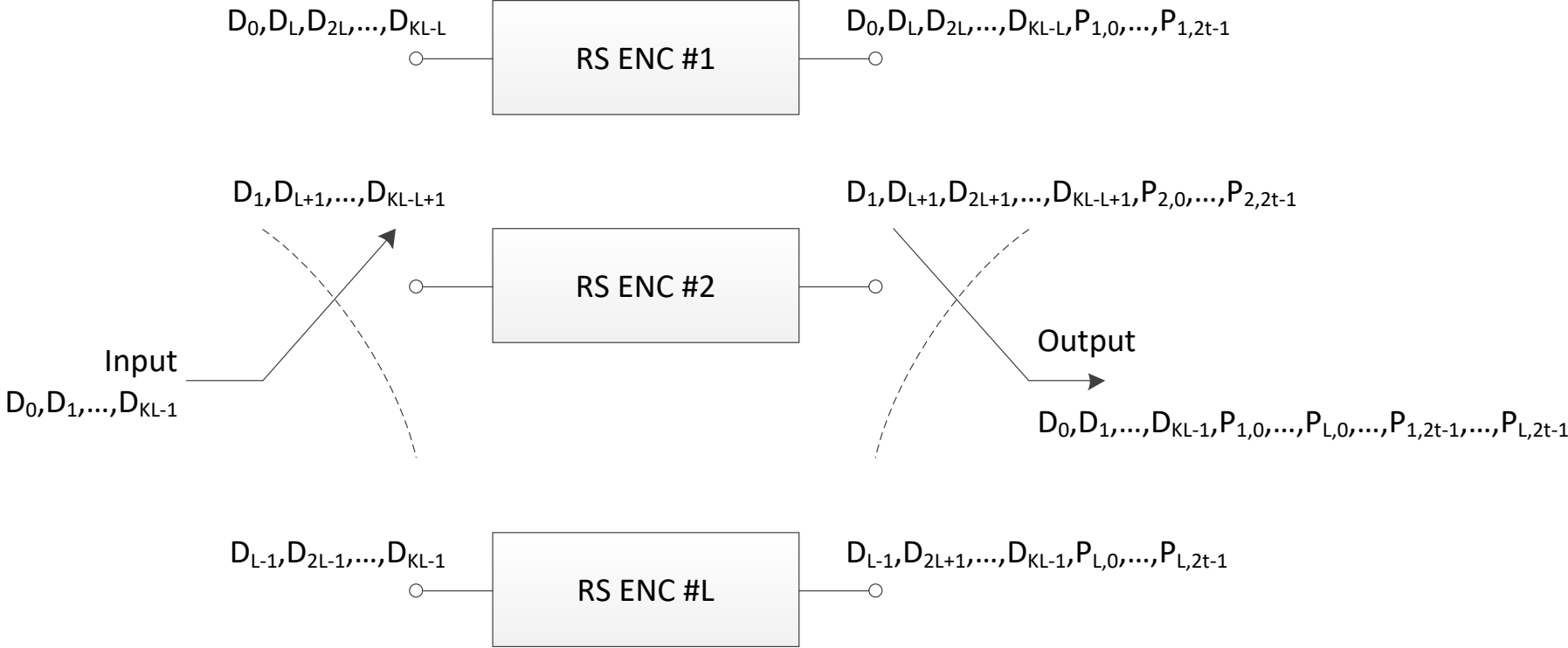


RS Encoder



- Modified from 802.3 Figure 91-5
- D_0 is the first input symbol, and the first output symbol

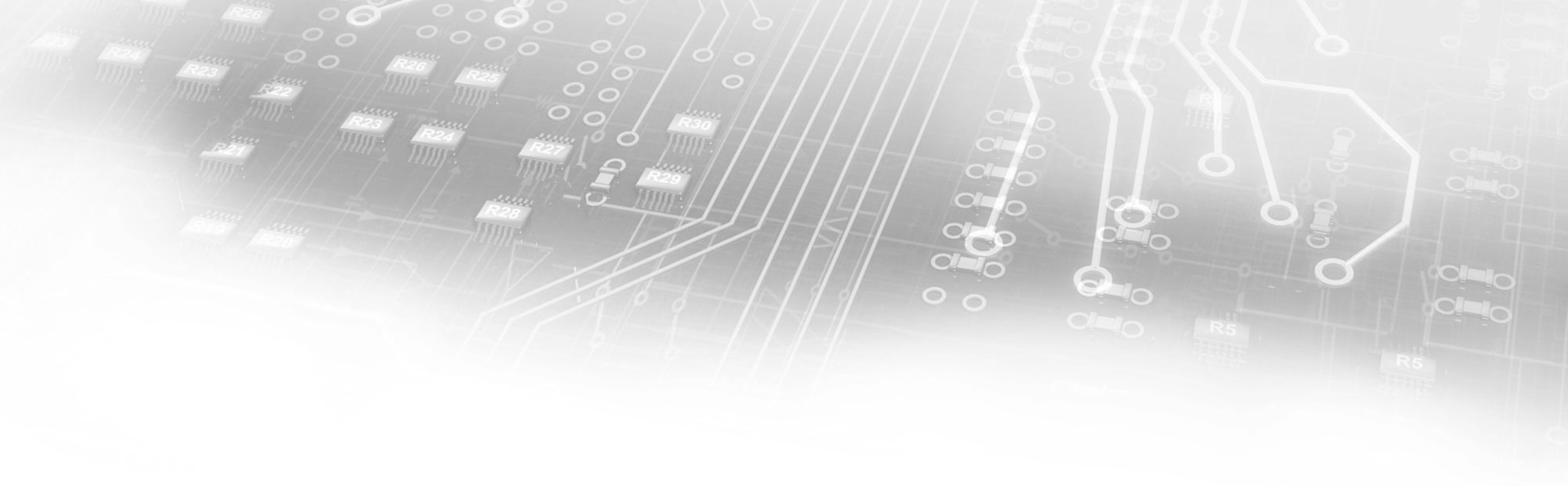
Interleaver Example



- $L =$ interleaving depth

Summary

- For 802.3ch, 60nsec of burst error correction is recommended for FEC
 - Assuming optional fixed pre-coder is adopted
 - Transient noise + random errors + some margin
 - 2.5G = 50nsec + 14 PAM4 symbols
 - 5G = 50nsec + 28 PAM4 symbols
 - 10G = 50nsec + 56 PAM4 symbols
- Propose to adopt PCS 64B/65B transcoding
- A new RS FEC (N=360, K=326, m=10) with interleaving is proposed
 - 50 blocks of 64B/65B PCS blocks + 1 OAM symbol
 - Default L=1 for 2.5G, L=2 for 5G, and L=4 for 10G
- A PCS transmit diagram is presented
- An interleaver example is provided



THANK YOU

