RS FEC Proposal for Multi-Gigabit Automotive PHY

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July 11, 2018

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802.3ch RS FEC Contributions

- Reuse 1000BASE-T1 FEC
  - RS(N=450, K=406, m=9)
  - http://www.ieee802.org/3/ch/public/may18/wu_3ch_01a_0518.pdf
  - http://www.ieee802.org/3/ch/public/may18/McClellan_3ch_01a_0518.pdf
- List of FEC code with m=10, 11, 12 without interleaving
  - http://www.ieee802.org/3/ch/public/may18/tu_3ch_01b_0518.pdf
- Interleaved RS FEC
  - http://www.ieee802.org/3/ch/public/adhoc/farjarad_3chah_01b_061218.pdf
  - RS (N=576, K=514, m=10) with L = 1 or 2
  - 512B/513B PCS encoding (new)

Considerations for RS FEC

- Match to constellation sizes
  - Ideally, m should be a multiple of 2 bits (e.g., PAM4) or 2.5 bits (DSQ-32 or 32-CROSS)
  - RS symbol “m=10 bits” is a good choice
- Match to PCS encoding block size
  - http://www.ieee802.org/3/ch/public/may18/McClellan_3ch_01a_0518.pdf
  - http://www.ieee802.org/3/ch/public/adhoc/farjarad_3chah_01b_061218.pdf
  - PCS encoding options: 64B/65B, 256B/257B, 512B/513B
  - Must contain integer number of PCS blocks per RS FEC frames
  - Simple clock multiplier ratios ➔ easier implementation
- Error correction requirements
  - Random errors
  - Burst errors, including errors due to DFE error propagation
- DFE error propagations
  - Sensitive to DFE coefficient values
  - We believe the burst error protection length should be at least 120nsec
  - Interleaved RS FEC can be applied

Selecting RS FEC Parameters

- m=10 bits
  - Note: N<=1023
  - Compatible with 2 or 2.5bits/baud constellations
- Interleaving depth L = 1, 2, or 4
  - Exchanged/selected during training via InfoFields
  - Selectable based on application needs
- 1 symbol reserved for OAM
  - “Borrowed” from one RS redundancy symbols
- Total PCS + FEC redundancy = 12.5% (same as 1000BASE-T1) to maintain simple clock ratios
- List of FEC parameters for PCS encoding 64B/65B, 256B/257B, 512B/513B
  - See following slide

RS FEC Candidates

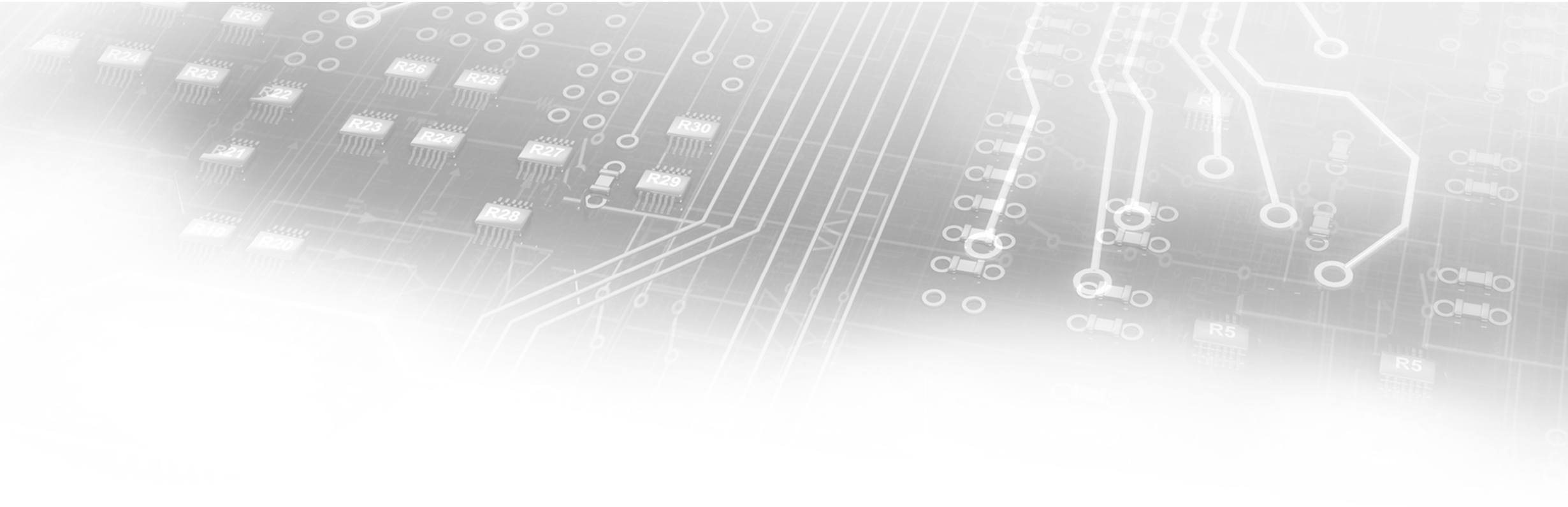
Code Option	RS m	RS N	RS K	RS N-K	FEC frame nsec	Correction nsec	FEC latency nsec	# Data symbols	PCS i/p P bits	PCS o/p P+1 bits	# PCS frames
802.3bp	9	450	406	44	3600.00	176.00	3952.00	405	80	81	45
A1	10	576	521	55	512.00	24.00	560.89	520	64	65	80
A2	10	648	586	62	576.00	27.56	631.11	585	64	65	90
A3	10	720	651	69	640.00	30.22	701.33	650	64	65	100
A4	10	792	716	76	704.00	33.78	771.56	715	64	65	110
A5	10	864	781	83	768.00	36.44	841.78	780	64	65	120
A6	10	936	846	90	832.00	40.00	912.00	845	64	65	130
A7	10	1008	911	97	896.00	42.67	982.22	910	64	65	140
B1	10	576	517	59	512.00	25.78	564.44	516	128	129	40
B2	10	720	646	74	640.00	32.89	705.78	645	128	129	50
B3	10	864	775	89	768.00	39.11	847.11	774	128	129	60
B4	10	1008	904	104	896.00	46.22	988.44	903	128	129	70
C1	10	576	515	61	512.00	26.67	566.22	514	256	257	20
C2	10	864	772	92	768.00	40.89	849.78	771	256	257	30
D1 (*)	10	576	514	62	512.00	27.56	567.11	513	512	513	10

Correctable burst length for 10GBASE-T1 = floor((N-K)/2) * m / 11.25Gbps

(*) Code option D1 proposed in http://www.ieee802.org/3/ch/public/adhoc/farjarad_3chah_01b_061218.pdf

Proposals on RS FEC and PCS Encoding

- Adopt the 64B/65B PCS encoding
  - Proven in 10G/5G/2.5GBASE-T applications
  - Existing design that speeds up PHY development
  - Smaller PCS blocks more likely to survive uncorrectable errors
  - Allows flexible choices in RS FEC parameters, due to smaller PCS blocks
- Adopt RS FEC option “A3” with N=720, K=651, m=10
  - FEC frame duration is 640nsec
  - Burst error protection of 31.11nsec
  - FEC intrinsic latency is 701.33nsec
  - Supports 1 symbol (10 bits) OAM
  - Each FEC frame consists of 100 PCS 64B/65B blocks
- Adopt configurable interleaver depth of L=1, 2, or 4, exchanged/selected during training via InfoFields
  - With L=4, the proposed RS FEC can protect more than 120nsec of burst errors
  - For applications requiring lower latency, L=1 or 2 can be selected instead



THANK YOU

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