

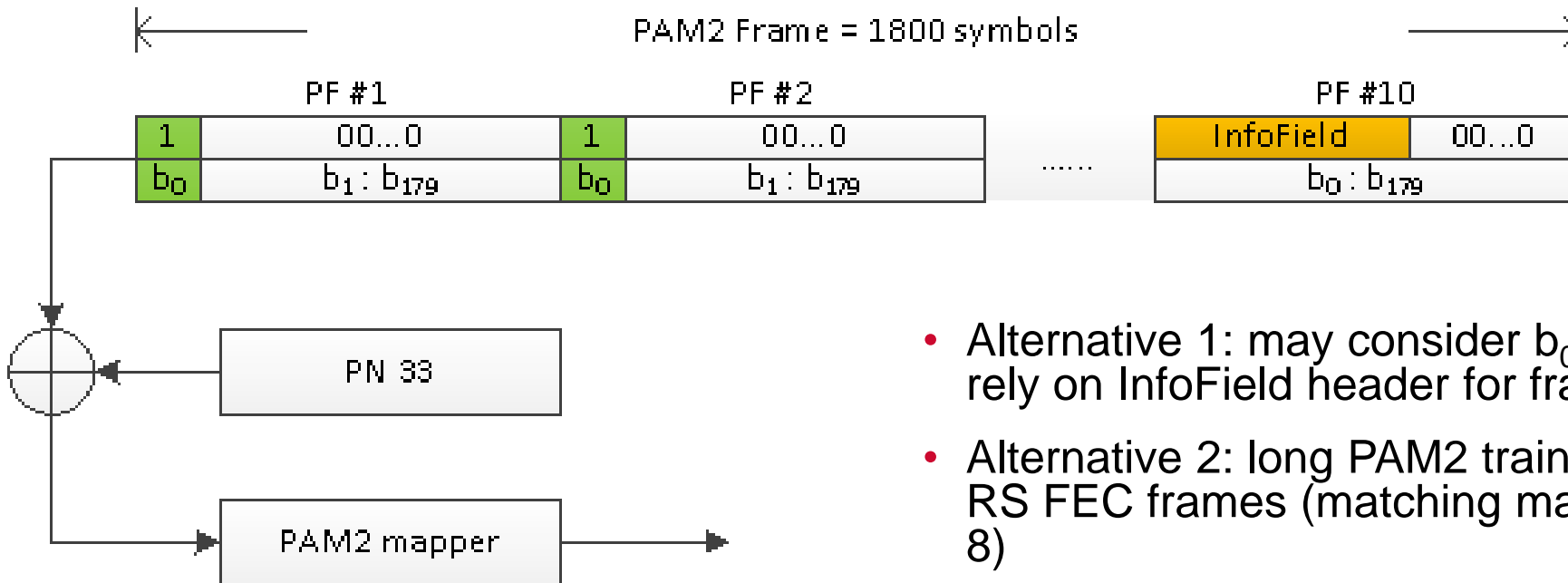
Proposed Baseline for Training Sequence

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Starting from 97.4.2.4 and Figure 97-26

- PAM2 training frame boundary aligned with data mode RS FEC frame
 - Data mode RS FEC (N=360, K=326, m=10) → 1800 PAM4 symbols
 - Training frame consists of 1800 PAM2 symbols
 - 320nsec for 10G, 640nsec for 5G, and 1.28usec for 2.5G
- 10 partial PHY frames
 - Each partial frame consists of 180 PAM2 symbols, same as in 1000BASE-T1
 - First bit of each partial PHY frame is inverted as alignment markers
 - InfoField XOR'ed at the start of the 10th partial frame



- Alternative 1: may consider $b_0=0$ for PF #1, ..., PF #9, and rely on InfoField header for frame alignment
- Alternative 2: long PAM2 training frame, e.g., equals to 8 RS FEC frames (matching maximum interleaving depth of 8)

InfoField

96-bit Infofield



Table 97-7—InfoField message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 97-8—InfoField message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

- Add to InfoField Exchange
 - Precoder selection = 2 bits (bypass, 1+D, 1-D, 1-D²)
 - Interleaver depth = 2 bits (L = 1/2/4/8)
- Already exchanged
 - Local partial frame counters
 - EEE and “OAM” capabilities
 - Data mode scrambler seeds
 - Exact time (partial frame count) to switch from PAM2 training to data mode

PHYC Training States (preliminary)

- Start with MS PAM2 half duplex
- SL PAM2 starts after en_slave_tx=1
- MS and SL check for loc_rcvr and rem_rcvr status OK
- Exchange EEE, OAM capabilities, precoder selection, and interleaver depth
- Exchange exact time for each PHY to switch into PCS Test
- Count down and switch to PCS Test
 - Precoder enabled
 - Transition to SEND DATA state

