Baseline for 149.4.2.4

Start from 97.4.2.4

~~97~~149.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure ~~97-26~~149-16.

During PMA training (TRAINING and COUNTDOWN states in Figure ~~97-26~~149-16), PHY Control information is exchanged between link partners with a 12-octet InfoField, which is XORed with the first 96 bits of the ~~15th~~ 16th partial PHY frame (bits ~~2520~~ 13500 to ~~2615~~13595) of the PHY frame. The InfoField is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the PAM2 to ~~PAM3~~ PAM4 transition.

The 12-octet InfoField shall include the fields in ~~97~~149.4.2.4.2 through ~~97~~149.4.2.4.8, also shown in the overview Figure ~~97-20~~149-nn1, and the more detailed Figure ~~97-21~~149-nn2 and Figure ~~97-22~~149-nn3. Each InfoField shall be transmitted at least 256 times to ensure detection at link partner.

[Editor note: Copy Figure 97-20 as Figure 149-nn1, Figure 97-21 as Figure 149-nn2, and Figure 97-22 as Figure 149-nn3.]

octet 1	octet 2	octet 3	octet 4/5/6	octet 7	octet 8/9/10			octet 11/12
0xBB	0xA7	0x00	PFC24	Message	MSG24	MSG24	MSG24	CRC16

Figure 149-nn1 – InfoField format

octet 1	octet 2	octet 3	octet 4/5/6	octet 7	octet 8/9/10	octet 11/12
0xBB	0xA7	0x00	PFC24	Message	UsrCfgCap	CRC16

Figure 149-nn2 – InfoField TRAINING format

octet 1	octet 2	octet 3	octet 4/5/6	octet 7	octet 8/9/10	octet 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 149-nn3 – InfoField COUNTDOWN format

~~97~~149.4.2.4.1 InfoField notation

For all the InfoField notations in the following subclauses, Reserved<bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The InfoField is transmitted following the notation ~~described in 97.3.2.2.3~~ where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

~~97~~149.4.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of 3 octets [Oct1<7:0>, Oct2<7:0>, Oct3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Oct1<7:0> and so forth.

~~97~~149.4.2.4.3 Partial PHY frame Count (PFC24)

The start of partial PHY frame Count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6<7:0>] and indicates the running count of partial PHY frames sent LSB first. There are ~~15~~ 16 partial PHY frames per PHY frame and the InfoField is embedded within the ~~15th~~ 16th partial PHY frame. The first partial PHY frame is zero, thus the first partial PHY frame count field after a reset is ~~14~~15.

~~97~~149.4.2.4.4 Message Field

Message Field (1 octet). For the MASTER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, reserved<3:0>}. For the SLAVE, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING, and PMA_state<7:6> = 01 indicates COUNTDOWN.

All possible Message Field settings are listed in Table ~~97–7~~149-tt1 for the MASTER and Table ~~97–8~~149-tt2 for the SLAVE. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table ~~97–7~~149-tt1 for the MASTER and the first or second row of Table ~~97–8~~149-tt2 for the SLAVE. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the InfoField variable is set to loc_rcvr_status<5> = 1 and set to 0 otherwise.

[Editor note: Copy Table 97-7 as Table 149-tt1, and Table 97-8 as Table 149-tt2.]

Table 149-tt1 – InfoField message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 149-tt2 – InfoField message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

~~97~~149.4.2.4.5 PHY Capability Bits~~,~~ ~~User Configurable Register,~~ and Data Mode Scrambler Seed

When PMA_state<7:6> = 00, then [0ct8<7:0>, 0ct9<7:0>, 0ct10<7:0>] contains the two PHY capability bits~~, the user configurable register bits,~~ and the 15-bit data mode scrambler seed (Seed). Each octet is sent LSB first.

As shown in Figure 149-nn4, ~~T~~the format of PHY capability bits is Oct9<7> = EEEen~~, and~~ Oct10<0> = OAMen, Oct10<2:1> = InterleaverDepth, and Oct10<4:3> = PrecodeSel.

EEEen and OAMen indicat~~eing~~ EEE and 1000BASE-T1 OAM capability enable, respectively. The PHY shall indicate the support of these two optional capabilities by setting the corresponding capability bits.

InterleaveDpeth indicates the requested data mode interleaving depth and PrecodeSel indicates the requested data mode precoder.

The data mode scrambler seed contains bits S14 (sent first) to S0 (sent last) to indicate the initial state of the data mode transmit scrambler of the local device upon reaching the data switch partial PHY frame count. The state of the scrambler in Figure ~~97–9~~149-nn5 shall be S14:S0 at the first bit of the first PHY frame when the partial PHY frame counter equals to the DataSwPFC24 value, see ~~97.4.2.4.6~~149.xyz. The format of Seed is Oct8<7:0> = S<7:14> and Oct9<6:0> = S<0:6>. Seed S<14:0> shall not be all zeros.

The remaining ~~73~~-bit Oct10<7:~~15~~> ~~form a user configurable register. See 97.4.2.4.11 for details~~shall be reserved and set to 0.

octet 8								octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Seed (or Reserved)															EEEen	OAMen	InterleaveDepth		PrecodeSel		Reserved	Reserved	Reserved

Figure 149-nn4 – PHY Capability Bits and Data Mode Scrambler Seed

Formatted: Keep with next

97149.4.2.4.6 Data Switch partial PHY frame Count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the data switch partial PHY frame count (DataSwPFC24) sent LSB first. DataSwPFC24 indicates the partial PHY frame count when the transmitter switches from PAM2 to ~~PAM3~~PAM4, which occurs at the start of an RS-FEC superframe~~block~~. The last value of PFC24 prior to the transition is DataSwPFC24 - 1. DataSwPFC24 shall be set to an integer multiple of ~~15~~16. This value of DataSwPFC24 guarantees that the switch from PAM2 to ~~PAM3~~ PAM4 occurs on a PHY frame boundary.

97149.4.2.4.7 Reserved Fields

When PMA_state<7:6> is greater than 01, then [Oct8<1:0>, Oct9<1:0>, Oct10<7:0>] contains a reserved field. All InfoField fields denoted Reserved are reserved for future use.

97149.4.2.4.8 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial (x+1)(x15+x+1) of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 97149–23. In Figure 97149–23 the 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards Oct4 through Oct10 are used to compute the CRC16 with the switch connected, which is setting CRCgen in Figure 97149–23. After all the 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

97149.4.2.4.9 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 97149–9. Mapping of MDIO status variables to PMA status variables is shown in Table 97149–10.

97149.4.2.4.10 Start-up sequence

The start-up sequence shall comply with the state diagram description given in Figure ~~97–26~~149-16. If the Auto-Negotiation function is not implemented, or mr_autoneg_en = false, PMA_CONFIG is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup.

The Auto-Negotiation function is optional ~~for 1000BASE-T1 PHYs~~. If the Auto-Negotiation function is used, during the Auto-Negotiation process PHY Control is in the DISABLE_TRANSMITTER state and the transmitter is disabled. If the Auto-Negotiation function is not used, during the PHY Link Synchronization stage the PHY Control remains in the DISABLE_TRANSMITTER state and the Link Synchronization function (see 97149.4.2.6) is the data source for the PMA Transmit function.

When the Auto-Negotiation asserts link_control = ENABLE, or PHY Link Synchronization process asserts sync_link_control = ENABLE, PHY Control enters the INIT_MAXWAIT_TIMER state. Upon entering the INIT_MAXWAIT_TIMER state, the maxwait_timer is started. PHY Control then transitions to the SILENT state where the minwait_timer is started and the PHY transmits zeros (tx_mode = SEND_Z).

In MASTER mode PHY Control transitions to the TRAINING state once the minwait_timer expires.

Upon entering the TRAINING state, the minwait_timer is started and the PHY Control asserts tx_mode = SEND_T sending PAM2 together with InfoFields. The PHY Control also sets PMA_state = 00 and sends the PHY capability bits, the user configurable register bits, and the Seed value used by the local device for the data mode scrambler initialization, see 97149.4.2.4.5.

The optional EEE capability shall be enabled only if both PHYs set the capability bit EEEen = 1. The optional 1000BASE-T1 OAM capability shall be enabled only if both PHYs set the capability bit OAMen = 1.

InterleaveDpeth indicates the requested data mode interleaving depth. The value Oct10<2:1> = 00 shall indicate interleaving depth L=1, or no interleaving. The values Oct10<2:1> = 01, 10, and 11 shall indicate interleaving depth of 2, 4, and 8, respectively. The PHY transmitter shall be able to support the requested interleaving depth as indicated by the link partner.

PrecodeSel indicates the requested data mode precoder. The value Oct10<4:3> = 00 shall indicate precoder bypass, or no precoder. The values Oct10<4:3> = 01, 10, and 11 shall indicate precoder choice of 1-D, 1+D, and $1+D^2$, respectively, as indicated in 149.3.2.2.20. The PHY transmitter shall be able to support the selected precoder as indicated by the link partner.

Initially the MASTER is not ready for the SLAVE to respond and sets en_slave_tx = 0, which is communicated to the link partner via the InfoField. After the MASTER has sufficiently converged the necessary circuitry, the MASTER shall set en_slave_tx = 1 to allow the SLAVE to transition to TRAINING.

In SLAVE mode PHY Control transitions to the TRAINING state only after the SLAVE PHY acquires timing, converges its equalizers, acquires its descrambler state and sets loc_SNR_margin = OK. The SLAVE shall align its transmit ~~81B~~ 65B RS FEC super frame to within +0/–1 partial PHY frames of the MASTER as seen at the SLAVE MDI. The SLAVE InfoField partial PHY frame Count shall match the MASTER InfoField partial PHY frame Count for the aligned frame.

Upon entering TRAINING state the SLAVE initially sets timing_lock_OK = 0 until it has acquired timing lock at which point the SLAVE sets timing_lock_OK = 1.

After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter InfoField value loc_rcvr_status. The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr_status. Upon expiration of the minwait_timer and when the condition loc_rcvr_status = OK and rem_rcvr_status = OK is satisfied, PHY control transitions to the COUNTDOWN state.

Upon entering the COUNTDOWN state, PHY Control sets PMA_state = 01 and DataSwPFC24 to the value of the partial PHY frame count when the transmitter switches from PAM2 to ~~PAM3~~PAM4.

Upon reaching DataSwPFC24 partial PHY frame count PHY Control transitions to the ~~SEND_IDLE1~~PCS_TEST1 state and forces transmission into the ~~idle~~ PCS Test mode by asserting tx_mode = ~~SEND_I~~SEND_N.

Once the link partner has transitioned from PAM2 to ~~PAM3~~PAM4, PHY Control transitions to the ~~SEND_IDLE2~~ PCS_TEST2 state and starts the minwait_timer.

Upon expiration of the minwait_timer and when the condition loc_phy_ready = OK and rem_phy_ready = OK is satisfied, PHY control transitions to the SEND_DATA state.

Upon entering the SEND_DATA state, PHY Control starts the minwait_timer and enables frame transmission to the link partner by asserting tx_mode = SEND_N.

The operation of the maxwait_timer requires that the PHY complete the start-up sequence from state INIT_MAXWAIT_TIMER to SEND_DATA in the PHY Control state diagram state diagram (Figure ~~97–26~~149-16) in less than 97.5 ms to avoid link_status being changed to FAIL by the Link Monitor state diagram (Figure ~~97–27~~149-17).

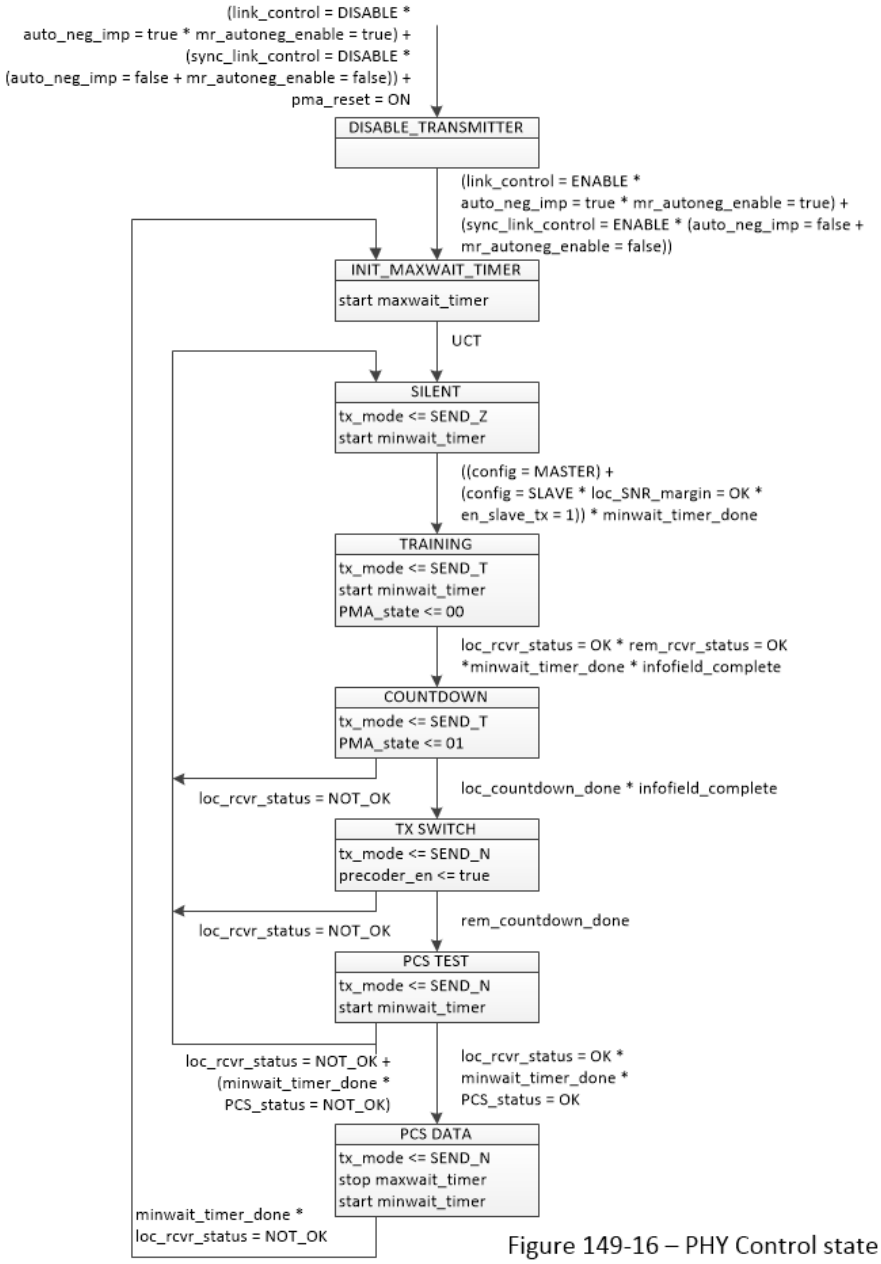
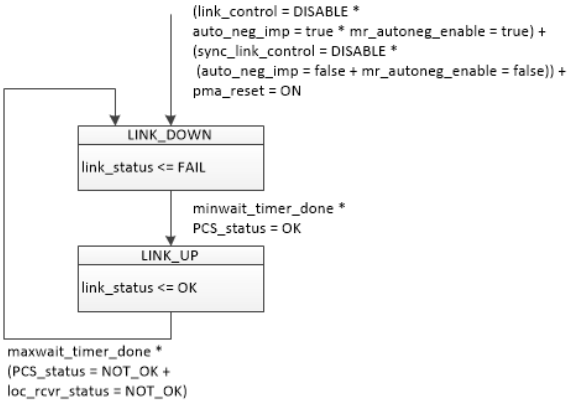


Figure 149-16 – PHY Control state diagram

[NOTE: Need to redefine “rem_countdown_done” to be based on implicit counter values, instead of checking last InfoField.]

[NOTE: Need to define “PCS_status” based on Clause 55.]



NOTE 1 – maxwait_timer is started in PHY Control state diagram (see Figure 149-16).
NOTE 2 – The variables link_control and link_status are designated as link_control_mGigT1 and link_status_mGigT1, respectively, by the Auto-Negotiation Arbitration state diagram (Figure 98-7) if the optional Auto-Negotiation function is implemented.

Figure 149-17 – Link Monitor state diagram

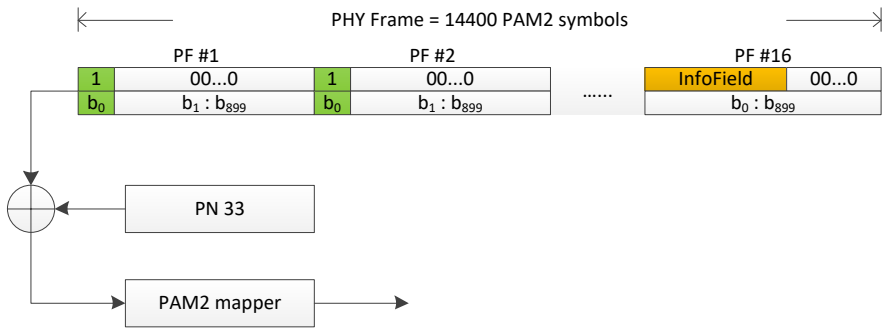


Figure 149-nn5 – PAM2 Training PHY frame

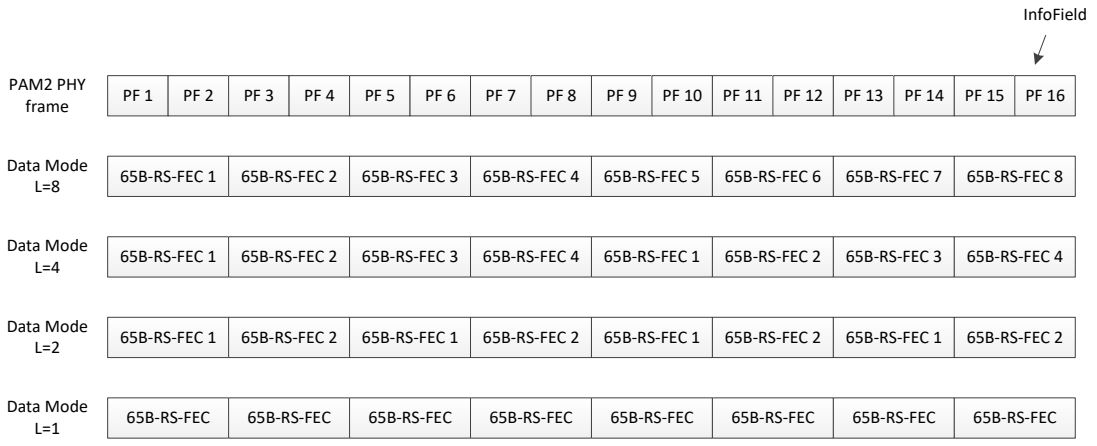


Figure 149-nn6 – Alignment of PAM2 Training PHY frame and data mode RS-FEC superframe

Formatted: Keep with next