IEEE802.3ch Timing and Next Steps Rev 2

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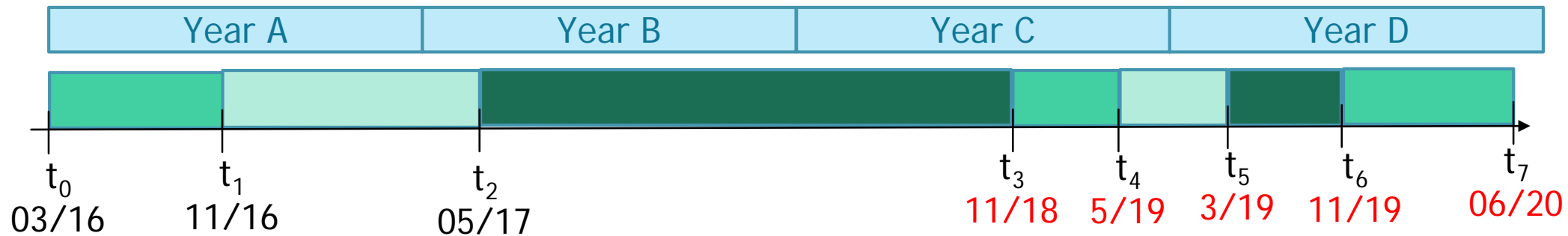
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IEEE P802.3ch

Typical Automotive Ethernet PHY IEEE Timing

Timeline from CFI with dates added.

- ▶ t_0 – Idea for CFI.
- ▶ t_1 – CFI approved. Start to work on PAR Components.
- ▶ t_2 – PAR approved. Start TF meetings and select technology components.
- ▶ t_3 – D1.0 complete. Refine specification.
- ▶ t_4 – D2.0 complete. WG ballot begins.
- ▶ t_5 – D3.0 complete. Sponsor ballot begins.
- ▶ t_6 – Sponsor ballot complete.
- ▶ t_7 – Completed specification available.

Year A	Year B	Year C	Year D

t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7

03/16 11/16 05/17 11/18 5/19 3/19 11/19 06/20

IEEE P802.3 P802.3ch NGAUTO Ethernet PHY DRAFT Timeline

- September 2017 - Review baseline proposals (Draft 0.1 skeleton)

- March 2018 – Draft 0.2 for TF review (link segment)

- September 2018 – baselines selected

- November 2018 – last technical feature, D1.0 for TF review
  - D1.1 (January), D1.2 (OOS February Interim), D1.3 (March), (OOS April Interim)?

- May 2019 – D2.0, start WG ballot
  - 2 recircs, July 2019 (D2.1), September 2019 (D2.2) (OOS interim in October to get to sponsor ballot in November 2019)

- November 2019 – D3.0, begin Sponsor ballot
  - D3.1 (January 2020), D3.2 (March) recirculations (Potential April OOS Interim)

- May/June 2020 SASB approval

Timing Questions

- Can we be ready for TF review in 6 months?
  - No, 10-12 months is more realistic based on discussions in TF.

- Final silicon (Engineering Samples) is currently projected to be needed mid 2021. What does this mean for the spec timing?

Goals to Draft 1.0

- March 2018
  - OEM topology Information and power consumption expectations
  - Cabling System Model (IL & RL at a minimum)
  - Signaling type and modulation (2.5 Gb/s and 10 Gb/s)
  - PHY vendors provide information on what type of EMC test data is preferred
  - Consider power budget and impact on PoDL
- May 2018
  - Cabling System Model (TCL, ELTCTL)
  - Finalized: Signaling type and modulation (2.5 Gb/s and 10 Gb/s)
  - MDI RL limit (baseline to be provided to PoDL)
  - Provide EMC test data
- July 2018
  - Line Coding and FEC initial proposals
  - PoDL definition (solicit help from bt)
  - OEMs provide results of Early EMC testing

Goals to Draft 1.0

- September 2018
  - Line Coding and FEC updated proposals
  - PoDL definition baseline proposals
  - Initial Register maps, EEE support, PICs
  - PHY Control State diagram proposals (take into account start up time requirements)

- November 2018
  - Line Coding and FEC baseline adopted
  - Complete Register maps, EEE support, PICs
  - PHY Control State diagram finalize