Text Edits for Clause 45 PHY Registers for 802.3ch

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Clause 1:

Insert new definition for MultiGBASE-T1 after 1.4.334 MultiGBASE-T

1.4.344a MultiGBASE-T1: PHYs that belong to the set of specific BASE-T1 PHYs at speeds in excess of 1000 Mb/s, including 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1. (See IEEE Std 802.3, Clause 149.)

Clause 45:

45.2.1 PMA/PMD Registers

Insert new rows to Table 45-3 for registers 1.2309 – 1.2313 after row for register 1.2308, and adjust reserved row as shown (unchanged rows not shown):

Table 45-3 PMA/PMD registers

Register address	Register name	Subclause
1.2309	MultiGBASE-T1 PMA control	45.2.1.192
1.2310	MultiGBASE-T1 PMA status	45.2.1.193
1.2311	MultiGBASE-T1 training	45.2.1.194
1.2312	MultiGBASE-T1 link partner training	45.2.1.195
1.2313	MultiGBASE-T1 test mode control	45.2.1.196
~~1.2309~~1.2314 through 32767	Reserved	

Insert 45.2.1.192 through 45.2.1.196 and Tables 45-155a through 45-155e after 45.2.191.

45.2.192 MultiGBASE-T1 PMA control register (1.2309)

The assignment of bits in the MultiGBASE-T1 PMA control register is shown in Table 45–155a.

Table 45-155a MultiGBASE-T1 PMA control register bit definitions

Bits(s)	Name	Description	R/W[a]
1.2309.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2309.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W

1.2309.13:12	Reserved	Value always 0	RO
1.2309.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2309.10:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.1.192.1 PMA/PMD reset (1.2309.15)

Resetting the MultiGBASE-T1 PMA/PMD is accomplished by setting bit 1.2309.15 to a one. This action shall set all MultiGBASE-T1 PMA/PMD registers to their default states. As a consequence, this action may change the internal state of a MultiGBASE-T1 PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the MultiGBASE-T1 PMA/PMD shall return a value of one in bit 1.2309.15 when a reset is in progress; otherwise, it shall return a value of zero. The MultiGBASE-T1 PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2309.15.
During a reset, the MultiGBASE-T1 PMD/PMA shall respond to reads from register bits 1.2309.15, 1.8.15:14, and 1.0.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 1.2309.15 is a copy of 1.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the MultiGBASE-T1 PMA/PMD.

45.2.1.192.2 Transmit disable (1.2309.14)

When bit 1.2309.14 is set to a one, the PMA shall disable output on the transmit path. When bit 1.2309.14 is set to a zero, the PMA shall enable output on the transmit path.
Bit 1.2309.14 is a copy of 1.9.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.192.3 Low power (1.2309.11)

When the low-power ability is supported, the MultiGBASE-T1 PMA/PMD may be placed into a low-power mode by setting bit 1.2309.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the MultiGBASE-T1 PMA/PMD. The behavior of the MultiGBASE-T1 PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2309.11 is zero.

This operation interrupts data communication. The data path of the MultiGBASE-T1 PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

Bit 1.2309.11 is a copy of 1.0.11 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the MultiGBASE-T1 PMA/PMD in low-power mode.

45.2.193 MultiGBASE-T1 PMA status register (1.2310)

The assignment of bits in the MultiGBASE-T1 PMA status register is shown in Table 45–155b.

Table 45-155b MultiGBASE-T1 PMA status register bit definitions

Bits(s)	Name	Description	R/W[a]
1.2310.15:12	Reserved	Value always 0	RO
1.2310.11	MultiGBASE-T1 OAM Ability	1 = PHY has MultiGBASE-T1 OAM ability 0 = PHY does not have MultiGBASE-T1 OAM ability	RO
1.2310.10	EEE Ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2310.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2310.8	Low-power ability	1 = PHY has low-power ability 0 = PHY does not have low-power ability	RO
1.2310.7:3	Reserved	Value always 0	RO
1.2310.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2310.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.2310.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

[a]RO = Read only, LL = Latching low

45.2.1.193.3 Receive fault ability (1.2310.9)

When read as a one, bit 1.2310.9 indicates that the MultiGBASE-T1 PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2310.9 indicates that the MultiGBASE-T1 PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.193.4 Low-power ability (1.2310.8)

When read as a one, bit 1.2310.8 indicates that the MultiGBASE-T1 PMA/PMD supports the low-power ability. When read as a zero, bit 1.2310.8 indicates that the MultiGBASE-T1 PMA/PMD does not support the low-power feature. If the MultiGBASE-T1 PMA/PMD supports the low-power feature, then it is controlled using either bit 1.2318.11 or bit 1.0.11.

45.2.1.193.5 Receive polarity (1.2310.2)

When read as zero, bit 1.2310.2 indicates that the polarity of the receiver is not reversed. When read as one, bit 1.2310.2 indicates that the polarity of receiver is reversed.

45.2.1.193.6 Receive fault (1.2310.1)

When read as a one, bit 1.2310.1 indicates that the MultiGBASE-T1 PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2310.1 indicates that the MultiGBASE-T1 PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2310.9. The MultiGBASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit.

45.2.1.193.7 Receive link status (1.2310.0)

When read as a one, bit 1.2310.0 indicates that the MultiGBASE-T1 PMA/PMD receive link is up. When read as a zero, bit 1.2310.0 indicates that the MultiGBASE-T1 PMA/PMD receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.194 MultiGBASE-T1 training register (1.2311)

The assignment of bits in the MultiGBASE-T1 training register is shown in Table 45–155c.

Table 45-155c MultiGBASE-T1 training register bit definitions

Bits(s)	Name	Description	R/W[a]
1.2311.15:11	Reserved	Value always 0	RO
1.2311.10:4	User field	7-bit user defined field to send to the link partner	R/W
1.2311.3:2	Reserved	Value always 0	RO
1.2311.1	MultiGBASE-T1 OAM advertisement	1 = MultiGBASE-T1 OAM ability advertised to link partner 0 = MultiGBASE-T1 OAM ability not advertised to link partner	R/W
1.2311.0	EEE advertisement	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.194.1 User field (1.2311.10:4)

This register is a user defined 7-bit field that is transmitted to the link partner during training.

45.2.1.194.2 MultiGBASE-T1 OAM advertisement (1.2311.1)

When set as a one, this bit indicates to the link partner that the MultiGBASE-T1 PHY is advertising MultiGBASE-T1 OAM capability. When set as a zero, this bit indicates to the link partner that the MultiGBASE-T1 PHY is not advertising MultiGBASE-T1 OAM capability. This bit shall be set to zero if the MultiGBASE-T1 PHY does not support MultiGBASE-T1 OAM.

45.2.1.194.3 EEE advertisement (1.2311.0)

When set as a one, this bit indicates to the link partner that the MultiGBASE-T1 PHY is advertising EEE capability. When set as a zero, this bit indicates to the link partner that the MultiGBASE-T1 PHY is not advertising EEE capability. This bit shall be set to zero if the MultiGBASE-T1 PHY does not support EEE.

45.2.195 MultiGBASE-T1 link partner training register (1.2312)

The assignment of bits in the MultiGBASE-T1 link partner training register is shown in Table 45–155d. The values in this register are not valid until link is up.

Table 45-155d MultiGBASE-T1 link partner training register bit definitions

Bits(s)	Name	Description	R/W[a]
1.2312.15:11	Reserved	Value always 0	RO
1.2312.10:4	Link partner user field	7-bit user defined field received from the link partner	RO
1.2312.3:2	Reserved	Value always 0	RO
1.2312.1	Link partner MultiGBASE-T1 OAM advertisement	1 = Link partner has MultiGBASE-T1 OAM ability 0 = Link partner does not have MultiGBASE-T1 OAM ability	RO
1.2312.0	Link partner EEE advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

[a]RO = Read only

45.2.1.190.1 Link partner user field (1.2312.10:4)

This register is a user defined 7-bit field that is received from the link partner during training.

45.2.1.190.2 Link partner MultiGBASE-T1 OAM advertisement (1.2312.1)

When read as a one, this bit indicates the link partner is advertising MultiGBASE-T1 OAM capability. When read as a zero, this bit indicates the link partner is not advertising MultiGBASE-T1 OAM capability. MultiGBASE-T1

OAM capability shall be enabled only when both the local device and its link partner are advertising MultiGBASE-T1 OAM capability.

45.2.1.190.3 Link partner EEE advertisement (1.2312.0)

When read as a one, this bit indicates the link partner is advertising EEE capability. When read as a zero, this bit indicates the link partner is not advertising EEE capability. EEE capability shall be enabled only when both the local device and its link partner are advertising EEE capability.

45.2.196 MultiGBASE-T1 test mode control register (1.2313)

The assignment of bits in the MultiGBASE-T1 test mode control register is shown in Table 45–155e. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45-155e MultiGBASE-T1 test mode control register bit definitions

Bits(s)	Name	Description	R/W[a]
1.2313.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Reserved 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2313.12:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

45.2.1.196.1 Test mode control (1.2313.15:13)

Transmitter test mode operations defined by bits 1.2313.15:13, are described in 149.5.1 and Table 149–7. The default value for bits 1.2313.15:13 is zero.

Editor's Note (to be removed prior to Working Group ballot): Other PMA/PMD registers common in BASE-T PHYs which may be considered follow, if adopted, these would also need to be added to Table 45-3

45.2.3.71 MultiGBASE-T1 SNR operating margin register (Register 1.2314)

Register 1.2314 contains the current SNR operating margin measured at the slicer input for the PMAs in the MultiGBASE-T1 set. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.3.72 MultiGBASE-T1 Minimum margin register (Register 1.2315)

Register 1.2315 contains a latched copy of the lowest value observed in the MultiGBASE-T1 SNR operating margin register (1.2314) since the last read. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.3.72 MultiGBASE-T1 RX signal power register (Register 1.2316)

The MultiGBASE-T1 RX signal power register is read only and contains the receive signal power measured at the MDI. The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or PMA_Training_Init_S (as appropriate, see 55.4.6.1, 113.4.6.1, and 126.4.6.1), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

Editor's Note (to be removed prior to Working Group ballot): The group should consider whether to follow the fault model in 1000BASE-T1 and have an optional "PMA receive fault" along with a "PCS fault" or the model of other 10G/25G and faster PHYs which have an optional PMA receive fault (latched) and an optional PMA transmit fault latched.

(my recommendation is not to add the extra optional bit and stick with the model in 1000BASE-T1)

If the higher speed model is followed, in addition to the PMA transmit fault bit being added to the PMA status register, a bit for "PMA transmit fault ability" needs to be added to the same register. Both the transmit and receive fault bits would be latching high in this model. Text describing the transmit fault would need to be added to clause 149 and the existing text would have to be checked for consistency with 10G receive faults. Additionally, the MultiGBASE-T1 PCS fault bit would be removed from the MultiGBASE-T1 PCS status 1 register.

45.2.3 PCS Registers

Insert new rows to Table 45-176 for registers 1.2318 – 1.2320 after row for register 1.2317, and adjust reserved row as shown (unchanged rows not shown):

Table 45-176 PCS registers

Register address	Register name	Subclause
3.2318	MultiGBASE-T1 PCS control	45.2.3.76
3.2319	MultiGBASE-T1 PCS status 1	45.2.3.77
3.2320	MultiGBASE-T1 PCS status 2	45.2.3.78
~~3.2318~~3.2321 through 32767	Reserved	

Editor's Note (to be removed prior to Working Group ballot): Registers for OAM channel need to be added to Table 45-176 once the group decides on the number and form. Additionally, if registers read latching bits, a shadow register for reading those bits remotely is recommended to be added.

Insert 45.2.3.76 through 45.2.1.78 and Tables 45-244a through 45-244c after 45.2.3.75.

45.2.3.76 MultiGBASE-T1 PCS control register (Register 3.2318)

The assignment of bits in the MultiGBASE-T1 PCS control register is shown in Table 45–244a. The default value for each bit of the MultiGBASE-T1 PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45-244a MultiGBASE-T1 PCS control register bit definitions

Bits(s)	Name	Description	R/W[a]
3.2318.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2318.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2318.10:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.76.1 PCS reset (3.2318.15)

Resetting the MultiGBASE-T1 PCS is accomplished by setting bit 3.2318.15 to a one. This action shall set all MultiGBASE-T1 PCS registers to their default states. As a consequence, this action may change the internal state of the MultiGBASE-T1 PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the MultiGBASE-T1 PCS shall return a value of one in bit 3.2318.15 when a reset is in progress; otherwise, it shall return a value of zero. The MultiGBASE-T1 PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2318.15. During a reset, a PCS shall respond to reads from register bits 3.0.15, 3.8.15:14, and 3.2318.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2318.15 is a copy of 3.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the MultiGBASE-T1 PCS.

45.2.3.76.2 Loopback (3.2318.14)

The MultiGBASE-T1 PCS shall be placed in a loopback mode of operation when bit 3.2318.14 is set to a one. When bit 3. 2318.14 is set to a one, the MultiGBASE-T1 PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2318.14 is zero.

Bit 3.2318.14 is a copy of 3.0.14 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.70 MultiGBASE-T1 PCS status 1 register (Register 3.2319)

The assignment of bits in the MultiGBASE-T1 PCS status 1 register is shown in Table 45–244b. All the bits in the MultiGBASE-T1 PCS status 1 register are read only; a write to the MultiGBASE-T1 PCS status 1 register shall have no effect.

Table 45-244b MultiGBASE-T1 PCS status 1 register bit definitions

Bits(s)	Name	Description	R/W[a]
3.2319.15:12	Reserved	Value always 0	RO
3.2319.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2319.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2319.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2319.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2319.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2319.6:3	Reserved	Value always 0	RO
3.2319.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2319.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.70.1 Tx LPI received (3.2319.11)

When read as a one, bit 3.2319.11 indicates that the transmit MultiGBASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2319.11 indicates that the MultiGBASE-T1 PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.70.2 Rx LPI received (3.2319.10)

When read as a one, bit 3.2319.10 indicates that the receive MultiGBASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2319.10 indicates that the MultiGBASE-T1 PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.70.3 Tx LPI indication (3.2319.9)

When read as a one, bit 3.2319.9 indicates that the transmit MultiGBASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2319.9 indicates that the MultiGBASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.70.4 Rx LPI indication (3.2319.8)

When read as a one, bit 3.2319.8 indicates that the receive MultiGBASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2319.8 indicates that the MultiGBASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.70.5 Fault (3.2319.7)

When read as a one, bit 3.2319.7 indicates that the MultiGBASE-T1 PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.2319.7 indicates that the MultiGBASE-T1 PCS has not detected a fault condition.

45.2.3.70.6 PCS receive link status (3.2319.2)

When read as a one, bit 3.2319.2 indicates that the MultiGBASE-T1 PCS receive link is up. When read as a zero, bit 3.2319.2 indicates that the MultiGBASE-T1 PCS receive link was down since the last read from this register. This bit is a latching low version of bit 3.2320.10. The PCS receive link status bit shall be implemented with latching low behavior.

45.2.3.71 MultiGBASE-T1 PCS status 2 register (Register 3.2320)

The assignment of bits in the MultiGBASE-T1 PCS status 2 register is shown in Table 45–244c. All the bits in the MultiGBASE-T1 PCS status 2 register are read only; a write to the MultiGBASE-T1 PCS status 2 register shall have no effect.

Table 45-244c MultiGBASE-T1 PCS status 2 register bit definitions

Bits(s)	Name	Description	R/W[a]
3.2320.15:11	Reserved	Value always 0	RO
3.2320.10	Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO
3.2320.9	PCS high BER	1 = PCS reporting a high BER 0 = PCS not reporting a high BER	RO
3.2320.8	PCS block lock	1 = PCS locked to received blocks 0 = PCS not locked to received blocks	RO
3.2320.7	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LH
3.2320.6	Latched block lock	1 = PCS has not lost block lock 0 = PCS has lost block lock	RO/LL
3.2320.5:0	BER count	1 = Fault condition detected 0 = Fault condition not detected	RO/NR

[a]RO = Read only, LH = Latching High, LL = Latching Low, NR = Non Roll-over

45.2.3.71.1 Receive link status (3.2320.10)

When read as a one, bit 3.2320.10 indicates that the MultiGBASE-T1 PCS is in a fully operational state. When read as a zero, bit 3.2320.10 indicates that the MultiGBASE-T1 PCS is not fully operational. This bit is a reflection of the PCS_status variable defined in 149.3.7.1.

45.2.3.71.2 PCS high BER (3.2320.9)

When read as a one, bit 3.2320.9 indicates that the MultiGBASE-T1 PCS receiver is detecting a BER of > 4×10^{-4}. When read as a zero, bit 3.2320.9 indicates that the MultiGBASE-T1 PCS is not detecting a BER of > 4×10^{-4}. This bit is a reflection of the state of the hi_rfer variable defined in 149.3.7.1.

45.2.3.71.3 PCS block lock (3.2320.8)

When read as a one, bit 3.2320.8 indicates that the MultiGBASE-T1 PCS receiver has block lock. When read as a zero, bit 3.2320.8 indicates that the MultiGBASE-T1 PCS receiver has not achieved block lock. This bit is a reflection of the state of the block_lock variable defined in 149.3.7.1.

45.2.3.71.4 Latched high BER (3.2320.7)

When read as a one, bit 3.2320.7 indicates that the MultiGBASE-T1 PCS has detected a high BER one or more times since the register was last read. When read as a zero, bit 3.2320.7 indicates that the MultiGBASE-T1 PCS has not detected a high BER. The latched high BER bit shall be implemented with latching high behavior. This bit is a latching high version of the MultiGBASE-T1 PCS high BER status bit (3.2320.9).

45.2.3.71.5 Latched block lock (3.2320.6)

When read as a one, bit 3.2320.6 indicates that the MultiGBASE-T1 PCS has achieved block lock. When read as a zero, bit 3.2320.6 indicates that the MultiGBASE-T1 PCS has lost block lock one or more times since the register was last read. The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the MultiGBASE-T1 PCS block lock status bit (3.2320.8).

45.2.3.71.6 BER count (3.2320.5:0)

The BER counter formed by bits 3.2320.5:0 is a six bit count as defined by RFER_count in 149.3.7.2. These bits shall be reset to all zeros when the MultiGBASE-T1 PCS status 2 register is read by the management function or upon execution of the MultiGBASE-T1 PCS reset. These bits shall be held at all ones in the case of overflow.

Editor's Note (to be removed prior to Working Group ballot): Registers for OAM channel need to be added here once the group decides. Additionally, if registers read latching bits, a shadow register for reading those bits remotely is recommended. A model for the register to be read by the OAM channel is shown below.

45.2.u.v MultiGBASE-T1 PHY status register (Register x.yyyy)

The assignment of bits in the MultiGBASE-T1 PHY status register is shown in Table 45–zzz. All the bits in the MultiGBASE-T1 PHY status register are read only; a write to the MultiGBASE-T1 PHY status register shall have no effect.

Table 45-zzz MultiGBASE-T1 PHY status register bit definitions

Bits(s)	Name	Description	R/W[a]
x.yyyy.15:13	Alarm Status Word	15 14 13 1 1 1 All notifications false (no issues) 1 1 0 Transmission lines swapped 1 0 1 Reserved 1 0 0 Degraded link segment 0 1 1 No messages from MAC 0 1 0 PHY internal temperature warning 0 0 1 PHY power supply warning 0 0 0 Status Invalid	RO
x.yyyy.12:11	PMA SNR alarm	12 11 1 1 PHY SNR is good 1 0 PHY SNR is marginal 0 1 Request link partner exit EEE to improve SNR 0 0 PHY link is failing	RO
x.yyyy.10:0	Reserved	Value always 0	RO

45.2.u.v Alarm Status Word (x.yyyy.15:13)

Bits 15:3 of register x.yyyy indicate the alarm status word. The alarm status word is implementation-specific. For a recommended interpretation see Annex 149A. Implementation of this register is optional.

45.2.3.71.6 PMA SNR alarm (x.yyyy.12:11)

Bits 12:11 of register x.yyyy indicate the status of the PMA SNR at the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent. A value of 1 1 indicates that the receiver SNR is good. A value of 1 0 indicates that the receiver SNR is marginal, but not yet failing. A value of 0 1 in the PMA SNR alarm requests the link partner to exit the quiet/refresh cycle of EEE and resume transmitting normal idles. When not receiving LPI quiet/refresh cycles, the value 0 1 shall not be used. A value of 0 0 indicates the PHY is about to drop link and initiate a retrain. Implementation of this register is optional.