Multi-Gig PHYs Channel Code Proposal

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Motivation

- Progress so far within IEEE802.3ch since May 2018
- 10GBASE-T1
  - 2 and 2.5bits/symbol are optimal from SNR point of view
- 2.5GBASE-T1
  - 1 to 2.5bits/symbol are optimal from SNR point of view
- Consensus within a group to choose RS as FEC for Multi-Gig
- Tu (tu_3ch_01a_0718.pdf) and Farjadrad (farjarad_3chah_01b_061218.pdf) suggest to use interleaving to reduce the FEC complexity
- Wu (wu_3ch_01a_0518.pdf) and McClellan (McClellan_3ch_01a_0518.pdf) suggest to use 1000BASE-T1 FEC

Criterion for Choosing RS FEC Parameters

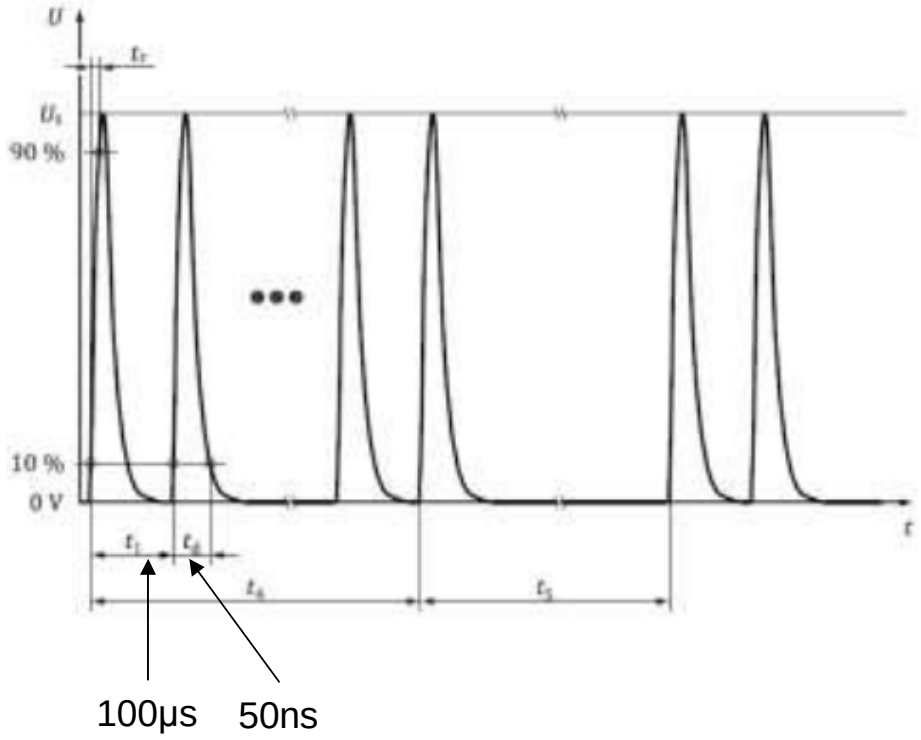
- Reed-Solomon codes RS(N,K,T) with m-bits
  - N: # of symbols after channel code ($N<2^m$)
  - K: # of symbols before channel code
  - T: # of symbols that can be corrected among n
  - where, T=(N-K)/2
- In general RS decoder complexity increases
  - Exponetially with m (farjarad_3chah_01b_061218.pdf also sees this)
  - $O(T^2)$ as length of t increases
    - Multiplier, adder, inverse function, and registers
  - $O(N)$ as length of N
- Complexity translates into
  - power
  - latency → $O(T)$ and $O(N)$

10GBASE-T1 RS Code

- RS code options exploration from Tu (tu_3ch_01b_0518.pdf)
  - Correction time (T) < 51ns can be done with RS bits (m) = 9 bits
  - While for correction time (T) > 51ns needs at least m = 10 bits
- Interleaving is a good option to keep RS decoder simple
  - farjarad_3chah_01b_061218.pdf and tu_3ch_01a_0718.pdf
  - With a penalty of added latency
- Channel code overhead is ~12%
- 1 RS code for OAM bit

Required Burst Error Correction Length

- Sources
  - Transient Impulse (ISO 7637-3)
    - 50ns with period of 100µs
  - Narrow Band RF Interferences
  - DFE error propagation
- 2.5GBASE-T1
  - Needs FEC with burst error correction length of ~80ns
- 10GBASE-T1
  - Needs FEC with burst correction length of ~65ns



RS FEC Proposals for Multi-Gig PHYs

- Encoding
  - 256B/257B for all speeds
- 2.5GBASE-T1
  - PAM4: 8-bits RS code (217,194,11) with L = 1 or 2 → 81.2ns (max)
    - Frame latency = 617ns
  - PAM3: 9-bits RS code (449, 409,24) with L = 1 → 85.9ns (max)
    - Frame latency = 720ns
- 10GBASE-T1 → PAM4
  - 10-bits RS code (692,618,37) with L = 1 or 2 → 66.2ns (max)
    - Frame latency = 615ns
- If needed interleaving level (L) can be higher than above

Conclusion

- Interleaving can be adopted for all speeds to make FEC less complex for power and area stand point
- But, need to understand the latency requirement to identify the interleaving levels
- There exists power and cost efficient FEC solution for 2.5GBASE-T1
  - Identifying FEC parameters from 10GBASE-T1 is very inefficient!
- 2.5GBASE-T1 RS code 8-bits (L = 1 or 2) and 9-bits (L = 1) meet the correction requirement
- 10GBASE-T1 RS code 10-bits (L = 2) meets the correction requirement

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