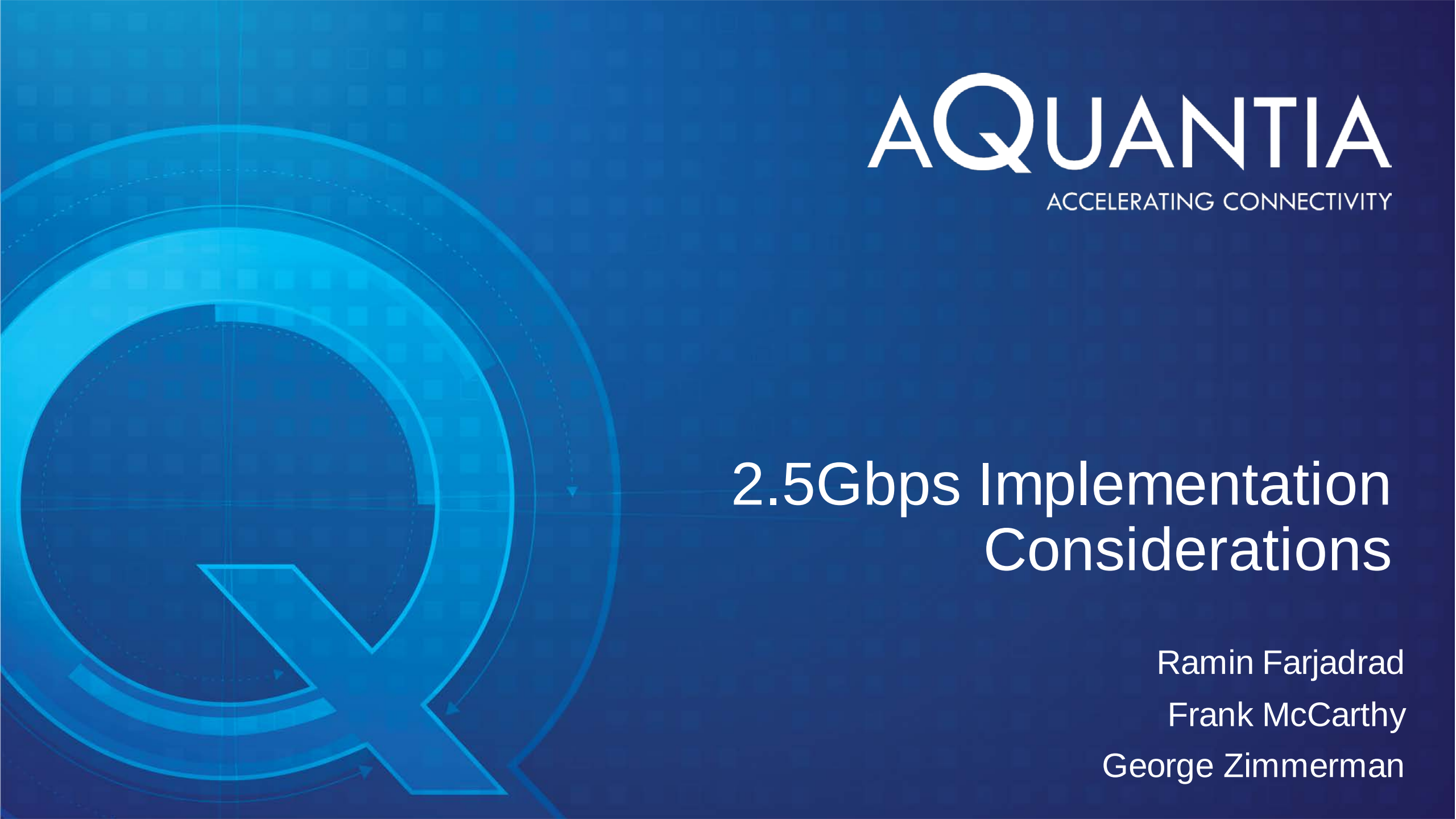


2.5Gbps Implementation Considerations

Ramin Farjadrad
Frank McCarthy
George Zimmerman

2.5Gbps as a Scaled Up Version of 1000BASE-T1

- A proper 2.5Gbps PHY needs full new analysis and design, and not a simple job of scaling up the 1000BASE-T1 scheme
  - Specified Channel for 1G standard is different from 2.5G standard: UTP vs. STP
    - Example: The UTP channel in 1G forced selection of PAM3 to solve Transmit EM emission, while 2.5Gbps running on STP, so it would be wrong to burden 2.5Gbps scheme with similar UTP restriction

    → Opens up the possibility of running at higher baud rate vs. increasing the PAM levels
  - Either case of higher baud rate or PAM levels means the SNR will be lower, thus necessitates recovering SNR margin elsewhere.
    - Thus tradeoffs of the channel/noise environment must be carefully analyzed with the new scheme
    - A shielded channel buys some immunity, but the analog front end will also likely need a full redesign with higher complexity.
  - The FEC used for 1000BASE-T1 can not be simply selected for 2.5Gbps
    - It may not provide the necessary coding gain, nor be able to deal with other effects such as DFE burst errors or Impulse events that cover many more symbols.
    - So a new FEC is to be proposed or at least the same FEC must be fully reevaluated from scratch

2.5Gbps as a Scaled Down Version of 10Gbps Mode

- The specified channel characteristics as well as the noise environment defined in 802.3ch is the same for 2.5G/5G/10G.
  - Therefore, once the committee converges on a modulation, FEC, PCS coding scheme for 10Gbps, the same scheme is guaranteed to work for to get 2.5G and 5G by a simply scaling down of the baud rate or modulation level or both.
  - For example: If committee converges at PAM4 at 5.6Gbaud with a 12% overhead FEC for 10Gbps mode, then without any additional analysis over the same channels:
    - 2.5Gbps mode is guaranteed to work with PAM2 at 2.8Gbaud with same FEC
    - 5Gbps mode is guaranteed to work with PAM2 at 5.6Gbaud or PAM4 at 2.8Gbps with same FEC
- Such selection significantly helps the committee to quickly converge on the final draft of 802.3ch standard for all 3 speeds

PAM2: The Most Mature & Low-Risk Signaling Choice

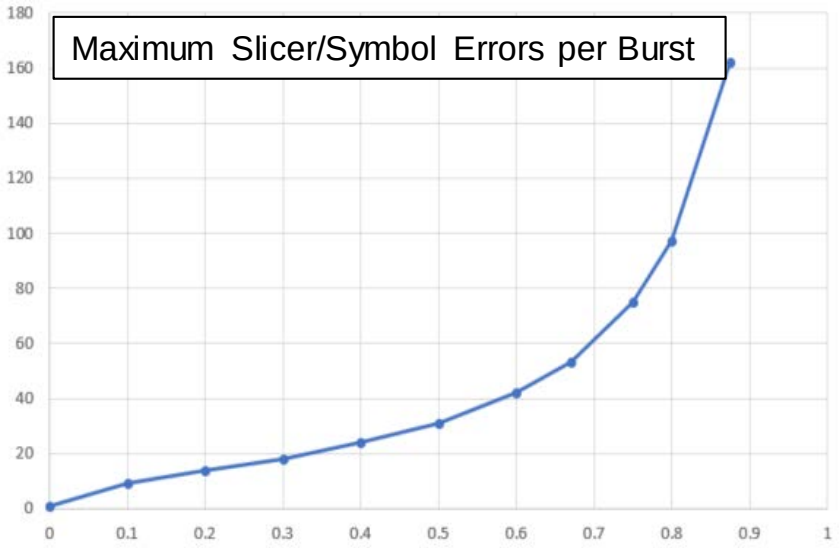
- The PAM2 is the most mature modulation that has always proven to provide the simplest, least risk and least complex architecture choice among all existing options when it provided enough SNR over the target channel
  - IEEE committees have always picked PAM2 as their first choice, and only switched to higher modulations if there was a definitive and obvious technical limitation over the target channel:
  - 802.3bj initially favored PAM4 (100GBASE-KP4) and added PAM2 (100GBASE-KR4) later, but eventually everyone designed PHYs using PAM2 for 100GBASE-KR4, despite higher channel loss at 2x rates, simply because of significant ease and robustness of PAM2 implementation
  - 802.3cd for 50GBASE-KR selected PAM4 only after lot of analysis showed PAM2 did not provide the minimum required SNR over target channels.
- In automotive applications with high level of RF interference, PAM2 offers the highest robustness to RFI, thus such modulation helps reduce the complexity or most likely even eliminate the RFI suppression block, further reducing the complexity of the implementation

PAM2: Robust to DFE Error Propagation & Best FEC Gain

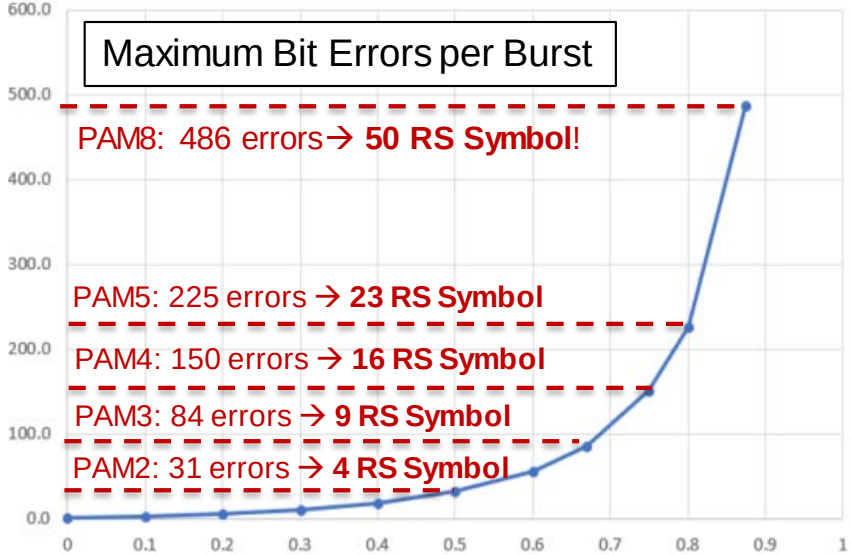
- Amogn key reasons to avoid high PAM levels is the high FEC inefficiency
  - Noises/Interference/Bursts in the link affect the received symbols

    ➔ A single symbol error leads to more bit errors for higher PAM levels
  - DFE error propagation grow exponentially with PAM level (anslow_3cd_01_0716)
  - In highly BW limited schemes that low PAM levels were not workable, DFE was avoided for this very reason!
    - Example: 10GBASE-T with 128DSQ (equivalent to PAM12) used THP instead of DFE

a: Probability of Burst Continuing



a: Probability of Burst Continuing



a: Probability of Burst Continuing

* For 1-tap DFE and Frame Error Rate of FER=~5E-10 → BER=~1E-12

PAM2: Robust to DFE Error Propagation & Best FEC Gain

- Higher the PAM levels

  →Longer the Burst error length

  → Lower the FEC coding gain (sun_nea_01a_0517)

Burst Effect on FEC Gain	PAM2 (a=0.5) Interleaving=1	PAM4 (a=0.75) Interleaving=2	PAM8 (a=0.875) Interleaving=3
FEC Coding Gain Penalty*	0.7dB	1.3dB	3.0dB

- Higher PAM levels lead to FEC gain loss due to high DFE error propagation, despite higher Interleaving FEC (thus higher complexity and higher latency) and using only 1-tap DFE

- Always best to choose the lowest level PAM that can deliver the target bit-rate at desired BER over target channel and environment

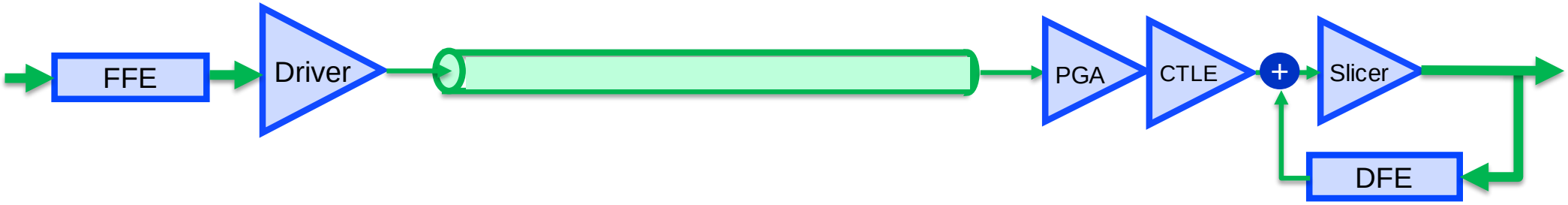
* For 1-tap DFE, KP FEC, and Frame Error Rate of FER=~5E-10 → BER=~1E-12

PAM2 Leads to Least PHY Complexity

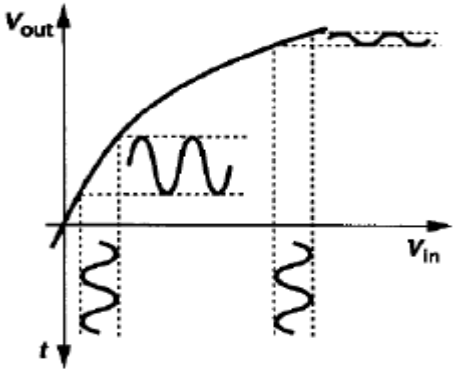
- All industry PAM2 SerDes architectures have been without ADC
  - Eliminating the ADC provides significant Area & Power savings

    → ADC usually consumes at least 30% of AFE power

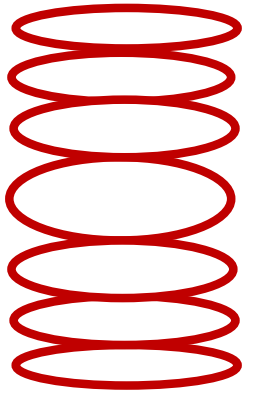
    → Additionally, Transmit FFE uses 1-bit input data, instead of multi-bit ADC output → Low DSP Area & Power
  - Mixed-mode DFE eliminates most of filter digital processing and complexity



  - PAM2 also eliminates the linearity requirement for AFE block, while higher the PAM levels, the higher the linearity AFE requirement to avoid distortion error → high linearity directly leads to higher power

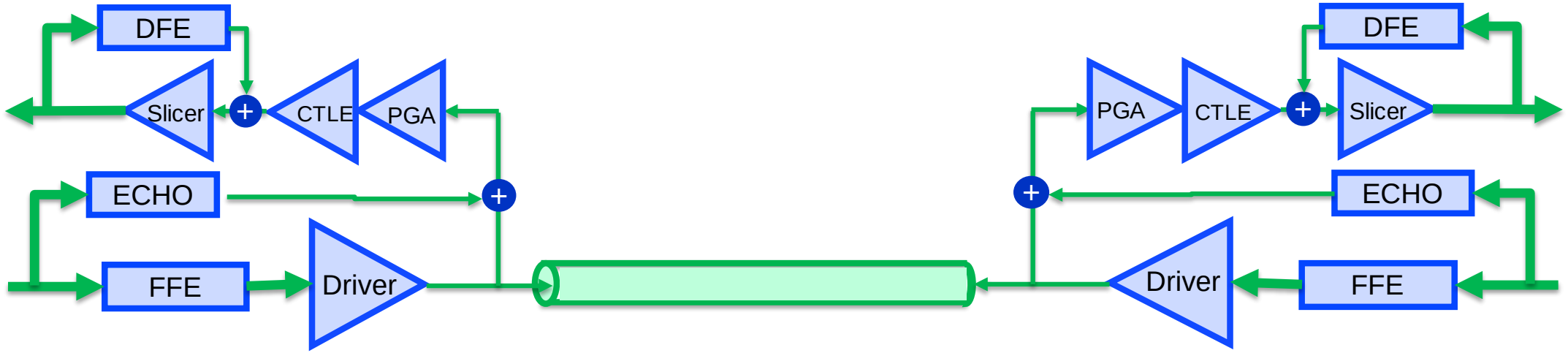


PAM8 with distortion



PAM2 Leads to Least PHY Complexity

- A bidirectional ADC-less PHY architecture provide similar benefits
  - Echo Canceller can be implemented in mixed-mode fashion similar to DFE
  - There is a much higher linearity requirement for Echo cancellation than a unidirectional PAM-N SerDes
    - The AFE must have much better linearity than the required Echo cancellation
    - This requirement exists even for PAM2
  - PAM2 modulation reduces AFE linearity requirements significantly



2.5Gbps Salz SNR Analysis over 802.3 d0.2.1 Limit Line

2.5Gbps	PAM2	PAM3	PAM4	PAM8
Baud rate (12% FEC Overhead) [GBaud]	2.8	1.86	1.4	0.94
Nyquist BW (FEC Overhead) [GHz]	1.4	0.93	0.7	0.47
IL @Nyquist [dB]	19.00	14.5	12.6	10
Tx Output Power (1V pkpk [dBm]	3.98	2.22	1.43	0.3
Received Signal Power [dBm]	-6.02	-6.52	-6.76	-7.05
Salz SNR Margin [dB]	31.49	29.05	26.62	20.46
Salz SNR Margin – FEC Penalty [dB]	30.79	28.05	25.32	17.46

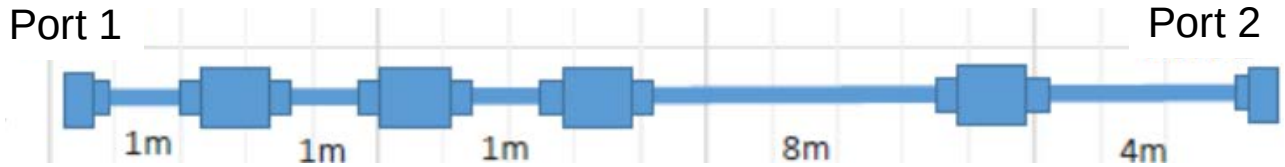
- 2.5Gbps mode over the proposed channel provides significant SNR margin for all modulations (Farjadrad_ch_01d_0318)
  - The high SNR margin must be leveraged to reduce the PHY complexity
- PAM2 shows the highest Salz SNR margin among all modulations

→ PAM2 offers the highest flexibility to trade off SNR with PHY complexity

2.5Gbps Echo Cancellation Analysis over Sample Channel

2.5Gbps	PAM2	PAM3	PAM4	PAM8
Baud rate (12% FEC Overhead) [GBaud]	2.8	1.86	1.4	0.94
Nyquist BW (FEC Overhead) [GHz]	1.4	0.93	0.7	0.47
IL @Nyquist [dB]	19.00	14.5	12.6	10
Required Residual Echo/Transmit Pwr [dB]	-33.00	-36.00	-38.50	-44.00
Echo Signal Power RL1 (at Rx input) [dBm]	-20.59	-23.45	-25.84	-28.03
Echo Signal Power RL2 (at Rx input) [dBm]	-24.17	-26.01	-27.91	-29.14
Required Echo Cancellation for RL1 [dB]	8.43	10.33	11.73	15.67
Required Echo Cancellation for RL2 [dB]	4.85	7.77	9.66	14.56

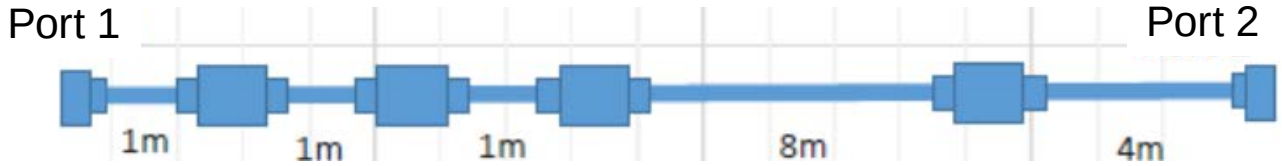
- Echo Analysis performed with different modulations over Channel-A in DiBiaso_3ch_01a_0917
  - Channel-A IL matches very closely with IL limit line
  - Channel-A RLs are worst-case of a realistic channel with four inline connectors
    - Three connectors on one side
    - Already available connectors (Not designed for multi-Gig)

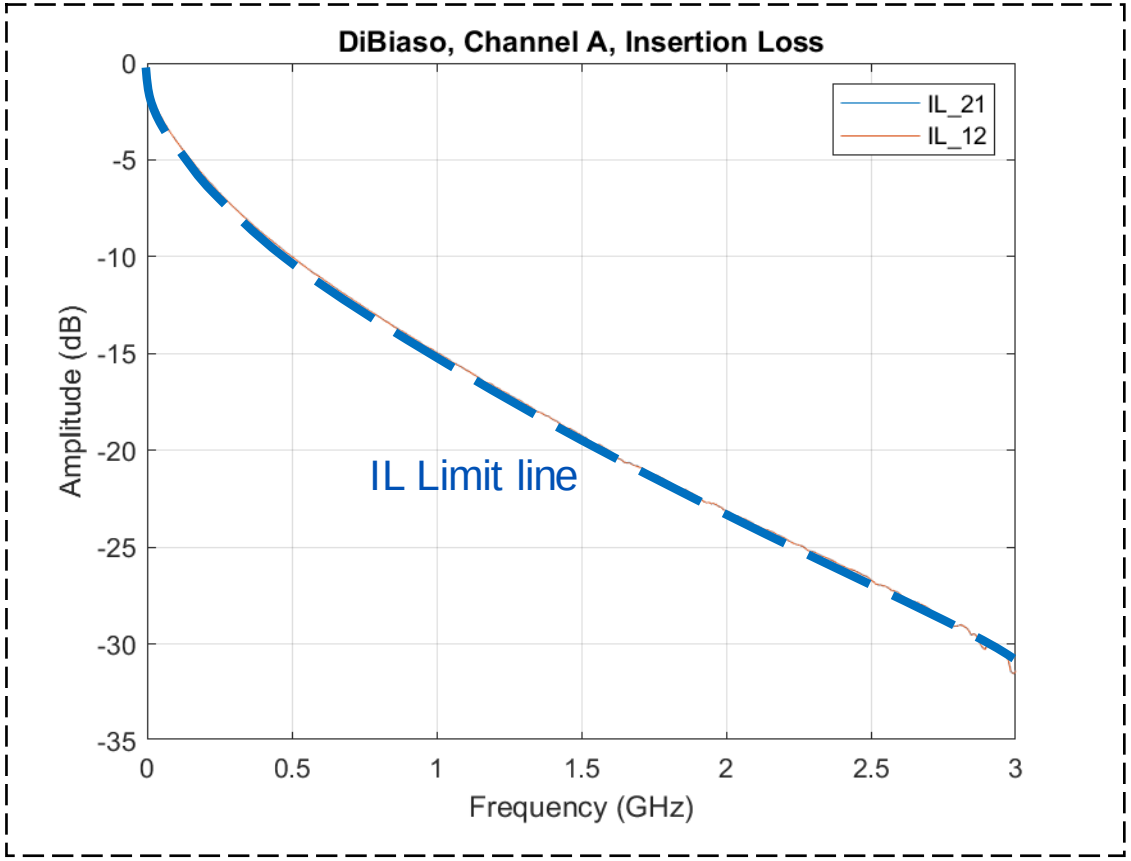


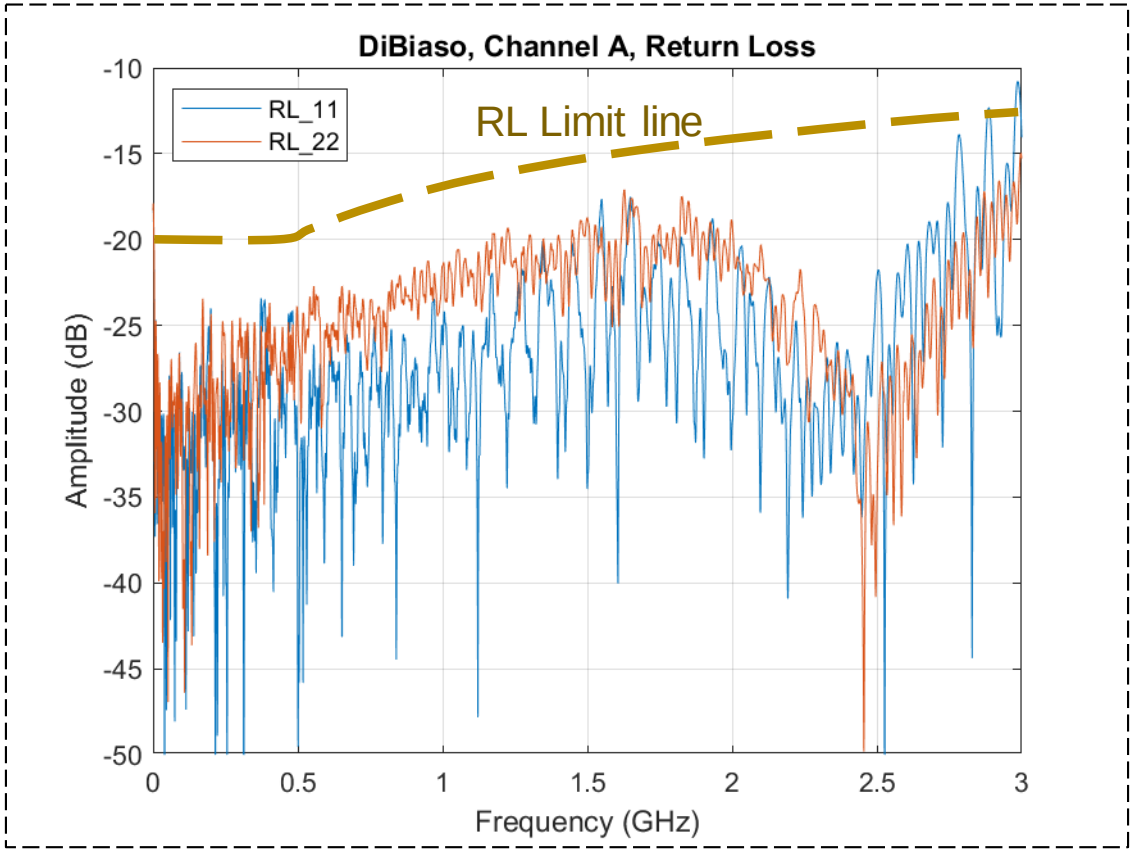
Sample Channel Characteristics

Note: This choice of channel favors lower baud rates

- IL is at the maximum allowed (highest loss at high frequencies)
- RL margin to limit line is lower for 2.8Gbaud (1.4GHz) vs. 0.94Gbaud (0.47GHz)

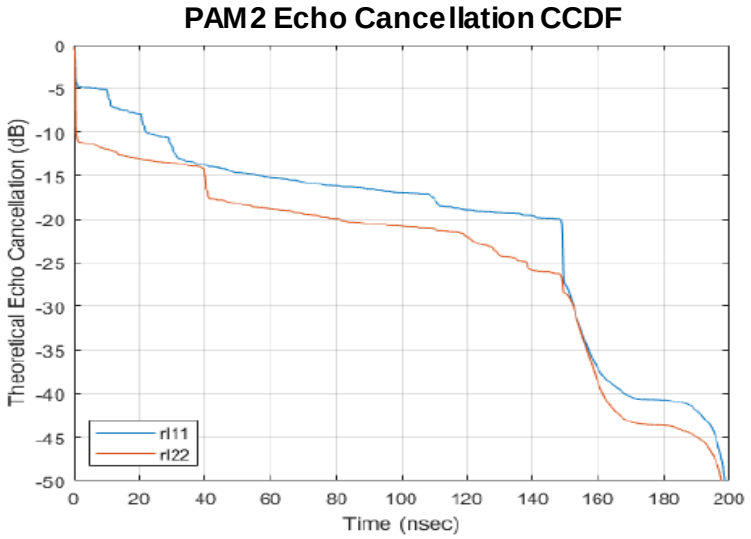


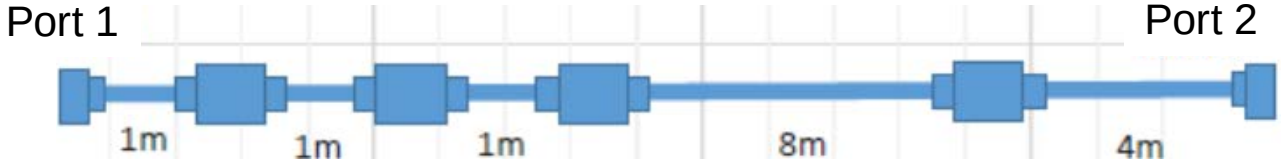


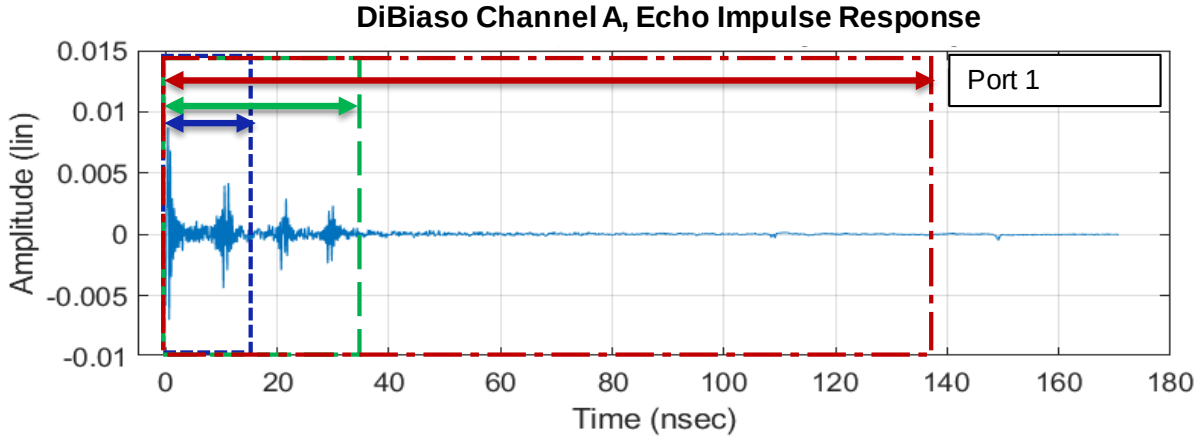


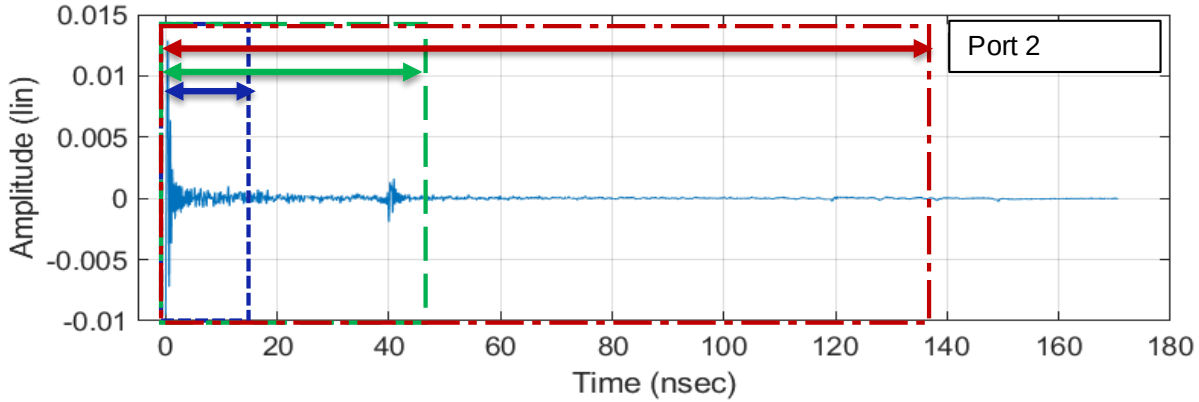
Echo Canceller Filter Length vs. Echo Suppression

- The channel Echo impulse response is independent of our choice of modulation or baud rate
  - Reflections occur at a certain time regardless of the signal
  - To cancel certain reflections, the length of Echo cancellers stays the same in time unit (e.g. nsec)
    - But the number of cancellers taps is inversely proportional to baud rate
  - However, Echo response magnitude is a function of the signal baud rate, PAM levels, and pulse shape
- Complementary Cumulative Distribution Function (CCDF) is used to calculate the residual Echo power after cancelling Echo for a certain length in time relative to uncancelled Echo power



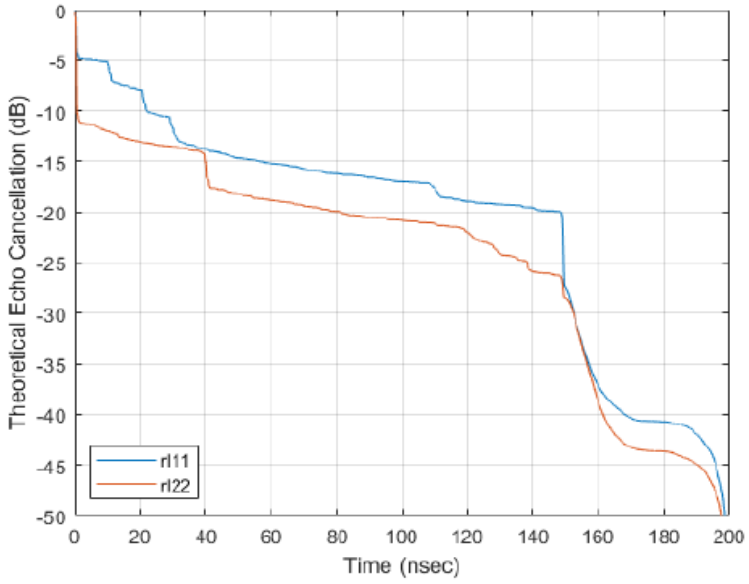




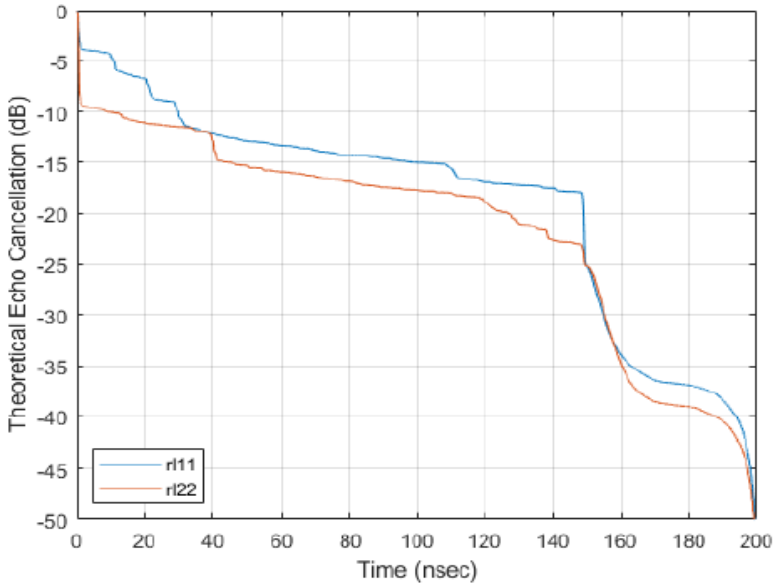


2.5Gbps Residual Echo Power Post Cancellation

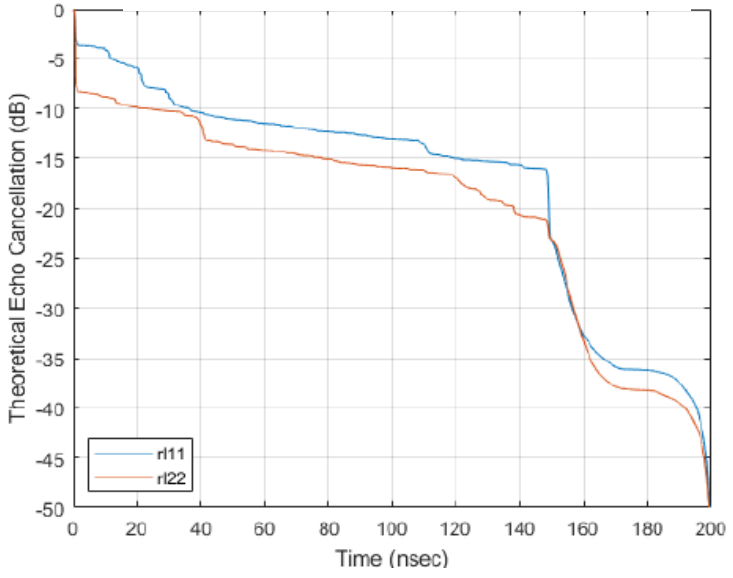
PAM2 Echo Cancellation CCDF



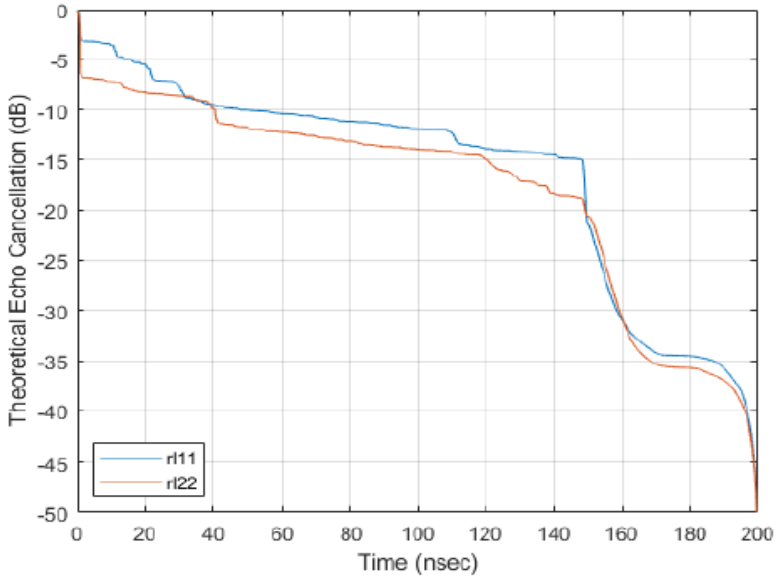
PAM3 Echo Cancellation CCDF



PAM4 Echo Cancellation CCDF



PAM8 Echo Cancellation CCDF



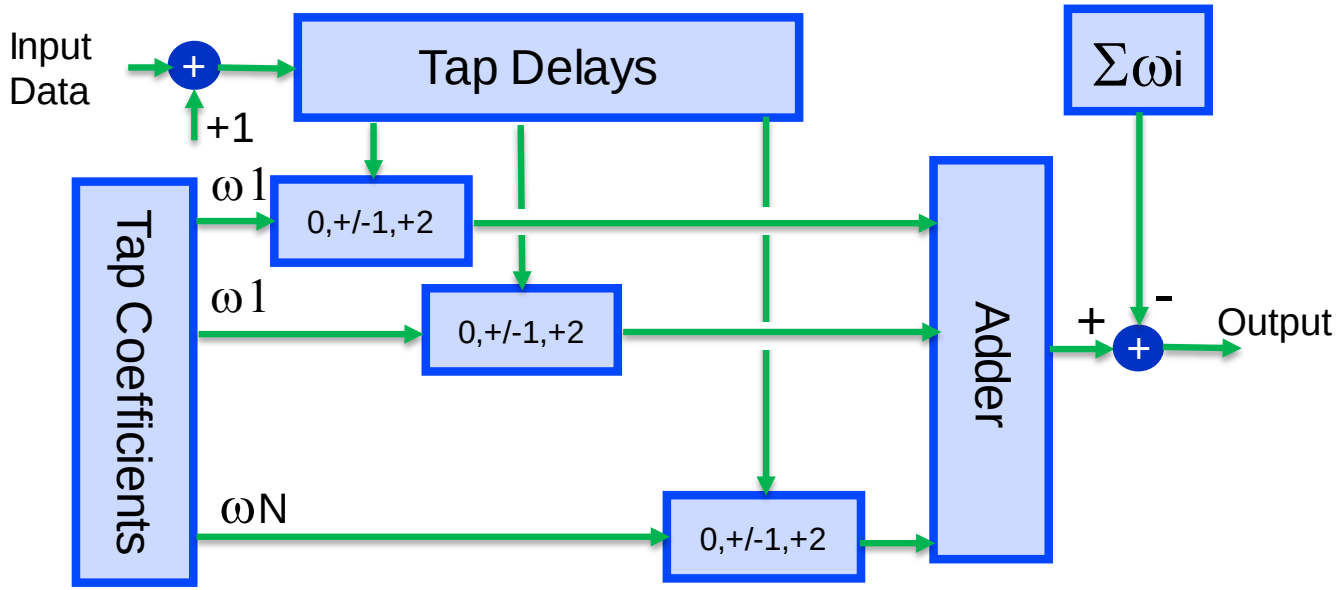
- Echo CCDF plot shows how much the Echo power at Rx input is suppressed as a function of the length (in nsec) of an ideal Echo Canceller
  - The number of Echo Canceller taps per nsec vary per baud rate
    - PAM2 (2.80Gbaud): 20n→ 56taps
    - PAM3 (1.86Gbaud): 20n→ 39taps
    - PAM4 (1.40Gbaud): 20n→ 28taps
    - PAM8 (0.94Gbaud): 20n→ 19taps

2.5Gbps	PAM2	PAM3	PAM4	PAM8
Baud rate (12% FEC Overhead) [GBaud]	2.8	1.86	1.4	0.94
Echo Signal Power RL1 (at Rx input) [dBm]	-24.17	-26.01	-27.91	-29.14
Echo Signal Power RL2 (at Rx input) [dBm]	-20.59	-23.45	-25.84	-28.03
Required Echo Cancellation for RL1 [dB]	4.85	7.77	9.66	14.56
Required Echo Cancellation for RL2 [dB]	8.43	10.33	11.73	15.67
Min # of Canceller taps for RL1	**<10**	**<10**	**64**	**110**
Min # of Canceller taps for RL2	**56**	**58**	**72**	**140**

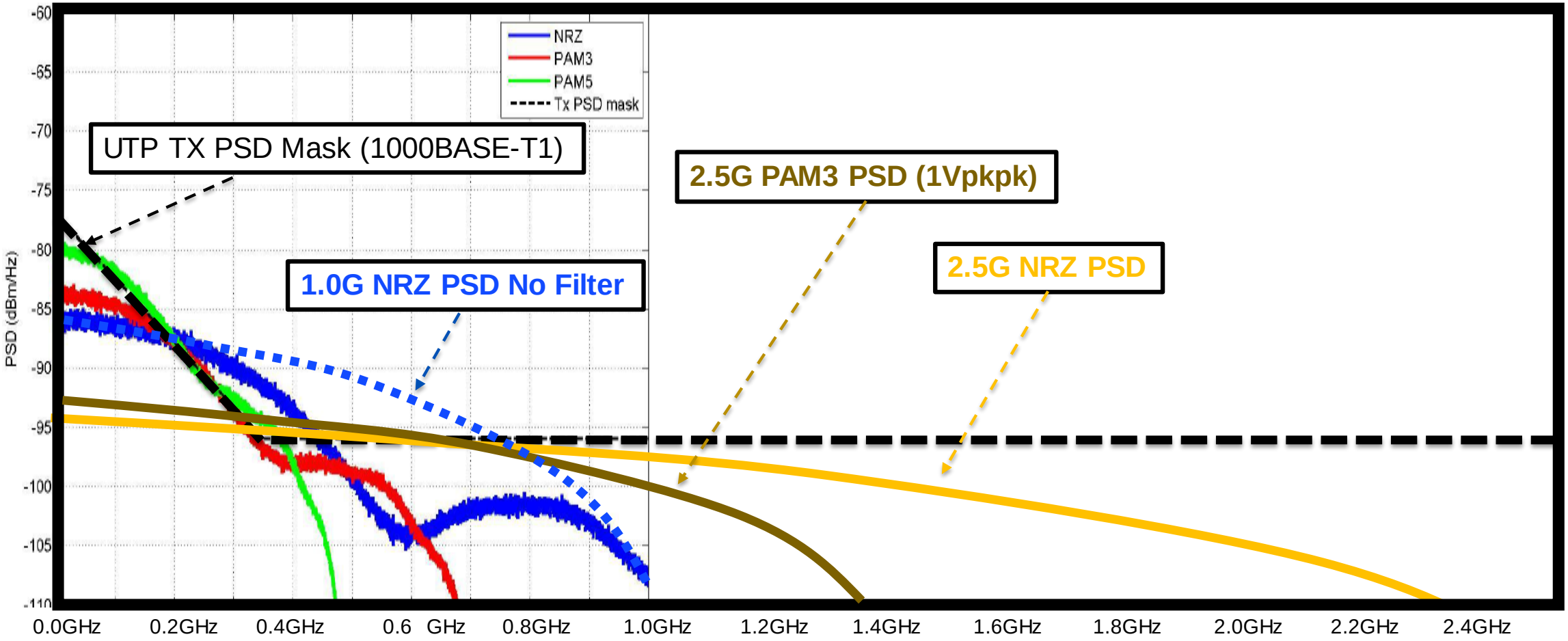
2.5Gbps Echo Canceller Complexity Analysis

2.5Gbps	PAM2	PAM3	PAM4	PAM8
Baud rate (12% FEC Overhead) [GBaud]	2.8	1.86	1.4	0.94
Echo Signal Power RL1 (at Rx input) [dBm]	-24.17	-26.01	-27.91	-29.14
Echo Signal Power RL2 (at Rx input) [dBm]	-20.59	-23.45	-25.84	-28.03
Required Echo Cancellation for RL1 [dB]	4.85	7.77	9.66	14.56
Required Echo Cancellation for RL2 [dB]	8.43	10.33	11.73	15.67
Min # of Canceller taps for RL1	<10	<10	64	110
Min # of Canceller taps for RL2	52	56	72	140
Required Echo Canceller Tap Resolution [bits]	7	7	8	9
Input Data to Echo Canceller [bits]	1	2	2	3
Echo Canceller Area/Tap [um^2]	695	1390	1589	2346
Echo Canceller Area/Tap (No Multplier) [um^2]	695	834	1,009	2,346
Total Echo Canceller Area [mm^2]	0.0389	0.0484	0.0727	0.3284
Relative Echo Canceller Area [um^2]	1.0	1.25	1.9	8.4

- Lower PAM level, with higher SNR margin, can use lower Filter Tap Coefficient resolution to lower complexity
- PAM2/PAM3/PAM4 can eliminate multipliers all together, and only use Booth-recoded partial products (e.g. simple shift function) at each filter tap
  - Example for a PAM4 FIR without Multipliers



2.5Gbps Transmit PSD Requirements



- 1000BASE-T1 selection of UTP cable necessitated transmit PSD limit line to meet EM emission specs
- Higher baud (spreads power over wider range) → Lower PSD level (e.g. 2.5G-NRZ 4dB below 1G-NRZ)
- At same transmit power → PAM2 provides best Tx PSD for emission spec
- **Minimal shielding attenuation of ~10dB provides lots of margin → Any STP cables provides this**

PAM2: Most Compatible to other Modulation Schemes

- PAM2 with 1bit per symbol does not create any grouping restriction
  - It won't place any requirement of conversion order of Mux/Demux from parallel bits to serial line symbols
  - It also won't place any requirement on number of bits per FEC symbols
    - Typically we need to make sure the bits carried by a single line symbol are not spread between two RS FEC symbols, leading to poorer FEC performance in case of an error in a line symbol
      - → We don't want a single PAM symbol error causes more than a single RS FEC symbol error
      - → PAM2 with 1 bit/symbol is compatible with any other PAM modulations and even/odd bits in FEC

Conclusion

- Historically, IEEE has always selected the lowest PAM level modulation that met the target bit rate and BER performance
- PAM2 modulation provides the highest SNR margin compared to all other PAMs
  - This highest SNR margin can be traded off for lowest PHY complexity
    - AFE: No ADC and minimal linearity requirement leads to significant power/area saving
    - Minimum Echo cancellation requirement→ Lowest DSP/Echo canceller complexity
    - Minimum DFE error propagation → Minimum FEC coding gain loss
      - No FEC Interleaving required and Even higher SNR margin to trade off
- PAM2 provides best transmit PSD emission mask compared to all other PAMs
- 2.5Gbps/PAM2 can be an scaled version of 10Gbps/PAM-N at lower baud rate
  - Simplified 10G scheme (DFE, FFE, FEC, etc) guaranteed to work→ No Separate standard path
- PAM2 with 1bit/symbol is compatible with any other PAM modulation
  - Flexibility for both backward and forward compatibility

Thank you.