Proposed Comment on Master Jitter Spec for Initial Working Group Ballot

Comment:
The jitter test in 149.5.2.3.1 is designed for the low-frequency square wave signal used in BASE-T PHYs and the test in 149.5.2.3.2 is designed for the at-speed test patterns (JP03A & JP03B) used in backplane phys. A control bit is needed to allow test mode 2 to support both tests, and additional language is needed specifying which signals to use in which tests.

Suggested Remedy:
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45.2.1.196 MultiGBASE-T1 test mode control register (1.2313)

Table 45-155e: Add new rows after Reserved row, and adjust reserved row to allocate bits 0,1 of register 1.2313 (Test mode control) register based:

Register Bits	Name	Description
1.2313.1:0	Jitter test control	00 01
		0 0: Normal square wave
		0 1: JP03A pattern
		1 0: JP03B pattern
		1 1: Reserved

Insert new subclause 45.2.1.196.2
45.2.1.196.2 Jitter test control (1.2313.1:0) : When the transmitter is in test mode 2, bits 1.2313.1:0 control the pattern of the jitter test signal. A value of 0 0 transmits a square wave from the transmitter, a value of 0 1 transmits the JP03A pattern, and a value of 1 0 transmits the JP03B pattern. See 149.5.1 for more information.

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149.5.1
Change the fourth paragraph of 149.5.1 to read:
Test mode 2 is for transmitter jitter testing on MDI when transmitter is in MASTER timing mode. When test mode 2 is enabled, the PHY shall transmit the pattern controlled by bits 1.2313.1:0, as shown in Table 149-15a, with the transmitted symbols timed from its local clock source.

Table 149-15a Jitter test modes

Bit 1.2313.1	Bit 1.2313.0	Pattern
0	0	Square wave: a continuous pattern of 16*S {+1} symbols followed by 16*S {–1} symbols
0	1	JP03A: a continuous pattern of JP03A (as specified in 94.2.9.1)
1	0	JP03B: a continuous pattern of JP03B (as specified in 94.2.9.2)
1	1	Reserved

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149.5.2.3.1
Change first sentence from:

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 and using test fixture 3 as shown in Figure 149–38
To:
In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 with the square wave pattern (see Table 149-15a) and using test fixture 3 as shown in Figure 149–38

149.5.2.3.2
Change first sentence from: “Jitter measurements in this subclause are performed with the transmitter enabled in Master timing mode with a local clock.”
To: “Jitter measurements in this subclause are performed with the transmitter enabled in Master timing mode in test mode 2, with either the JP03A or JP03B pattern, and timed with a local clock.”