The following text shows the complete set of changes to be made by comments 39, 40, 41, 117, 119, 120, and 200

149.5.1 Test Modes

...

Test mode 2 is for transmitter jitter testing on MDI when transmitter is in MASTER timing mode. When test mode 2 is enabled, the PHY shall transmit a continuous pattern of JP03A (as specified in 94.2.9.1) or JP03B (as specified in 94.2.9.2) with the transmitted symbols timed from its local clock source.

...

Test mode 4 is for transmitter linearity testing. When test mode 4 is enabled, the PHY shall transmit **a continuous pattern of PRBS13Q (as specified in 120.5.11.2.1)**~~the transmitter linearity test pattern defined in 94.2.9.4~~.

...

149.5.2.2 Transmitter linearity

With the transmitter in test mode 4 and using the transmitter test fixture 1 shown in Figure 149–36, the test defined in 120D.3.1.2~~94.3.12.5.1~~ shall be performed. The ideal PAM4 level of 1/3 should be used for effective symbol levels of ES1 and ES2. The transmitter ~~shall meet the~~ SNDR distortion, as specified in 120D.3.1.6, ~~94.3.12.7~~shall exceed 38 dB in 10G, 36 dB in 5G and 35 dB in 2.5G modes, respectively.~~.~~

149.5.2.3 Transmitter timing jitter

The transmitter timing jitter is measured by capturing the TX_TCLK_175 waveform in both MASTER and SLAVE configurations while in test mode 1 using the transmitter test fixture 2 shown in Figure 149–37. When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the MASTER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 1/*S* ps. The peak-to-peak value of the MASTER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 10/*S* ps. See Table 149–1 for definition of *S*.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the SLAVE TX_TCLK_175 jitter relative to an unjittered reference shall be less than 2/*S* ps. The peak-to-peak value of the SLAVE TX_TCLK_175 jitter relative to an unjittered reference shall be less than 20/*S* ps.

TX_TCLK_175 jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the capturing device shall be at least~~larger than~~ 200 MHz (this is equivalent to phase noise integration of the clock over a bandwidth of at least 100 MHz from the carrier frequency). The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK_175. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

149.5.2.3.1 Transmit MDI random jitter in master mode

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 with the square wave pattern (see Table 149-15a) and using test fixture 3 as shown in Figure 149–38. The RMS value of the MDI output jitter relative to an unjittered reference shall be less than 1/*S* ps. The peak-to-peak value of the MDI output jitter

relative to an unjittered reference shall be less than 10/*S* ps. Jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the measurement device shall be larger than 200 MHz. Unjittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

Table 149-15a – Jitter test modes

Bit 1.2313.1	Bit 1.2313.0	Test Pattern
0	0	Square wave: TX_TCLK_175
0	1	JP03A (as specified in 94.2.9.1)
1	0	JP03B (as specified in 94.2.9.2)
1	1	Reserved

149.5.2.3.2 Transmit MDI deterministic jitter in master mode

Jitter measurements in this subclause are performed with the transmitter enabled in Master timing mode in test mode 2, with the patterns as defined by Table 149-15a, and timed- with a local clock.

To measure the peak-to-peak Deterministic Jitter ($DJ_{pk\text{-}pk}$) and Even-Odd jitter ($EOJ_{pk\text{-}pk}$) follow the steps as specified in Clause 94.3.12.6.1, with following modifications to step 5:

$f_n = 1 \times S$ MHz, $T = 68 / S$ ns.

Using this method, $DJ_{pk\text{-}pk}$ shall be less than 9 / S ps.

To measure peak-to-peak Even-odd jitter ($EOJ_{pk\text{-}pk}$) follow the steps as specified in Clause 94.3.12.6.2.

Using this method, $EOJ_{pk\text{-}pk}$ shall be less than 4 / S ps.