Changes to overview descriptive text to align with the data ordering and PCS state diagrams:

149.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 149–16 and Figure 149–17, and to the PCS Transmit bit ordering in Figure 149–6 and Figure 149–7.

Dashed rectangles in Figure 149–16 and Figure 149–17 are used to indicate states and state transitions in the transmit process state diagram that shall be supported by PHYs with the EEE capability. PHYs without the EEE capability do not support these transitions.

When communicating with the XGMII, the MultiGBASE-T1 PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map ~~packets~~ between the XGMII ~~format~~ and the PMA service interface formats.

Commented [GZ1]: Do we need this? – it really seems out of place, and probably can and should be deleted (but it's a separate issue).

The subsequent functions of the PCS Transmit process then take a block of fifty 65B blocks, append a 10-bit OAM field, then add 340 bits of parity for the RS_FEC, interleave the RS-FEC symbols, and then scramble the resulting bits~~block~~. These bits are then mapped, two at a time, into a PAM4 symbol. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a PAM4 symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. A symbol period, *T*, is 1000 / (5.625 x *S)* ps. See Table 149–1 for definition of *S*.

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate a sequence (T_n) defined in 149.3.5.1 to the PMA via the PMA_UNITDATA.request primitive. These code-groups are used for training mode and only transmit the values {–1, +1}. During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See 149.4.2.5.)

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control. During transmission, the fifty blocks of 65B encoded bits are appended with a 10-bit OAM field to form the RS-FEC input frame. During data encoding, PCS Transmit utilizes ~~a~~ L-interleaved (L=1, 2, or 4) Reed Solomon encoders to generate and append ~~the~~ 340 parity check bits to form ~~a~~ 3600-bit (360, 326) RS-FEC frames which are interleaved into an L-interleaved RS-FEC superframe. ~~Then this output frame is scrambled by the PCS using a PCS scrambler. The 3600 bits in this frame are then encoded into PAM4 symbols and transferred to the PMA.~~

Commented [GZ2]: Note – this is a struck-out space after the hyphen in RS- FEC frame to make it RS-FEC frame.

Commented [GZ3]: Delete paragraph break?

~~The PHY aggregates L RS-FEC input frames into an L-interleaved (L=1, 2, or 4) RS-FEC input superframe.~~ Each RS-FEC input superframe consists of 3260 × L bits, or 326 × L Reed-Solomon message symbols. The interleaving function is integrated with the RS-FEC encoding, ~~or~~ applying ~~ies~~ a round robin interleaving scheme and distributing the 10-bit Reed-Solomon message symbols into L

RS—FEC encoders. After encoding, the RS-FEC frames from each encoder are recombined into one single interleaved RS-FEC superframe, which consists of 360 × L symbols, or 3600 × L bits. ~~Afterwards, these bits~~ The bits of the RS-FEC superframe are then scrambled by the PCS using ~~the PCS~~ an additive scrambler, encoded in PAM4 symbols, and transferred to the PMA.

L is called the interleaving depth, and the possible choices of L are 1, 2, and 4, which shall be determined during the PAM2 training mode InfoField.

After reaching the normal mode of operation, EEE-capable PHYs may enter the LPI transmit mode under the control of the MAC via the XGMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The EEE capability is described in 149.3.2.2.21.

….

149.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B receive state diagram in Figure 149–18 and the PCS Receive bit ordering in Figure 149–7 including compliance with the associated state variables as specified in 149.3.7.2.2.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received PAM4 symbols are demapped and descrambling is performed.

Following descrambling, the L-interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames which cannot be corrected are marked with error symbols by the decoder. ~~The 65B RS-FEC frames are then decoded with Reed-Solomon error correction~~ The RS-FEC decoded frame is then separated into a 10-bit OAM field, separated from the 64B/65B blocks, and fifty 64B/65B blocks. This process generates the 64B/65B block vector rx_coded<64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state dia- gram (see Figure 149–18 and Figure 149–19). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acqui- sition of the descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primi- tive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 consecutive RS-FEC frame errors are detected, the block_lock flag is de-asserted. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication (loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Syn- chronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes 1 bit pattern every 450 PAM2 symbols, which is aligned with the PCS partial PHY frame boundary, as well as an InfoField, which is inserted in the 16th PCS partial PHY frame. When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

PHYs with the EEE capability support transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. Transitions to and from the LPI mode are allowed to occur inde- pendently in the

transmit and receive functions. The PCS receive function is responsible for detecting transi- tions to and from the LPI receive mode and indicating these transitions using signals defined in 149.2.2.

The link partner signals a transition to the LPI mode of operation by transmitting 8 RS-FEC frames com- posed entirely of 64B/65B blocks of /LI/. When blocks of /LI/ are detected at the output of the 64B/65B decoder, rx_lpi_active is asserted by the PCS receive function and the /LI/ character is continuously asserted at the receive XGMII. These frames may be preceded by a frame composed partially of /LI/ characters. After these frames, the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses RS-FEC frame counters to main- tain synchronization with the remote PHY and receives periodic refresh signals that are used to update coef- ficients, so that the integrity of adaptive filters and timing loops in the PMA is maintained. LPI signaling is defined in 149.3.6. The quiet-refresh cycle continues until the link synchronization detect asserts send_s_sigdet to indicate that the alert (link synchronization) sequence has been reliably detected. After the alert sequence, the link partner transmits repeated /I/ characters, representing a wake signal. The PHY receive function sends /I/ to the XGMII for eight RS-Frame periods (wake duration) and then resumes nor-
mal operation.