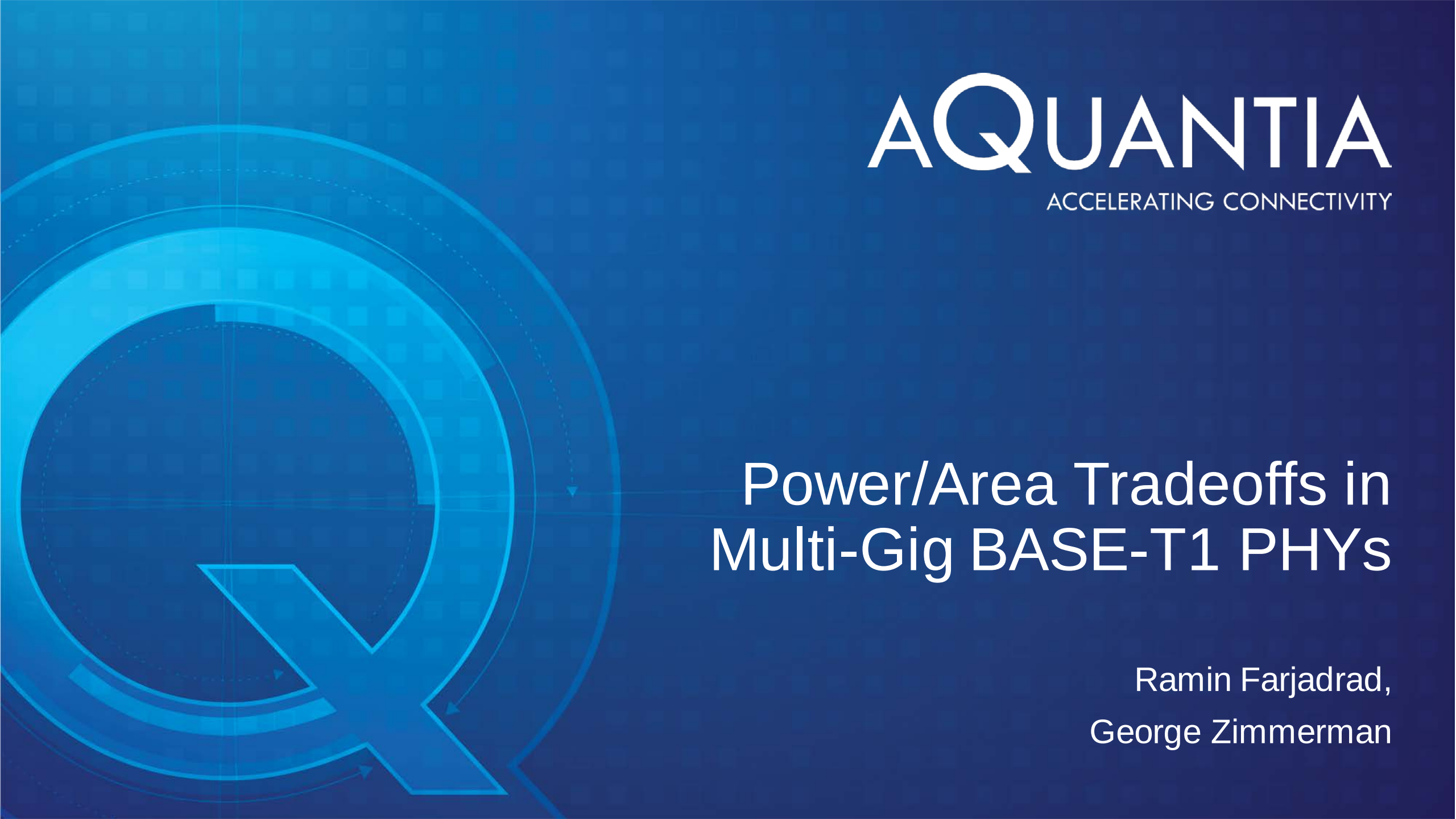


Power/Area Tradeoffs in Multi-Gig BASE-T1 PHYs

Ramin Farjadrad,
George Zimmerman

Decision Factors for Selection of Modulation Schemes

- The top factor in modulation selection is the target performance feasibility
  - Do the selected modulations deliver the target performance (Data rate & BER) over the target medium?

- Among the feasible modulations choices, the next decision factor is to determine the choice with minimum PHY cost. The main PHY cost factors are:
  - Power
  - Area

Salz SNR Margins over 802.3 d0.2.1 Limit Line: 2.5G/5G/10Gbps

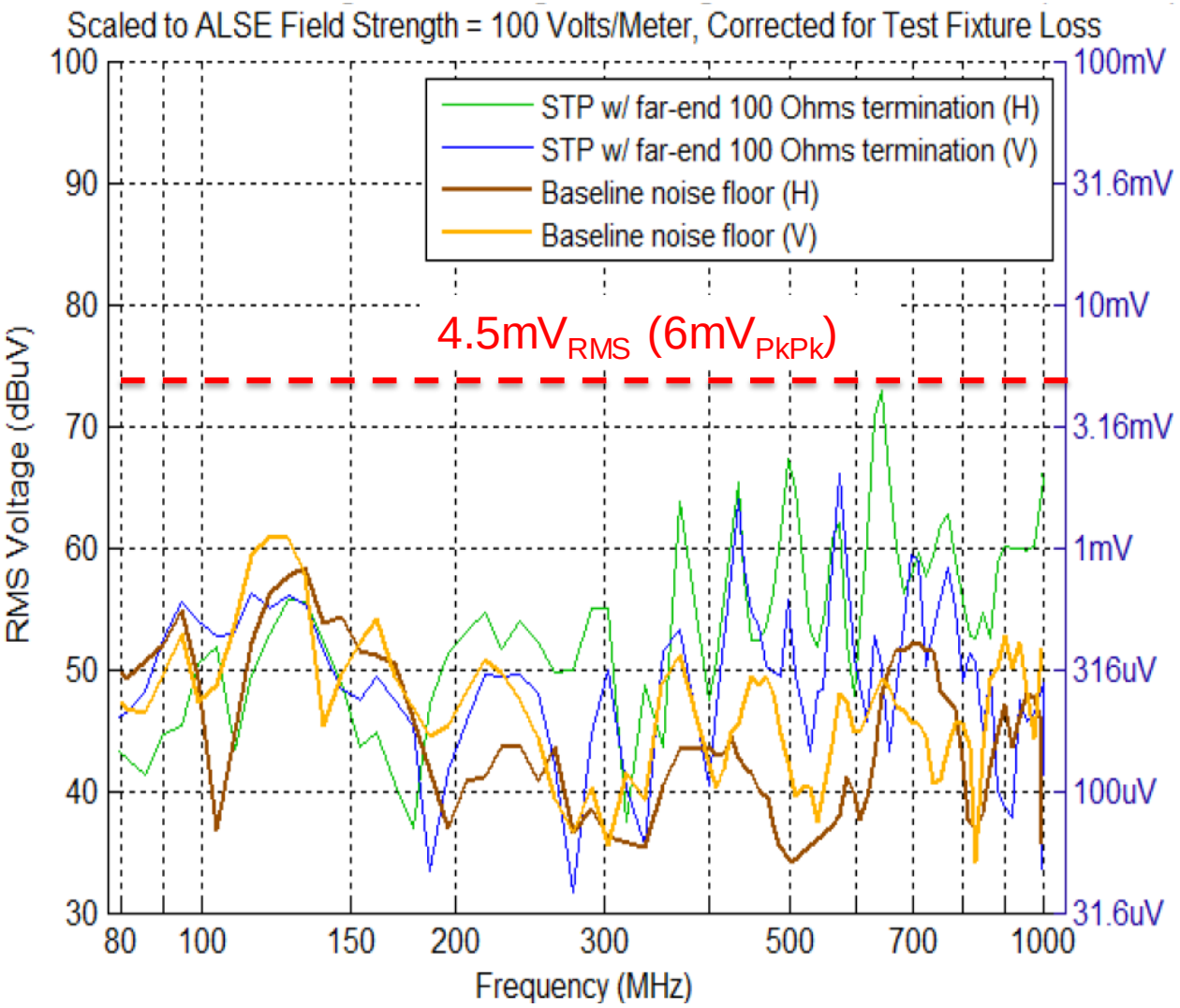
2.5Gbps	PAM2	PAM3	PAM4	PAM8
Baud rate (10% FEC Overhead) [GBaud]	2.75	1.74	1.38	0.92
Nyquist BW (FEC Overhead) [GHz]	1.38	0.91	0.69	0.46
10% Excess BW [GHz]	1.52	1.01	0.76	0.51
IL @Nyquist [dB]	19.00	14.41	12.58	9.96
Ideal PHY Salz SNR margin [dB]	31.49	28.82	26.62	20.46

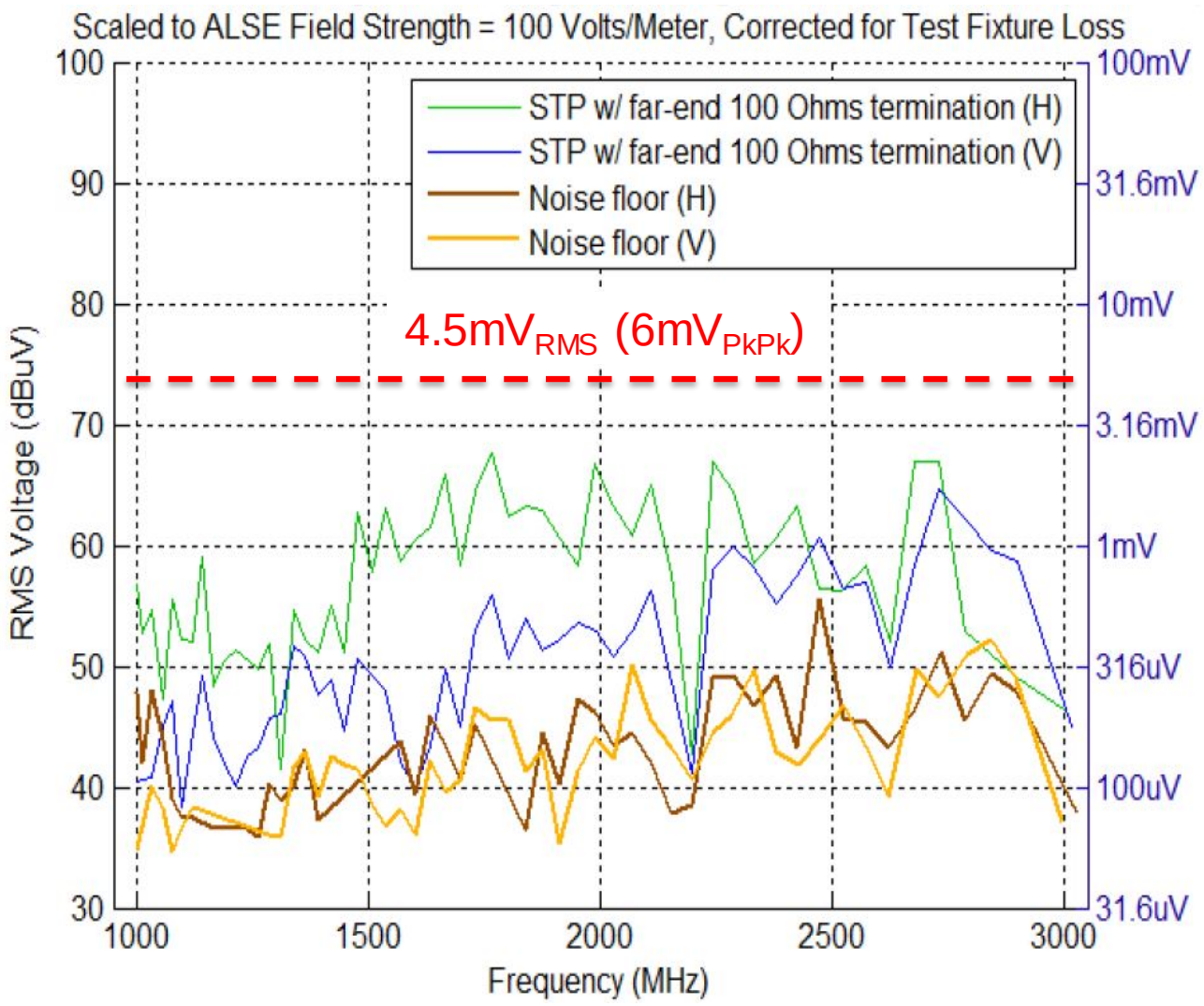
10Gbps	PAM2	PAM3	PAM4	DSQ32	PAM8
Baud rate (10% FEC Overhead) [GBaud]	11.0	7.33	5.50	4.40	3.67
Nyquist BW (FEC Overhead) [GHz]	5.50	3.67	2.75	2.2	1.83
10% Excess BW [GHz]	6.04	4.04	3.02	2.42	2.01
IL @Nyquist [dB]	46.16	35.24	29.23	25.36	22.64
Ideal PHY Salz SNR margin [dB]	14.42	14.68	12.62	10.95	9.97

5.0Gbps	PAM2	PAM3	PAM4	PAM8
Baud rate (10% FEC Overhead) [GBaud]	5.50	3.47	2.75	1.83
Nyquist BW (FEC Overhead) [GHz]	2.75	1.83	1.38	0.92
10% Excess BW [GHz]	3.02	2.01	1.52	1.01
IL @Nyquist [dB]	29.23	22.64	19.00	14.89
Ideal PHY Salz SNR margin [dB]	21.80	21.02	20.23	16.22

- Ideal PHY Salz SNR Assumptions:
  - PHY AFE with AWGN = -150dBm/Hz & Ideal ADC
  - Tx Amplitude= 1.0Vpp (differential)
  - FEC coding gain fully used to cover SNR degradation of
    - Finite DSP Filters Length/Resolutions
    - RF Interferences
- 2.5G/5Gbps ➔ Large SNR margins across all modulations
- 10Gbps ➔ Evaluate Performance vs. Power/Area Tradeoff

RFI Assumption Based on ALSE Measurements on STP/H-MTD

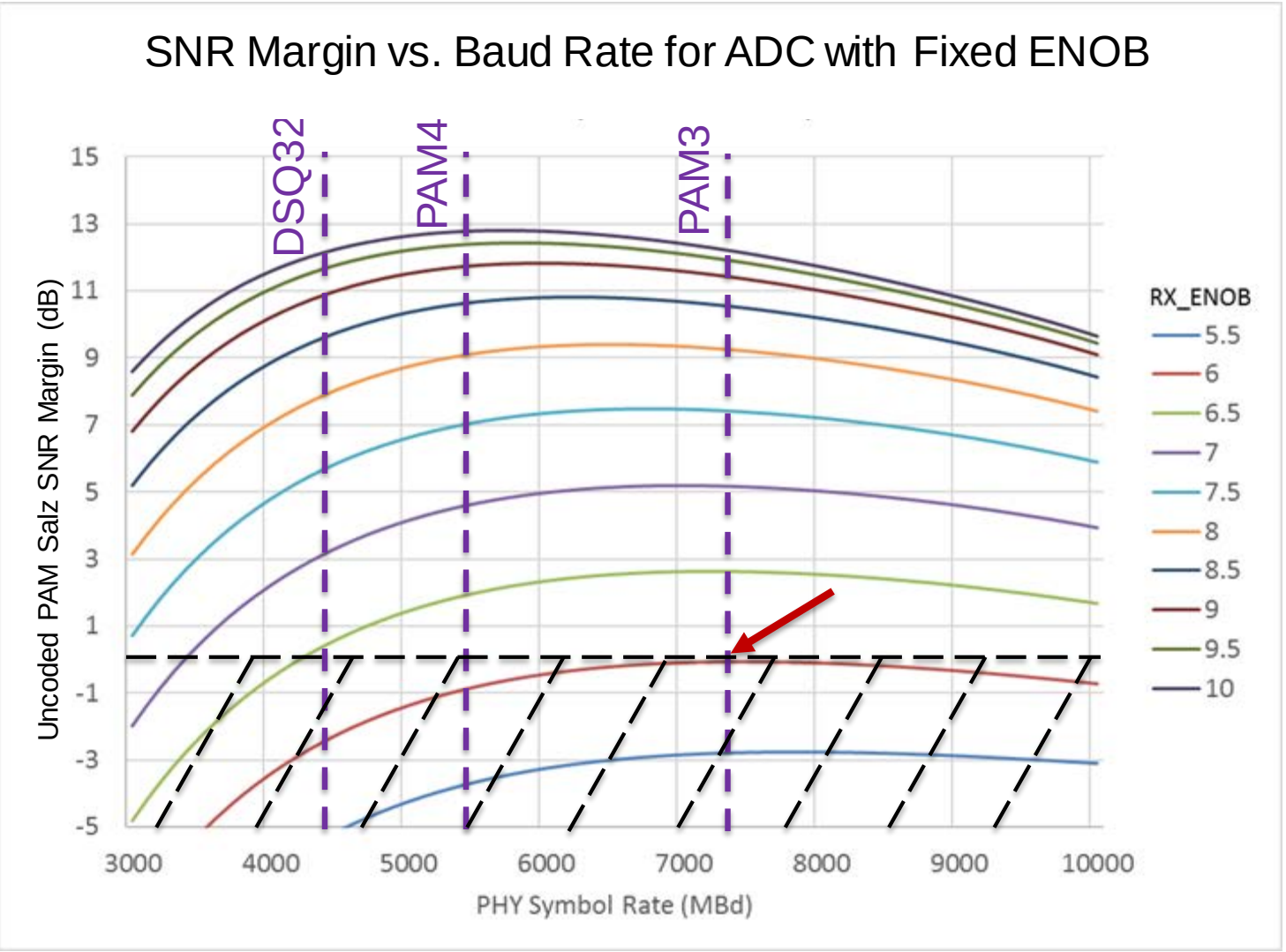




PHY Analog Power/Area Tradeoff versus Modulations/Baud

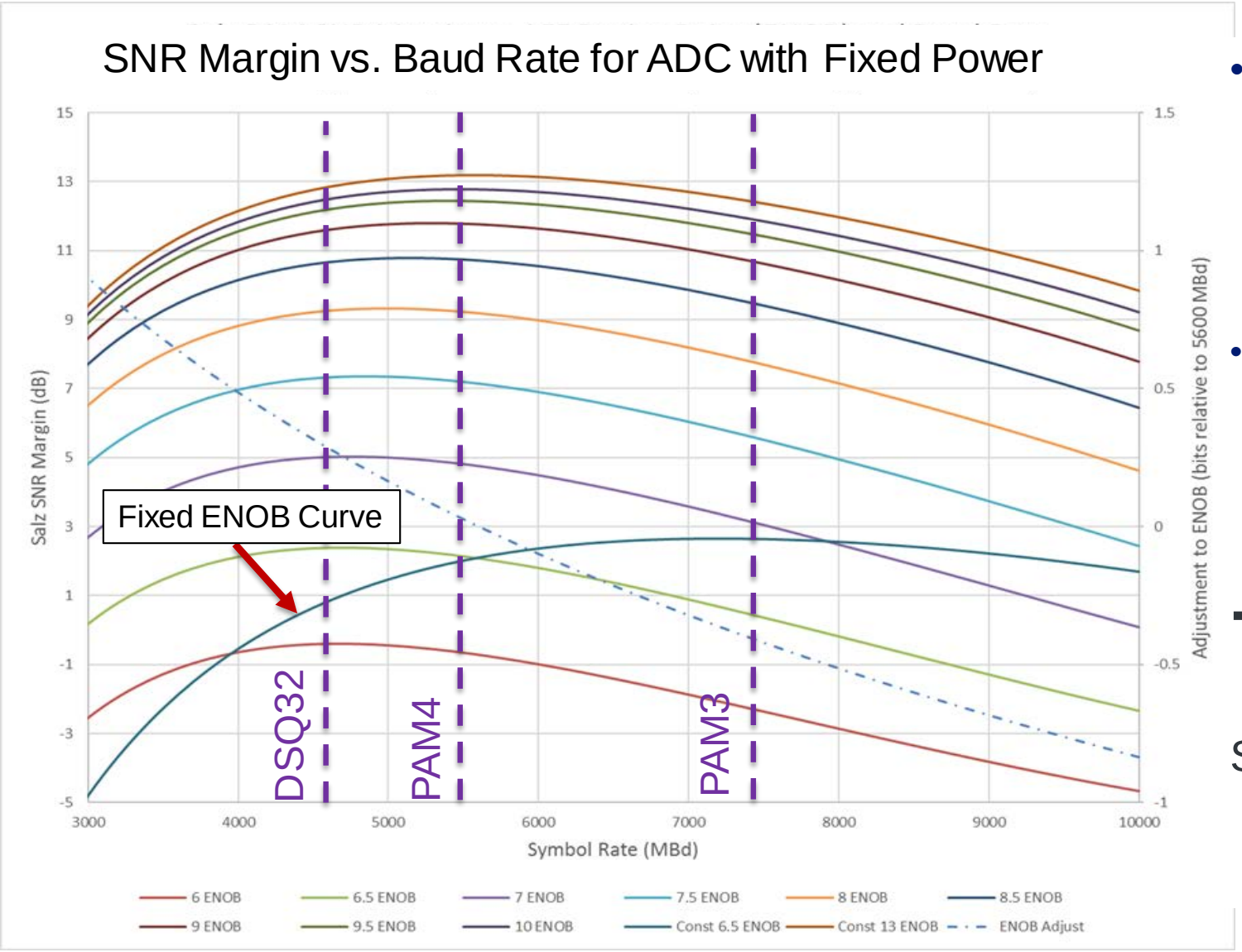
- Analog Front-End (AFE)
  - Analog circuitry introduce device noise generally in form of AWGN
    - At fixed power, AFE AWGN PSD (dBm/Hz) is fixed
      - ➔ Noise power increases with higher Baud/BW
  - Higher Baud (lower PAM) leads to more high-frequency insertion loss
    - ➔ More high-freq noise amplification after high-pass analog equalization
  - ADC power increases with its ENOB (effective number of bits) and Baud
    - ADC Power = K. Baud. 2^{ENOB} → Baud2/Baud1 = $2^{(ENOB1-ENOB2)}$

10Gbps Performance Feasibility



- Simulation assumption:
  - Data rate + Coding overhead=~11Gbps
    - Higher PAM → Lower Baud
  - 15m Cable with 802.3ch d0.1 IL & RL
  - 15dB echo reduction before receive ADC
  - AWGN at receiver input -150dBm/Hz
  - FEC gain fully used by SNR degradation of
    - Finite DSP Filters Length/Resolutions
    - RF Interferences
- Minimum ADC performance to provide positive SNR margin ➔ ~6.1ENOB
  - An ADC with fixed 6.1ENOB leads to PAM3 having highest (non-zero) SNR margin

Effect of ADC Power vs. ENOB on 10Gbps SNR Margin



- ADC with Constant Power

  ENOB2= ENOB1+ $\mathbf{log_2}$(Baud1/Baud2)

  ➔ Higher ENOB with Lower Baud

- PAM3 ADC with 6.1ENOB has same power as:
  - PAM4 ADC with 6.5ENOB (5.5Gbaud)
  - DSQ32 ADC with 6.8ENOB (4.4Gbaud)

➔ Fix ADC power at 6.5ENOB/5.5Gbaud

	DSQ32	PAM4	PAM3
SNR Margin =	2.2dB	2.1dB	0.6dB

PHY Digital Power/Area Tradeoff versus Modulations/Baud

- DSP Cancellation Filters (ISI, Echo, etc)
  - Higher Baud (lower PAM) leads to higher clocking frequency for FIR filters
    - Power per FIR tap increases at least proportional to Baud (clock frequency) → $P=C.V^2.f$
      - Higher clock rate usually needs larger logic gates, leading to large capacitances
  - Higher Baud (lower PAM) leads to more FIR taps over the same channel
    - Higher Baud → Higher signal BW → Higher distortion/interference (ISI/Echo) to cancel
    - Higher Baud → Shorter symbols → Proportionally more taps to cover same channel length

PHY Power/Area Tradeoff versus Modulations/Baud

- Higher PAM leads to higher bits/Sym resolution (e.g. DFE & Echo)
  - Each symbol in PAM3 or PAM4 are represented by 2bits*
  - Each one of two symbols in DSQ32 is represented by 3bits

➔ PHY DSP Estimates: (α & β are constants)

- Power = α x Baud^2 x Bits/Symbol
- Area = β x Baud x Bits/Symbol

- PAM3 vs. PAM4

  Power(PAM3)= 1.78 x Power(PAM4)

  Area(PAM3) = 1.33 x Area(PAM4)

  Power Advantage: PAM4 — Area Advantage: PAM4

- PAM4 vs. DSQ32

  Power(PAM4)= 1.04 x Power(DSQ32)

  Area(PAM4) = 0.8 x Area(DSQ32)

  Power Advantage: None — Area Advantage: PAM4

* PAM3 & PAM4 benefit from implementation simplification by eliminating full multiplicatiers

FIR Implementation Complexity at Different PAM Levels

- FIR implementation can be significantly simplified if multipliers are replaced by simple shift functions.
- PAM2 to PAM5 benefit from this simplification, while PAM6 and beyond do not

✓ PAM2: [+/-1]

✓ PAM3: [0, +/-1]

✓ PAM4: [+/-1, +/-3] $\xrightarrow{+1}$ [0, +/-2, +4] (DC offset of +1 added to FIR input and the output is DC adjusted)

✓ PAM5: [0, +/-1, +/-2]

✗ PAM6: [+/-1, +/-3, +/-5] $\xrightarrow{+1}$ [0, +/-2, +/-4, +6] (All but +6 is not a power of 2)

✗ PAM8: [+/-1, +/-3, +/-5, +/-7] $\xrightarrow{+1}$ [0, +/-2, +/-4, +/-6, +8] (All but +6 is not a power of 2)

- Modulations such as PAM6, PAM8, DSQ32(2xPAM8), Cross32(2xPAM6), PAM16 end up with relatively complex FIR implementations

Conclusion

- Power/Area of the PHY is the second most important factor in selection of proper modulation scheme.
- Factoring in a constant-power AFE in the SNR calculations (with a reasonable ADC ENOB & AFE AWGN) shows DSQ32 & PAM4 offer the best SNR margins
- Factoring in DSP implementation complexity, PAM4 offers better area/power combination than those of DSQ32 and PAM3
- Next step is to evaluate the EMC immunity tolerance of each modulation choice.

Thank you.