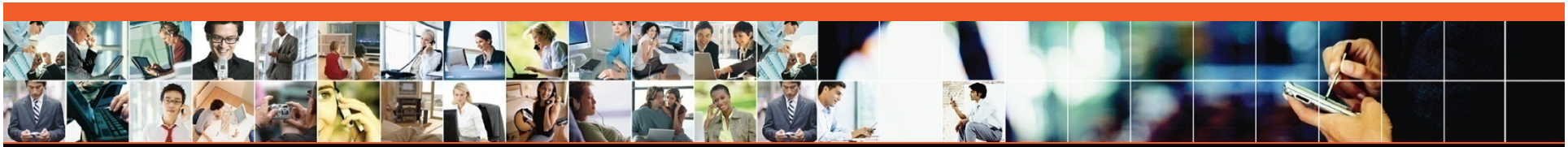

2.5GBASE-T1 PHY Strawman

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Background

- Multi-level PAM options were studied for 2.5, 5 and 10G
  - Large SNR margins for all modulations studied at 2.5G
    - Farjadrad_3ch_01_0518
  - PAM8 is the best choice for 2.5GBASE-T1
    - wu_3ch_01_0518
    - wu_3ch_02_0518
- Start selection of modulation and line rates to meet schedule
  - http://ieee802.org/3/ch/todo/P802_3ch_Timeline_status_0418.xlsm
    - Signaling and modulation target May ‘18
    - Line Coding and FEC target July ’18
    - Draft 1.0 Nov ‘18
- Start with a strawman for 2.5G
  - Study feasibility, cost, time to standard completion
  - Propose and refine further details
  - Contribute to the draft specification

Strawman 2.5GBASE-T1 PHY

- PAM8
  - 2x bits per symbol vs. 1000BASE-T1
- 937.5 Mbaud
  - 25% faster than 1000BASE-T1
  - Modest analog complexity increase vs 1000BASE-T1
- Reed-Solomon(450, 406, 2^9) FEC
  - Shared with 1000BASE-T1
  - 2.5X higher bit rate

PAM8

- PAM8 is the ‘sweet spot’ of PAM-M choices
  - Lower baud rate
    - Near 1000BASE-T1, 1.25X
    - Lower digital power dissipation
  - Higher immunity tolerance
    - 4X vs PAM16
      - **40mV vs 10mV**
  - Simple 3-bit mapping

937.5 MBaud

- Line rate should be compatible with:
  - Low cost components
  - Commonly used clocks: 25 MHz & 156.25 MHz
  - Ethernet infrastructure, lower costs, and simplified design
    - 2.5GBASE-X host side interface – 3.125 Gbaud
      - **125 x 25 MHz**
      - **20 x 156.25 MHz**
- Choose N / M x 25 MHz, N / M x 156.25 MHz
  - Common reference clocks for 1G, 2.5, 5 and 10G PHYs and MAC
  - 937.5 = 75/2 x 25, 6 x 156.25
- PAM8 - 2.5x of 1000BASE-T1 bit rate
  - 3 x 937.5 = 2812.5 Mb/s -> 2.5G + 12.5% overhead

Reed-Solomon(450, 406, 2^9) FEC

- Matched to PAM8 3-bit mapping
  - One RS 9-bit word per three PAM8 symbols
    - vs. 6 PAM3 symbols
  - Preserves the correction power of the 9-bit RS word
    - Aligned to symbol mapping
  - Symbol bit errors do not cross the RS word boundary
- Common with 1000BASE-T1
  - RS encoder/decoder can support both 1G and 2.5G PHY
  - Single IC implementation will support two speeds

Benefits

- Common blocks shared with 1000BASE-T1
  - One PHY can support 1G and 2.5G with minimal relative cost
  - Majority of 1000BASE-T1 can be re-used in 2.5G PHY
- Modest complexity vs. 1000BASE-T1
  - 3-level -> 8-level signaling on transmit and receive paths (DAC, ADC)
    - PAM8 on STP has similar RX analog requirements to 1000BASE-T on UTP
  - 25% increase in clock rate
- Specifications based on 1000BASE-T1
  - Fast track to completed specification
  - Known working state machines for synchronization, training, link monitor, EEE, OAM
    - Minimal modifications needed

Benefits

- Power dissipation
  - PAM4 digital power ~1.75X vs PAM8
  - PAM4 analog power similar to PAM8
    - ADC power increases with baud rate (PAM4 1.5X)
- Relative cost
  - PAM4 digital size ~1.15X vs PAM8
- Cabling
  - Opportunity for lower cost cabling
  - PAM8 bandwidth >470MHz
  - PAM4 bandwidth >700MHz

Next Steps

- PCS
  - Block code encapsulation of XGMII vs GMII
    - http://www.ieee802.org/3/ch/public/sep17/McClellan_3ch_01_0817.pdf
  - Scrambler – leverage 1000BASE-T1
  - OAM – leverage 1000BASE-T1
- PMA
  - Electrical specifications –
    - Transmit power – TX PSD, power level, peak output
    - EMC requirements
  - Start up – highly leverage 1000BASE-T1
    - Synchronization
    - Training pattern – line code, scrambling
    - Boundary alignment
    - State Machines
      - **link training, message exchanges,**
      - **link monitor**
  - EEE - highly leverage 1000BASE-T1