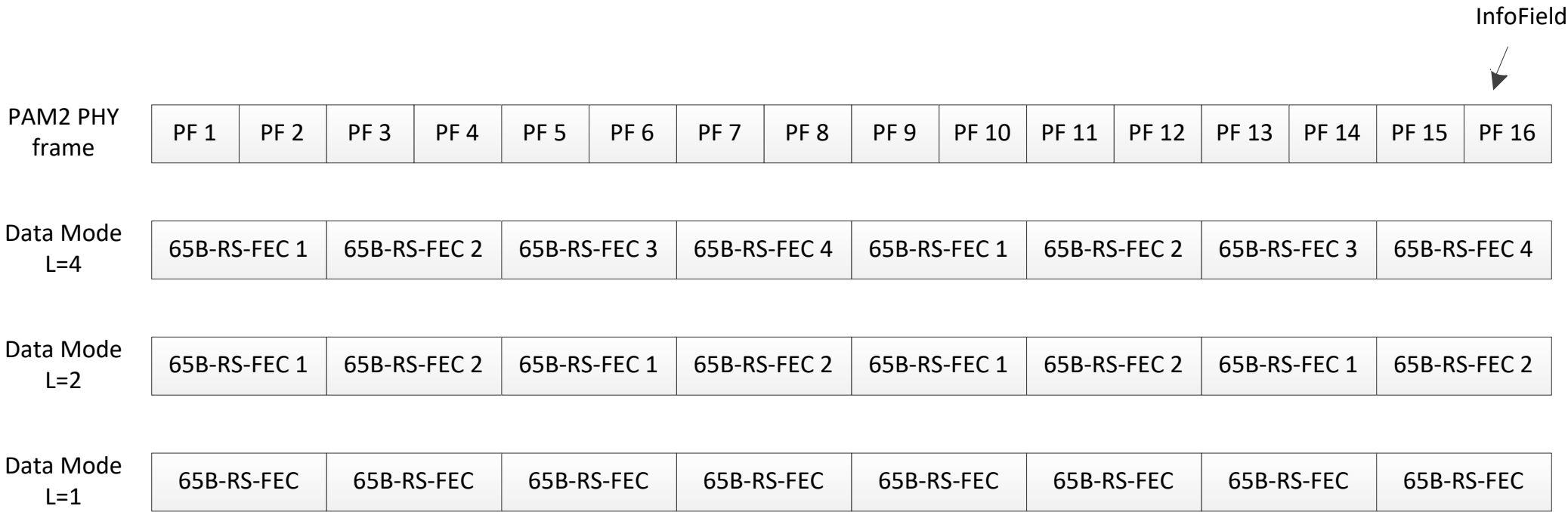# Interleaver Depth
and
Proposed Baseline for PHY Control

Mike Tu
Tom Souvignier

Proposed Baseline

- InfoField Exchange
  - Interleaving depth = 1, 2, or 4
    - Transmitter must support all choices for all speeds
  - Precoder selection = bypass, 1+D, 1-D, 1-D^2
    - Transmitter must support all four selections
  - OAM and EEE enabled only if both sides support it

- PAM2 training PHY frame length = 8 x data mode RS-FEC frame length
  - Partitioned into 16 partial frames
  - Each side maintains a partial frame counter which is embeded in InfoField
  - Switching from PAM2 to PAM4, and enabling precoder are based on announced partial frame counter values

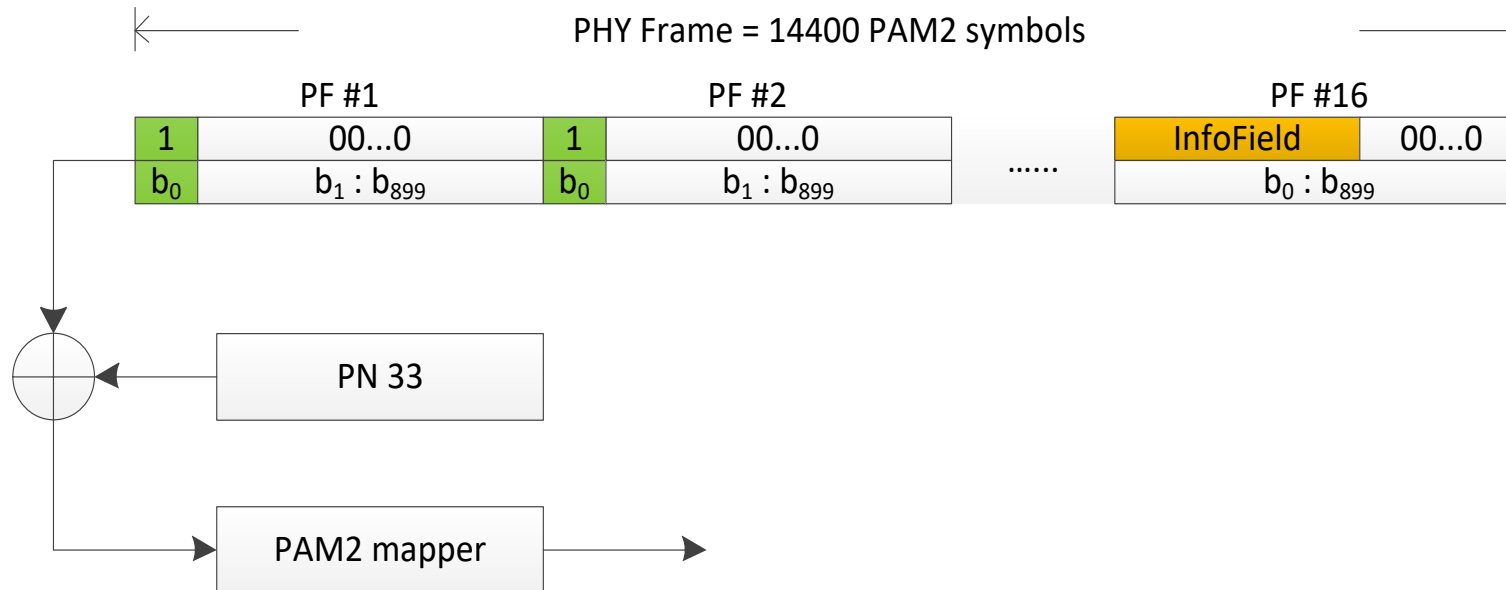- Data mode RS FEC interleaving boundaries aligned with PAM2 training PHY frame boundaries

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Alignment of PAM2 and Data Mode Frames

InfoField

PAM2 PHY frame	PF 1	PF 2	PF 3	PF 4	PF 5	PF 6	PF 7	PF 8	PF 9	PF 10	PF 11	PF 12	PF 13	PF 14	PF 15	PF 16

Data Mode L=4	65B-RS-FEC 1	65B-RS-FEC 2	65B-RS-FEC 3	65B-RS-FEC 4	65B-RS-FEC 1	65B-RS-FEC 2	65B-RS-FEC 3	65B-RS-FEC 4

Data Mode L=2	65B-RS-FEC 1	65B-RS-FEC 2	65B-RS-FEC 1	65B-RS-FEC 2	65B-RS-FEC 1	65B-RS-FEC 2	65B-RS-FEC 1	65B-RS-FEC 2

Data Mode L=1	65B-RS-FEC	65B-RS-FEC	65B-RS-FEC	65B-RS-FEC	65B-RS-FEC	65B-RS-FEC	65B-RS-FEC	65B-RS-FEC

- L=4: 1 superframe ⇔ 4 x 65B-RS-FEC frame

- L=2: 1 superframe ⇔ 2 x 65B-RS-FEC frame

- L=1: 1 superframe ⇔ 1 x 65B-RS-FEC frame

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PAM2 Training PHY Frame Format

- Data mode RS FEC (N=360, K=326, m=10) ➜ 1800 PAM4 symbols

- Training frame consists of 8x1800 = 14400 PAM2 symbols
  - 2.56usec for 10G, 5.12usec for 5G, and 10.24usec for 2.5G

- 16 partial PHY frames
  - Each partial frame = 900 PAM2 symbols
  - First bit of each partial PHY frame is inverted as alignment markers
  - InfoField XOR'ed at the start of the 16th partial frame

InfoField

96-bit Infofield

octet 0	octet 1	octet 2	octet 3/4/5	octet 6	octet 7	octet 8	octet 9	octet 10/11
0xBB	0xA7	0x00	PFC24	Message	MSG24	MSG24	MSG24	CRC16

Table 149-tt1 – InfoField message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 149-tt2 – InfoField message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

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InfoField Formats at Different States

octet 1	octet 2	octet 3	octet 4/5/6	octet 7	octet 8/9/10			octet 11/12
0xBB	0xA7	0x00	PFC24	Message	MSG24	MSG24	MSG24	CRC16

Figure 149-nn1 – InfoField format

octet 1	octet 2	octet 3	octet 4/5/6	octet 7	octet 8/9/10	octet 11/12
0xBB	0xA7	0x00	PFC24	Message	UsrCfgCap	CRC16

Figure 149-nn2 – InfoField TRAINING format

octet 1	octet 2	octet 3	octet 4/5/6	octet 7	octet 8/9/10	octet 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 149-nn3 – InfoField COUNTDOWN format

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Capability Bits

- EEE enabled only if both PHYs set EEEen = 1.

- OAM enabled only if both PHYs set OAMen = 1.

- InterleaveDepth
  - Oct10<2:1> = 00 ⟺ L=1
  - Oct10<2:1> = 01 ⟺ L=2
  - Oct10<2:1> = 10 ⟺ L=4
  - Oct10<2:1> = 11 ⟺ reserved
  - Tx must support the requested interleaving depth

- PrecodeSel
  - Oct10<4:3> = 00 ⟺ precoder bypass, or no precoder
  - Oct10<4:3> = 01 ⟺ 1-D
  - Oct10<4:3> = 10 ⟺ 1+D
  - Oct10<4:3> = 11 ⟺ $1-D^2$
  - Tx must support the selected precoder

- Seed
  - For deg=58 data mode scrambler, these 15 bits shall be part of the initial state. Fill out the other bits with pre-defined known values.
  - If PN33 training mode scrambler is used for data mode as well, then these 15 bits can be changed to Reserved.

octet 8								octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Seed (or Reserved)															EEEen	OAMen	InterleaveDepth		PrecodeSel		Reserved	Reserved	Reserved

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PHY Control state diagram

- Start with MS PAM2 half duplex
- SL PAM2 starts after en_slave_tx=1
- MS and SL check for loc_rcvr and rem_rcvr status OK
- Exchange EEE, OAM capabilities, precoder selection, and interleaving depth
- Exchange exact time for each PHY to switch into PCS Test
- Local count down and enter TX SWITCH state
  - Send PAM4
  - Precoder enabled
  - FEC encoder enabled
  - Interleaver enabled
- Remote count down and switch to PCS Test
- 10G RS layer responsible for data flow control after link up

Figure 149-16 – PHY Control state diagram

PHY Control state diagram (cont.)

- Note: "rem_countdown_done" is based on implicit counter values, instead of checking last InfoField.

- "PCS_status" is the same as defined in Clause 55.3.6.1.

- Similar to 10GBASE-T, the two sides rely on Clause 46 Reconciliation Sublayer "link fault detection" to determine if the remote receiver is ready to receive data.
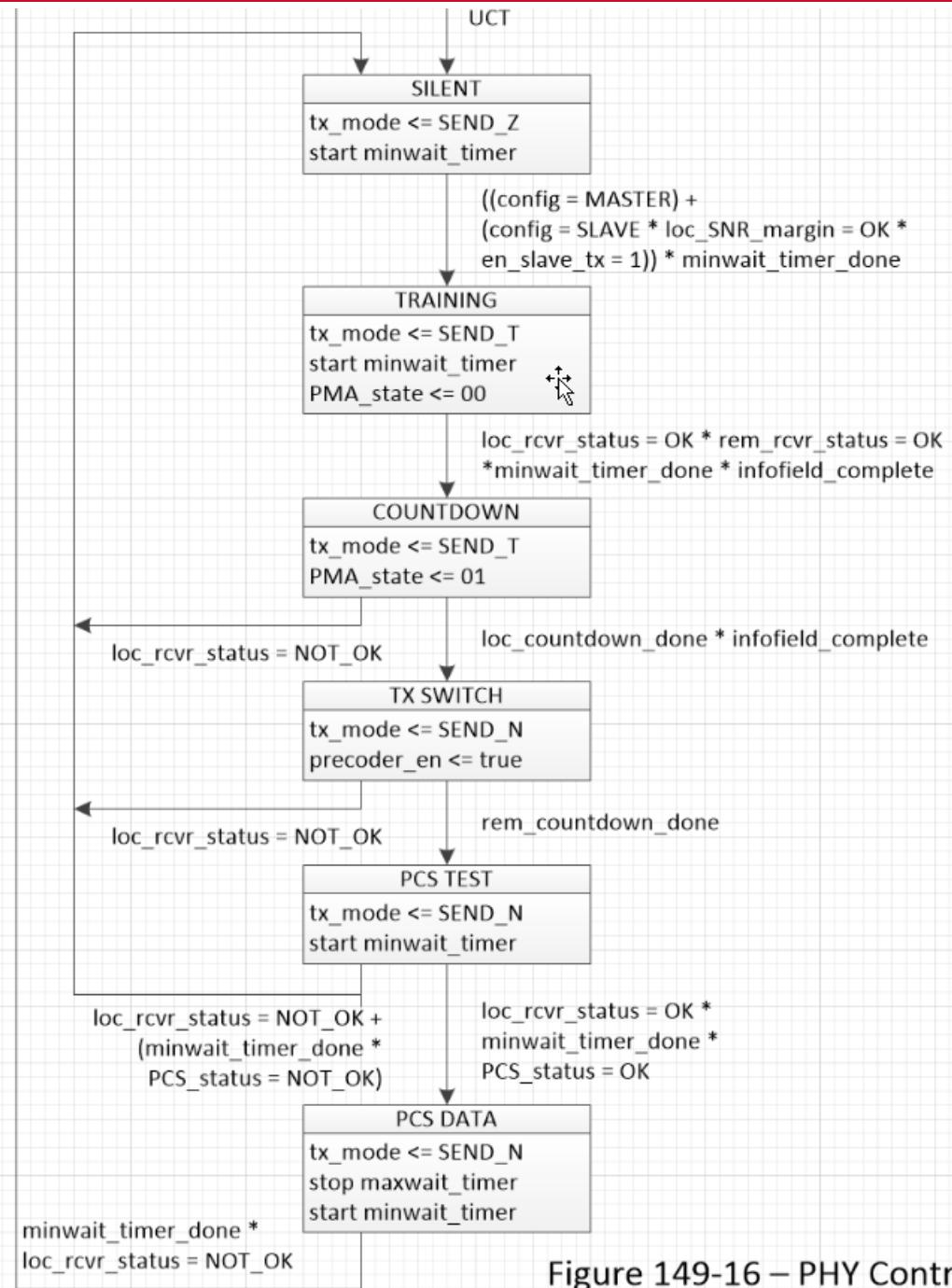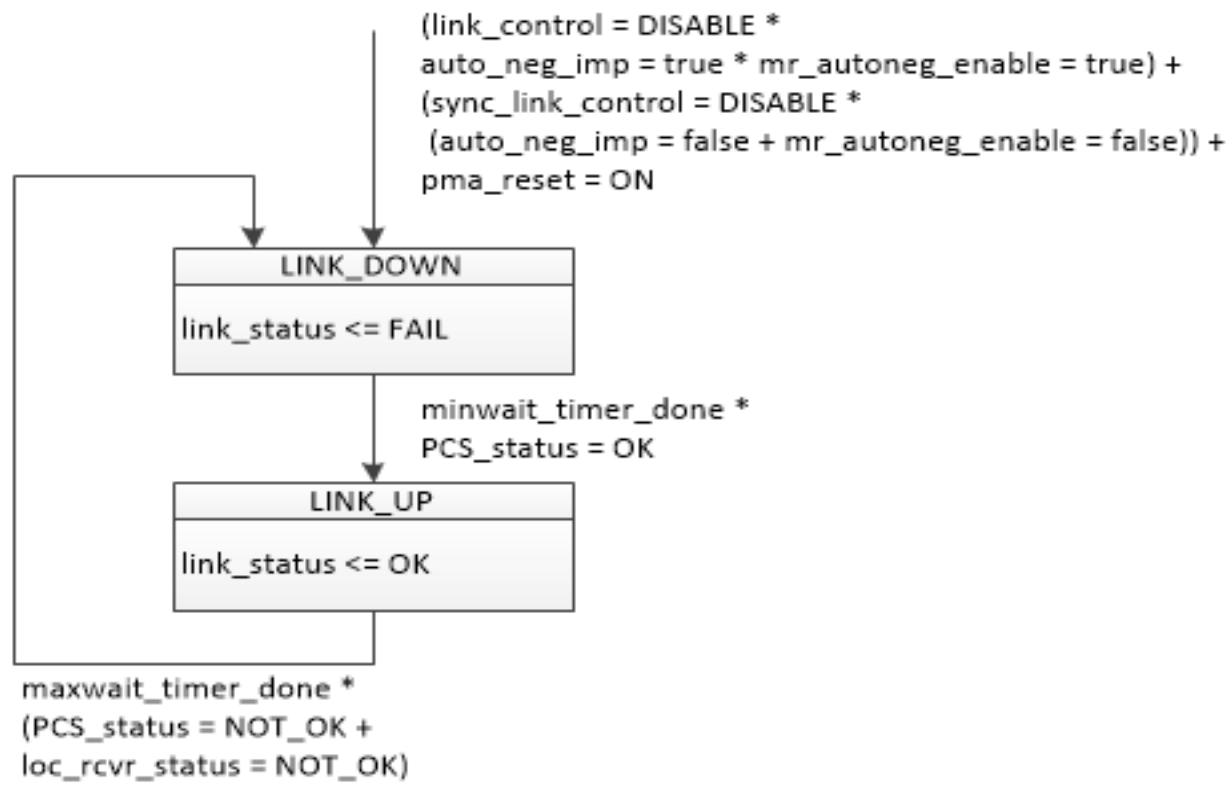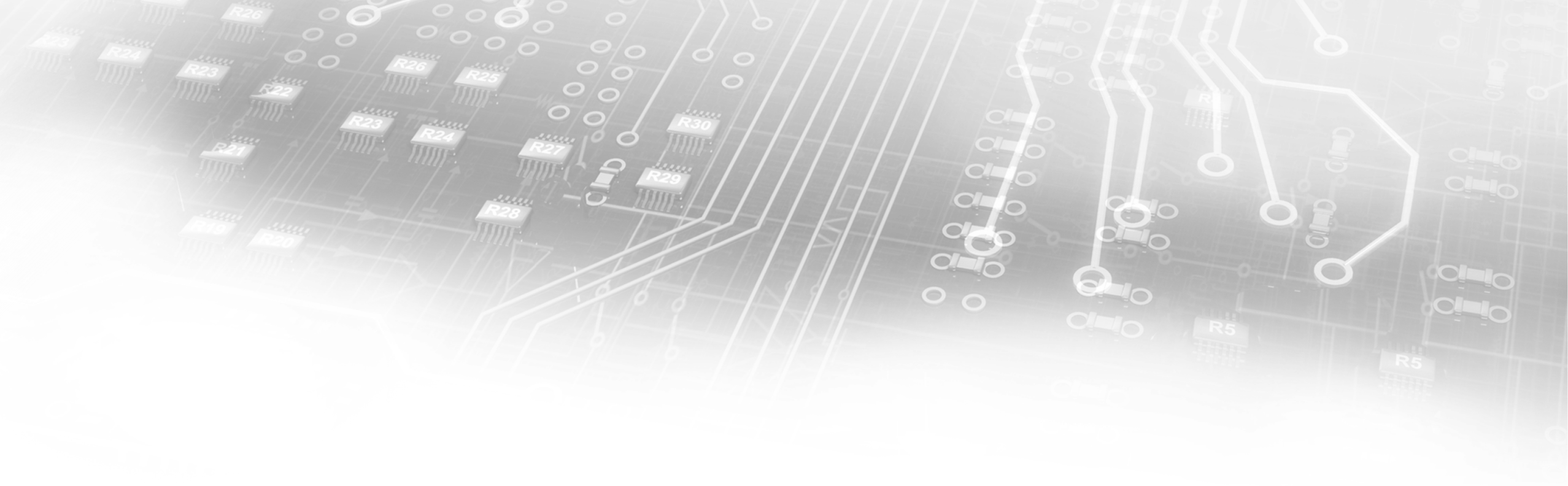

Figure 149-16 – PHY Control state diagram

Link Monitor state diagram

(link_control = DISABLE *
auto_neg_imp = true * mr_autoneg_enable = true) +
(sync_link_control = DISABLE *
 (auto_neg_imp = false + mr_autoneg_enable = false)) +
pma_reset = ON

LINK_DOWN

link_status <= FAIL

minwait_timer_done *
PCS_status = OK

LINK_UP

link_status <= OK

maxwait_timer_done *
(PCS_status = NOT_OK +
loc_rcvr_status = NOT_OK)

NOTE 1 – maxwait_timer is started in PHY Control state diagram (see Figure 149-16).
NOTE 2 – The variables link_control and link_status are designated as link_control_mGigT1
and link_status_mGigT1, respectively, by the Auto-Negotiation Arbitration state diagram
(Figure 98-7) if the optional Auto-Negotiation function is implemented.

Figure 149-17 – Link Monitor state diagram

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THANK YOU

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IEEE 802.3ch Task Force – November 2018