Timing in PHY startup (D2.1 Comment #169)

Rev b (first presented in 9/4/19 ad hoc)

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Comment 169

Cl **149** *SC* **149.4.2.4.10** *P* **147** *L* **35** # 169

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Comment Type **T** *Comment Status* **X** *late*

To ensure interoperability during the training phase, certain timing allocations between Master, Slave and other steps of training must be observed. We propose to the text of 802.3bz for interoperability and just scale the timing of 10G mode and deduct the timing for PCS_TEST that is set by min_wait_timer.

SuggestedRemedy

tModify FIgure 149_33 as attached and Include the associated Table 145.15 in section 149.4.2.4.10 page 147, line 35 to read as follows

MASTER	SLAVE	MAX REQUIRED TIME
Traning	Silent	40.00 msec
Training	Training	57.02 msec
PCS Test	PCS Test	0.98 msec
TOTAL		98.00 msec

Proposed Response *Response Status* **O**

Timing the startup

- PHY control must complete in no more than 97 msec or risk being terminated by the link_fail_inhibit_timer
  - 97 msec, Max = 98 msec (see 98.5.2)
- No timers control times in:
  - SILENT
  - TRAINING
  - COUNTDOWN/TX_SWITCH
- Experience from 10GBASE-T showed different designers made different assumptions of the time distribution
  - Discovered after initial publication, so it was a recommendation, not a requirement

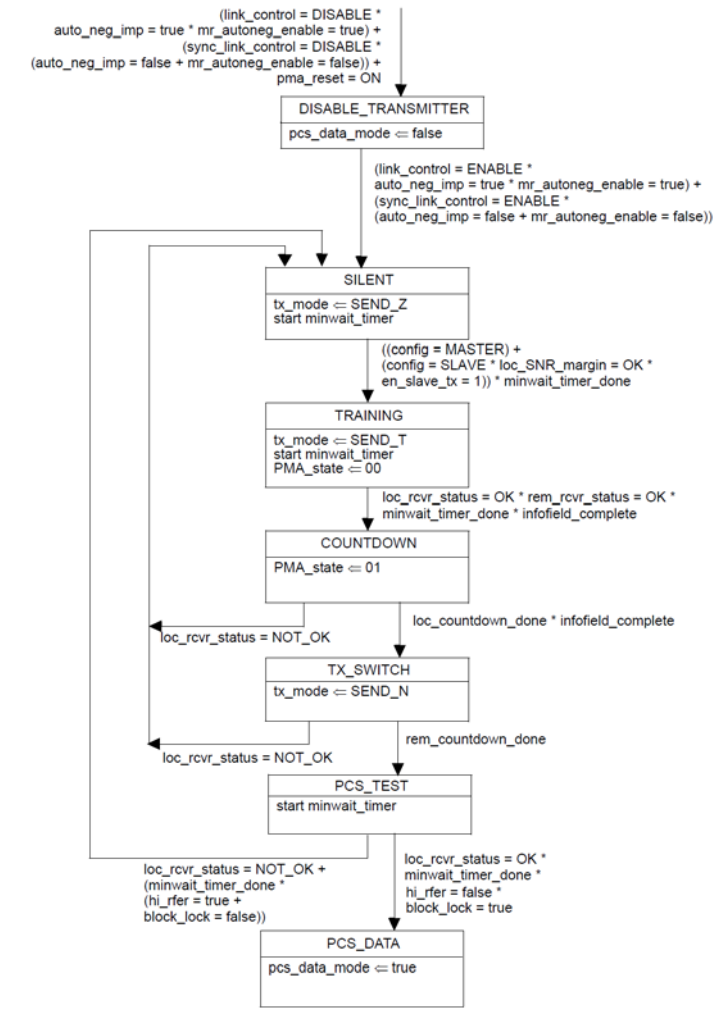

Figure 149–33—PHY Control state diagram

Approaches to the problem

- Modify state diagram: Add timers to push on to the next state
  - This makes us define the behavior in the over-time case which isn't supposed to happen: EXTRA WORK & UNINTENDED CONSEQUENCES!
- Add a statement "a compliant phy shall spend no more than *X* msec in state *Y*" into state diagram text
  - Such statements get lost and are unusual in 802.3 style
- Add a table for timing, similar to 2.5G/5G/10GBASE-T, but REQUIRED.

Suggested response

Insert new final paragraph to 149.4.2.4.10 Startup sequence (Page 147 line 35): ”The startup timing shall comply with Table 145-15 for MASTER, and Table 145-16 for SLAVE.”

Insert new tables 145-15 and 145-16 at end of 149.4.2.4.10:

Table 145-15: Startup timing maximums for MASTER

Timing Interval	Maximum time (msec)
From entry to SILENT state until en_slave_tx = 1 is transmitted	40 – 0.384/S
From entry of SILENT state until entry to COUNTDOWN state	95.975 – 0.384/S
Entry to COUNTDOWN until entry of TX_SWITCH	0.384 / S
Entry to exit of PCS TEST	1.025
Total (Entry to SILENT to exit of PCS TEST)	97 msec

Table 145-16: Startup timing maximums for SLAVE

Timing	Maximum time (msec)
Entry to exit of SILENT state	40
Entry of SILENT state to exit of TRAINING state	95.975 – 0.384/S
Entry to COUNTDOWN until entry of TX_SWITCH	0.384 / S
Entry to exit of PCS TEST	1.025
Total (Entry to SILENT to exit of PCS TEST)	97 msec

THANK YOU!

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