Baseline proposals for copper twinaxial cable specifications

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Purpose

- Baseline proposals for 802.3ck copper twinaxial cable specifications consistent with adopted objectives
  - Tx/Rx receiver PCB insertion loss specifications
  - Test fixtures PCB insertion loss specifications
  - Host channel insertion loss specifications
  - Channel insertion loss specifications
  - Cable assembly specifications
  - Test fixture specifications
  - MDI specifications

Supporters

- Greg McSorley, Samuel Kocsis - Amphenol
- Nathan Tracy – TE Connectivity

802.3ck Objectives

OBJECTIVES (1 OF 2)

- Support a MAC data rate of 100 Gb/s, 200 Gb/s and 400 Gb/s
- Support full-duplex operation only
- Preserve the Ethernet frame format utilizing the Ethernet MAC
- Preserve minimum and maximum FrameSize of current IEEE 802.3 standard
- Support the existing bit error ratios (BERs) at the MAC/PLS service interface (or the frame loss ratio equivalent) for 100 Gb/s, 200 Gb/s and 400 Gb/s Ethernet

- Define a single-lane 100 Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 100 Gb/s per lane optical signaling
- Define a single-lane 100 Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications
- Define a single-lane 100 Gb/s PHY for operation over electrical backplanes supporting an insertion loss ≤ 28 dB at 26.56 GHz.
- Define a single-lane 100 Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 2 m.

Source: http://www.ieee802.org/3/ck/P802_3ck_Objectives_2018mar.pdf

802.3ck Objectives

OBJECTIVES (2 OF 2)

- Define a two-lane 200 Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 100 Gb/s per lane optical signaling.
- Define a two-lane 200 Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications.
- Define a two-lane 200 Gb/s PHY for operation over electrical backplanes supporting an insertion loss ≤ 28 dB at 26.56 GHz.
- Define a two-lane 200 Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 2 m.

- Define a four-lane 400 Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 100 Gb/s per lane optical signaling.
- Define a four-lane 400 Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications.
- Define a four-lane 400 Gb/s PHY for operation over electrical backplanes supporting an insertion loss ≤ 28 dB at 26.56 GHz.
- Define a four-lane 400 Gb/s PHY for operation over twin-axial copper cables with lengths up to[3] at least 2 m.

Source: http://www.ieee802.org/3/ck/P802_3ck_Objectives_2018mar.pdf

Use 136 as template

- 136.8.1 Figure 136-2
- 136.10 Channel characteristics
- 136.11 Cable assembly characteristics
- 136.12 MDI specifications
- Annex 136A (informative)
  - TP0 and TP5 test point parameters and channel characteristics for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4
- Annex 136B (normative)
  - Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M
- Annex 136C (normative)
  - MDIs for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4
- Annex 136D (informative)
  - Host and cable assembly form factors for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

Type 100GBASE-CR, 200GBASE-CR2, 400GBASE-CR4 - baseline

- xxx.8.1 Figure xxx-2
- xxx.10 Channel characteristics
- xxx.11 Cable assembly characteristics
- xxx.12 MDI specifications
- Annex xxxA (informative)
  - TP0 and TP5 test point parameters and channel characteristics for 100GBASE-CR, 200GBASE-CR2, and 400GBASE-CR4
- Annex xxxB (normative)
  - Test fixtures for 100GBASE-CR, 200GBASE-CR2, 400GBASE-CR4, 100GAUI-1 C2M, and 200GAUI-2 C2M
- Annex xxxC (normative)
  - MDIs for 100GBASE-CR, 200GBASE-CR2, and 400GBASE-CR4
- Annex xxxD (informative)
  - Host and cable assembly form factors for 100GBASE-CR,

NOTE: The assumptions used to generate the values in the baseline need to be validated and therefore recognized by the inclusion of TBDs.

Type 100GBASE-CR, 200GBASE-CR2, 400GBASE-CR4 - baseline

136.8.1 Link block diagram

One direction of a 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4 link is shown in Figure 136–2.

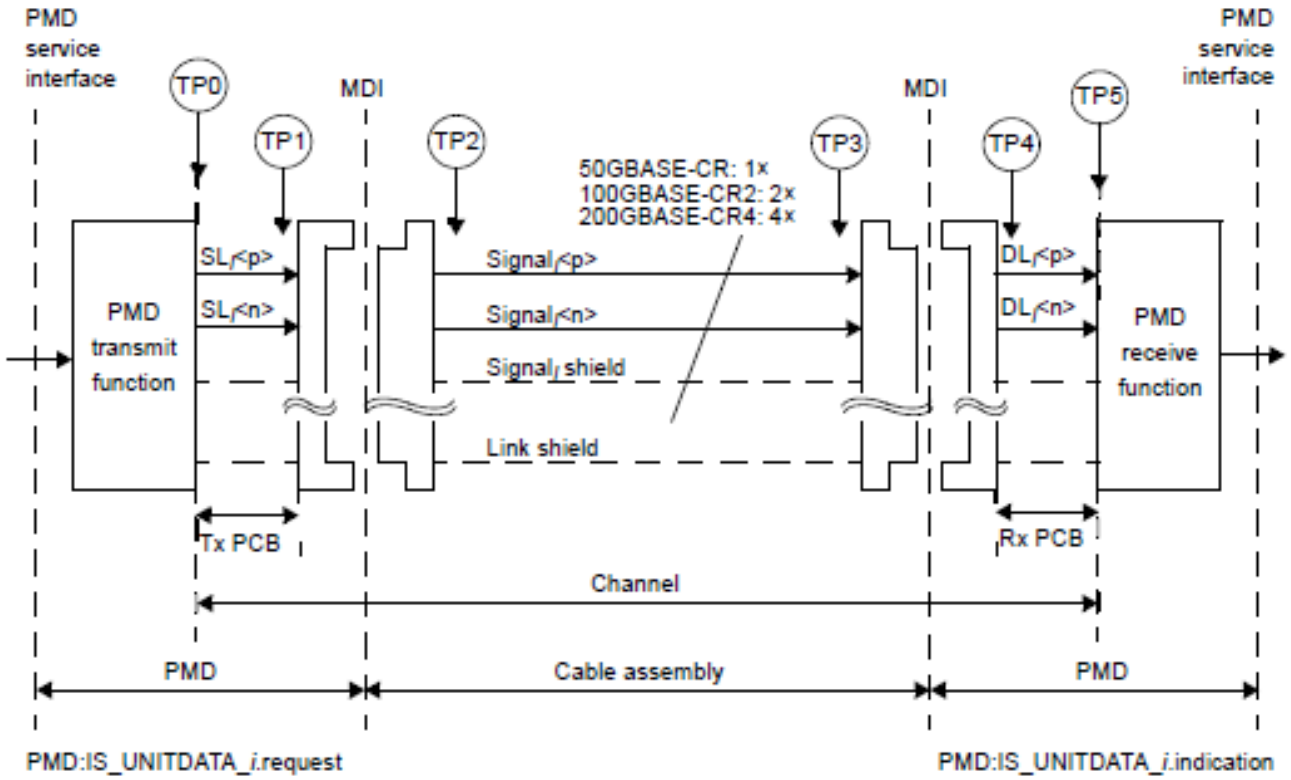


Figure 136–2—50GBASE-CR, 100GBASE-CR2 or 200GBASE-CR4 link (one direction is illustrated)

Adopt Figure 136-2 – revised to 100GBASE

802.3bj/by/cd - Tx/Rx receiver PCB IL

- The recommended maximum and minimum printed circuit board trace insertion losses are specified in
- Equation (92A–1) and Equation (92A–2), respectively. Specified in 92A.4 EQ(92A-1 (max) and 92A-2 (min))– referenced 110A.4

$$IL_{PCB}(f) \le IL_{PCBmax}(f) = 0.5(0.0694 + 0.4248\sqrt{f} + 0.9322f) \quad \text{(dB)} \qquad (9$$

for 0.01 GHz $\le f \le$ 19 GHz.

where

f	is the frequency in GHz
$IL_{PCB}(f)$	is the insertion loss for the transmitter and receiver PCB
$IL_{PCBmax}(f)$	is the recommended maximum insertion loss for the transmitter and receiver PCB

$$IL_{PCB}(f) \ge IL_{PCBmin}(f) = 0.086(0.0694 + 0.4248\sqrt{f} + 0.9322f) \quad \text{(dB)}$$

for 0.01 GHz $\le f \le$ 19 GHz.

where

f	is the frequency in GHz
$IL_{PCB}(f)$	is the insertion loss for the transmitter and receiver PCB
$IL_{PCBmin}(f)$	is the minimum insertion loss for the transmitter and receiver PCB

Host Tx and Rx PCB losses

- Transmitter and receiver differential printed circuit board trace loss

GHz	dB/in
1	0.1856
6.5	0.8971
7	0.9557
12.89	1.5924
14	1.702

Attenuation* (dB/in) at:	1 GHz	6.5 GHz	7 GHz	12.89 GHz	14 GHz
Meg6_LowSR – Wide	0.0951	0.4159	0.4433	0.7562	0.8127
Meg6_LowSR – Narrow	0.1466	0.5849	0.6205	1.0152	1.0847
Meg6_HighSR – Wide	0.1175	0.5960	0.6367	1.0891	1.1688
Meg6_HighSR – Narrow	0.1856	0.8971	0.9557	1.5924	1.7020
ImpFR4_LowSR – Wide	0.1202	0.6096	0.6541	1.1772	1.2734
ImpFR4_LowSR – Narrow	0.1717	0.7794	0.8323	1.4410	1.5512
ImpFR4_HighSR – Wide	0.1427	0.7904	0.8484	1.5158	1.6367
ImpFR4_HighSR – Narrow	0.2106	1.0930	1.1692	2.0283	2.1813

*using Algebraic Model v2.02a – see backup slides for values entered in Model

PROPOSED PARAMETERS; GRAPHS ON PREVIOUS SLIDE

Proposal for Defining Material Loss 26-Jan 12	Elizabeth Kochuparambil Joel Goergen	Cisco

http://www.ieee802.org/3/bj/public/jan12/kochuparambil_01a_0112.pdf

12

802.3bj Cu specifications

Transmitter and receiver differential PCB IL

- IL @ 26.56 GHz

$$IL_{PCB}(f) \le IL_{PCBmax}(f) = 0.5(0.0694 + 0.4248\sqrt{f} + 0.9322f) \quad \text{(dB)}$$

for $0.01\ \text{GHz} \le f \le 19\ \text{GHz}$.

where

f is the frequency in GHz
$IL_{PCB}(f)$ is the insertion loss for the transmitter and receiver PCB
$IL_{PCBmax}(f)$ is the recommended maximum insertion loss for the transmitter and receiver PCB

IL @ 12.89 GHz = 6.81 dB
IL @ 13.28 GHz = 7.00 dB
IL @ 26.56 GHz = 13.51 dB

PCB IL @ 12.89 GHz 1.5924 dB/in

GHz	ILpcb(max)	ILpcb(min)	inches (Max)	inches (Min)
12.89	6.81	1.17	4.27	0.74

$$IL_{PCB}(f) \ge IL_{PCBmin}(f) = 0.086(0.0694 + 0.4248\sqrt{f} + 0.9322f) \quad \text{(dB)}$$

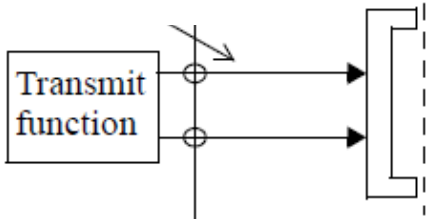
for $0.01\ \text{GHz} \le f \le 19\ \text{GHz}$.

where

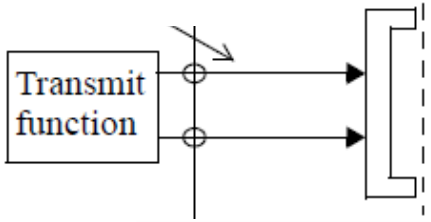
f is the frequency in GHz
$IL_{PCB}(f)$ is the insertion loss for the transmitter and receiver PCB
$IL_{PCBmin}(f)$ is the minimum insertion loss for the transmitter and receiver PCB

IL @ 12.89 GHz = 1.17 dB
IL @ 13.28 GHz = 1.20 dB
IL @ 26.56 GHz = 2.32 dB

IL @ 12.89 GHz = Max 6.81 dB
= Min 1.17 dB



IL @ 13.28 GHz = Max 7.00 dB
= Min 1.20 dB



Transmitter and receiver differential PCB IL

Why 7.5dB is Required for Host PCB Budget ?

- With Meg-7N material, 4.5mil trace IL at HT is measured to be 1.24 dB/in at 28 GHz

- For each front port channel there will be 2 set of vias (at host ASIC BGA footprint & at I/O connector footprint) with stripline routing
  - Footprint via with 7.9mil drill & 130mil thick stackup is simulated to be 0.68 dB at 28 GHz

- Total host PCB budget = (5 x 1.24 + 2 x 0.68) = **7.56 dB**

Source: http://www.ieee802.org/3/ck/public/18_05/lim_3ck_01a_0518.pdf

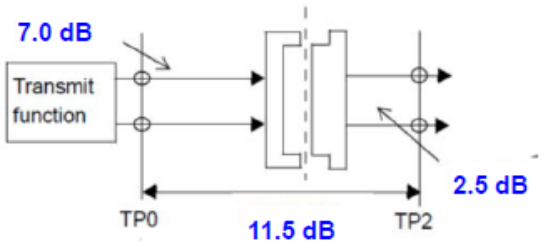


Figure 2: 100GEL CR **TP0-TP2** insertion loss budget at 26.56 GHz

Figure source: http://www.ieee802.org/3/ck/public/18_07/lim_3ck_01b_0718.pdf

ILpcb(max)=(4.55 in*1.24 dB/in)+(2*0.68)dB = 7.00 dB

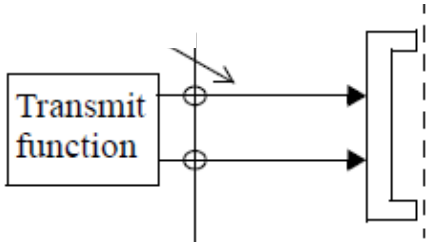
Transmitter and receiver differential PCB IL - baseline

ILpcb(max)=(4.55 in*1.24 dB/in)+(2*0.68)dB = 7.00 dB

ILpcb(max)=0.26*(0.0694+0.4248*SQRT(25.56)+0.9322*25.56) = 7 dB

For 0.01 GHz ≤ f ≤ 38 GHz

IL @ 26.56 GHz = Max 7.00 dB

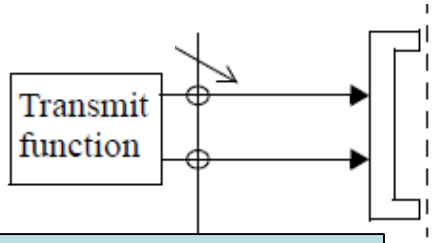


ILpcb(min)=(0.76 in*1.24 dB/in)+(2*0.68) dB = ~ 2.3 dB

ILpcb(min)=0.0852*(0.0694+0.4248*SQRT(25.56)+0.9322*25.56) = 2.3 dB

For 0.01 GHz ≤ f ≤ 38 GHz

IL @ 26.56 GHz = Min 2.3 dB



Adopt Tx/Rx – PCB IL with TBD

Host Channel – Baseline

- Use transmitter and receiver differential printed circuit board trace loss max (with IL @ 26.56 GHz) slide 7.
- Note: The connector insertion loss is 1.5 dB for the mated test fixture. The host connector is allocated 0.5 dB for implementation allowance.

IL host connector @ 26.56 GHz = 11.5-7-2.5 = 2 dB

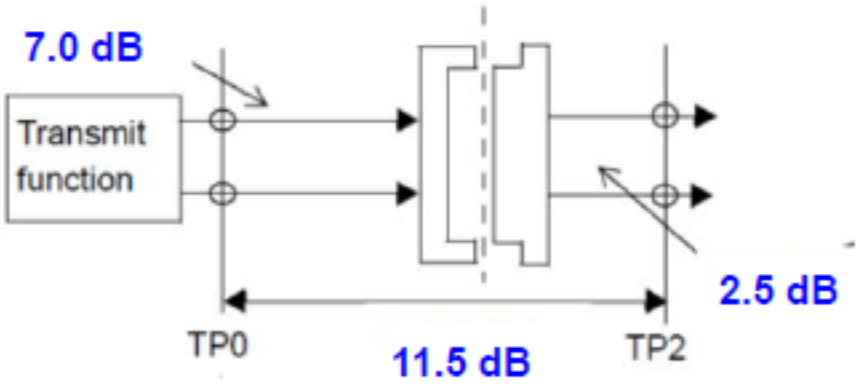


Figure 2: 100GEL CR **TP0-TP2** insertion loss budget at 26.56 GHz

Figure source: http://www.ieee802.org/3/ck/public/18_07/lim_3ck_01b_0718.pdf

Adopt Host Channel IL @ 26.56 GHz with TBD

Bulk Cable Assumed @ 26.56 GHz

- Bulk cable assumed =15.4-(2*1.2)-(2*1.5) = 10 dB

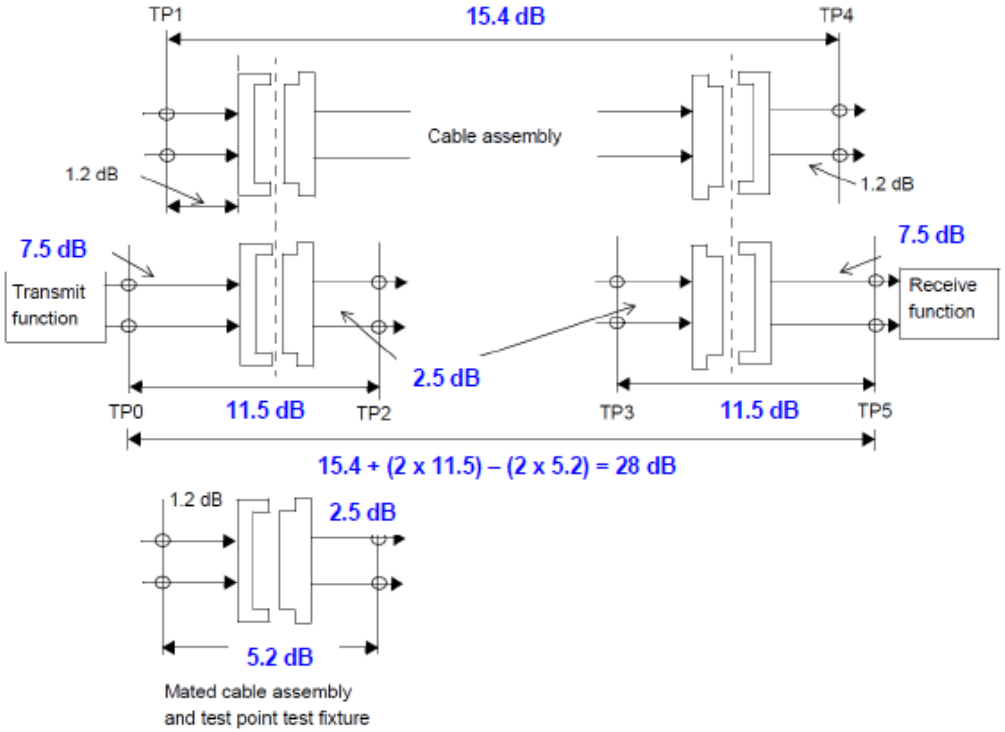
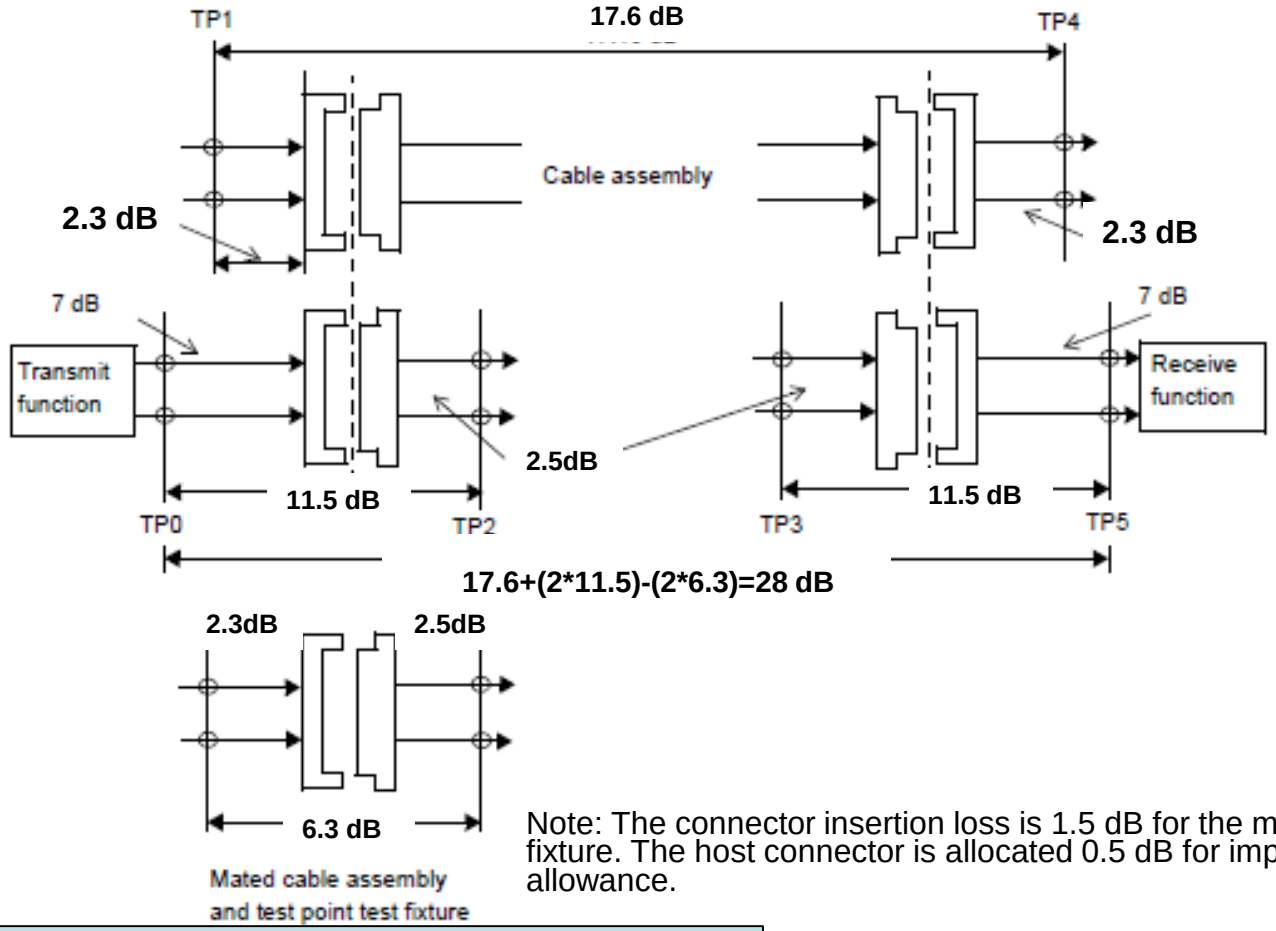


Figure 2: 100GEL CR **28dB** insertion loss budget at 26.56 GHz

Source: http://www.ieee802.org/3/ck/public/18_05/lim_3ck_01a_0518.pdf

Cable assembly and Channel IL - Baseline

- Cable assembly Max IL dB @ 26.56 GHz= 10 (bulk cable) + (2*2.3) (TF) +(2*1.5) (connector) = 17.6 dB
- Cable assembly Min IL dB @ 26.56 GHz= 2.5 (bulk cable) + (2*2.3) (TF) +(2*1.5) (connector) = 10.1 dB
- Channel Max IL dB @ 26.56 GHz= 17.6 (Cable assembly) +2*11.5 (TP0-TP2)- (2*6.3) MTF = 28 dB
- Channel Min IL dB @ 26.56 GHz= 10.1 (Cable assembly) +2*11.5 (TP0-TP2)- (2*6.3) MTF = 20.5 dB
- Channel Max IL dB @26.56 GHz =10 (bulk cable)+(2*7) Host IL +(2*2) Host connector IL = 28 dB



Note: The connector insertion loss is 1.5 dB for the mated test fixture. The host connector is allocated 0.5 dB for implementation allowance.

Adopt Channel and Cable Assembly IL @ 26.56 GHz with TBD

Cable assembly – baseline

- Cable assembly specifications – Adopt CL136 – referenced parameters @ 26.56 GHz, f=0.01≤f≤38 (signaling rate 53.125 GBd).

Cable assembly characteristics summary

Parameter description	Value	Unit
Maximum insertion Loss	17.6 (TBD)	dB
Minimum Insertion Loss	10.1 (TBD)	dB
Minimum ERL	TBD	dB
Differential to Common-mode return loss	Equation(TBD)	dB
Differential to Common-mode conversion loss	Equation(TBD)	dB
Common-mode to common–mode return loss	Equation(TBD)	dB
Minimum COM	TBD	dB

Adopt cable assembly parameters with TBD

802.3bj/by/cd - Test Fixture PCB IL

- 92.11.1.2 Test fixture insertion loss equation (92-34)

$$IL_{tfref}(f) = -0.00144 + 0.13824\sqrt{f} + 0.06624\,f \qquad \text{(dB)}$$

for $0.01 \le f \le 25$ GHz

where

f	is the frequency in GHz
$IL_{tfref}(f)$	is the reference test fixture PCB insertion loss at frequency f

- 92.11.1.2 Test fixture insertion loss equation (92-34)

$$IL_{catf}(f) = -0.00125 + 0.12\sqrt{f} + 0.0575f \qquad \text{(dB)}$$

for $0.01\ \text{GHz} \le f \le 25$ GHz

where

f	is the frequency in GHz
$IL_{catf}(f)$	is the reference test fixture printed circuit board insertion loss at frequency f

TP0-TP3 test fixture IL - HCB

$$IL_{tfref}(f) = -0.00144 + 0.13824\sqrt{f} + 0.06624\,f \quad \text{(dB)}$$

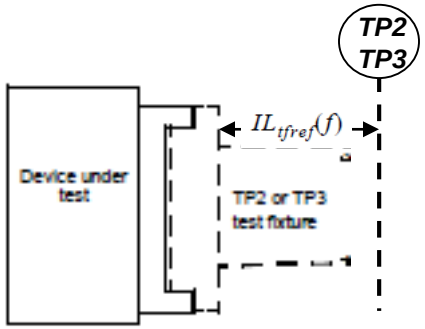
for $0.01 \le f \le 25$ GHz

where

f is the frequency in GHz

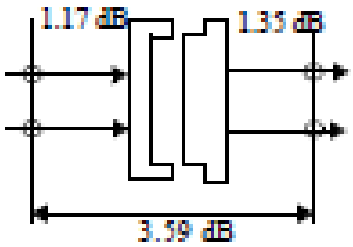
$IL_{tfref}(f)$ is the reference test fixture PCB insertion loss at frequency f

IL @ 12.89 GHz = 1.35 dB
IL @ 13.28 GHz = 1.38 dB
IL @ 26.56 GHz = 2.47 dB

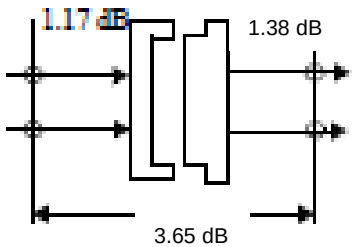


Adopt TP0 or TP3 Test Fixture IL: For 0.01 GHz ≤ f ≤ 40 GHz with TBD

IL @ 12.89 GHz

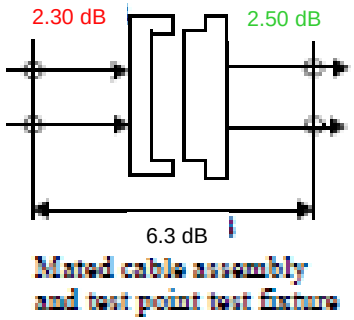


IL @ 13.28 GHz



NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

IL @ 26.56 GHz



- Note: The connector insertion loss is 1.5 dB for the mated test fixture. The host connector is allocated 0.5 dB for implementation allowance.

Cable assembly test fixture IL - MCB

$$IL_{catf}(f) = -0.00125 + 0.12\sqrt{f} + 0.0575f \quad \text{(dB)}$$ *TBD*

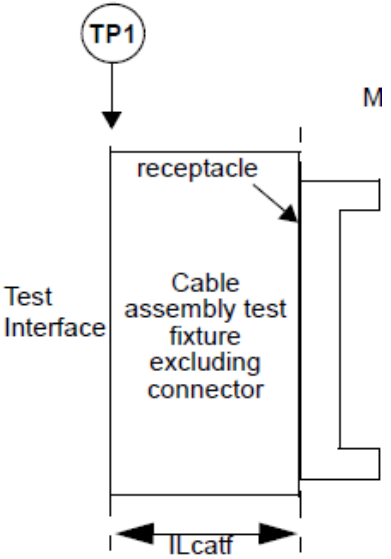
for 0.01 GHz ≤ f ≤ 25 GHz

where

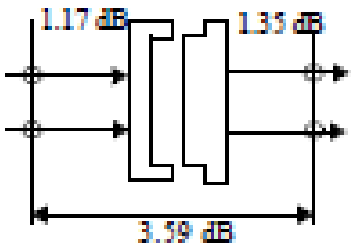
f is the frequency in GHz

$IL_{catf}(f)$ is the reference test fixture printed circuit board insertion loss at frequency f

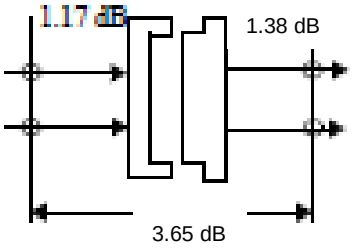
IL @ 12.89 GHz = 1.17 dB
IL @ 13.28 GHz = 1.20 dB
IL @ 26.56 GHz = 2.14 dB



IL @ 12.89 GHz

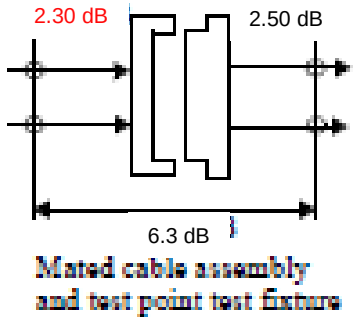


IL @ 13.28 GHz



NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

IL @ 26.56 GHz



Adopt cable assembly test fixture IL with TBD:
For 0.01 GHz ≤ f ≤ 40 GHz

Note: The connector insertion loss is 1.5 dB for the mated test fixture. The host connector is allocated 0.5 dB for implementation allowance.

Cable assembly test fixture reference IL

The reference insertion loss of the mated test fixture is determined using Equation (136B–1).

$$IL_{MatedTF}(f) = 0.471\sqrt{f} + 0.1194f + 0.002f^2 \text{ (dB)} \quad (136B\text{–}1)$$

for $0.01 \text{ GHz} \le f \le 25 \text{ GHz}$

GHz	dB
13.28	3.65
26.56	7.01

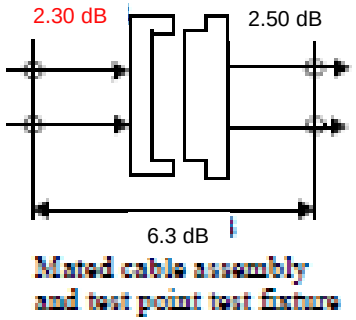
where

f is the frequency in GHz

ILmatedTF(f)=0.899(0.471*SQRT(f)+0.1194*f+0.002*f^2)*

GHz	dB
26.56	6.3

IL @ 26.56 GHz



Adopt cable assembly test fixture reference IL with TBD:
For 0.01 GHz ≤ f ≤ 40 GHz

Note: The connector insertion loss is 1.5 dB for the mated test fixture. The host connector is allocated 0.5 dB for implementation allowance

Cable Assembly COM- Baseline

- COM - consistent with methodology CL136 – signaling rate 53.125 GBd
- COM parameter values TBD

Table 136–18—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step[a]	Δf	0.01	GHz
Device package model			
Single-ended device capacitance	C_d	1.8×10^{-4}	nF
Transmission line length, Test 1	z_p	12	mm
Transmission line length, Test 2	z_p	30	mm
Single-ended package capacitance at package-to-board interface	C_p	1.1×10^{-4}	nF
Package transmission line characteristic impedance	Z_c	95	Ω
Single-ended reference resistance	R_0	50	Ω

TBD

Table 136–18—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, 1st pre-cursor coefficient	$c(-1)$		—
Minimum value		–0.25	
Maximum value		0	
Step size		0.05	
Transmitter equalizer, 2nd pre-cursor coefficient	$c(-2)$		—
Minimum value		0	
Maximum value		0.1	
Step size		0.025	
Transmitter equalizer, post-cursor coefficient	$c(1)$		—
Minimum value		–0.25	
Maximum value		0	
Step size		0.05	
Continuous time filter, DC gain	g_{DC}		
Minimum value		–20	dB
Maximum value		0	dB
Step size		1	dB
Continuous time filter, DC gain 2	g_{DC2}		
Minimum value		–6	dB
Maximum value		0	dB
Step size		1	dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	$f_b / 2.5$	GHz
Continuous time filter, pole frequencies	f_{p1}	$f_b / 2.5$	GHz
	f_{p2}	$2 \times f_b$	GHz
Continuous time filter, low-frequency pole/zero	f_{LF}	$f_b / 40$	GHz
Transmitter differential peak output voltage			
Victim	A_v	0.415	V
Far-end aggressor	A_{fe}	0.415	V
Near-end aggressor	A_{ne}	0.604	V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	UI
Normalized DFE coefficient magnitude limit	$b_{max}(n)$		—
for $n = 1$		0.7	
for $n = 2$ to N_b		0.2	
Random jitter, RMS	σ_{RJ}	0.01	UI

TBD

Test Fixtures

- Test Fixture specifications – Adopt– referenced parameters 26.56 GHz f=0.01≤f≤40 (signaling rate 53.125 GBd).

Mated test fixtures parameters

Parameter description	Value	Unit
Maximum differential insertion Loss	Equation(TBD)	dB
Minimum differential Insertion Loss	Equation(TBD)	dB
Reference differential insertion loss	Equation (slide 22) TBD	dB
Figure of Merit(FOM) ILD	Equation(TBD)	dB
Minimum Differential Return Loss	Equation(TBD)	dB
Common-mode conversion insertion loss	Equation(TBD)	dB
Common-mode return loss	Equation(TBD)	dB
Common-mode to differential –mode return loss	Equation(TBD)	dB
Integrated crosstalk noise	(TBD)	mV

Adopt mated test fixture parameters with TBD

MDI/plug connector - Baseline

- References to 136C (support for 56.125 GbD - TBD)

Table 136C–1—Number of PMDs supportable for each connector type

MDI types	50GBASE-CR	100GBASE-CR2	200GBASE-CR4	Reference
SFP28	1	—	—	110.11.1
QSFP28	1, 2, 4	1, 2	1	92.12.1.1
microQSFP	1, 2, 4	1, 2	1	136C.2.3
QSFP-DD	1, 2, 4, 8	1, 2, 4	1, 2	136C.2.4
OSFP	1, 2, 4, 8	1, 2, 4	1, 2	136C.2.5

100GBASE-CR	200GBASE-CR	400GBASE-CR

- Addition of MDI/plugs – TBD -

  Consider: palkert_3ck_01_0918.pdf

Call to action

- *Please provide inputs on values to close the TBDs.*