A Dual-Duplex PAM4 100Gbps PHY Analysis

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Supporters

- Jon Lewis (DELL)
- George Zimmerman (CME)

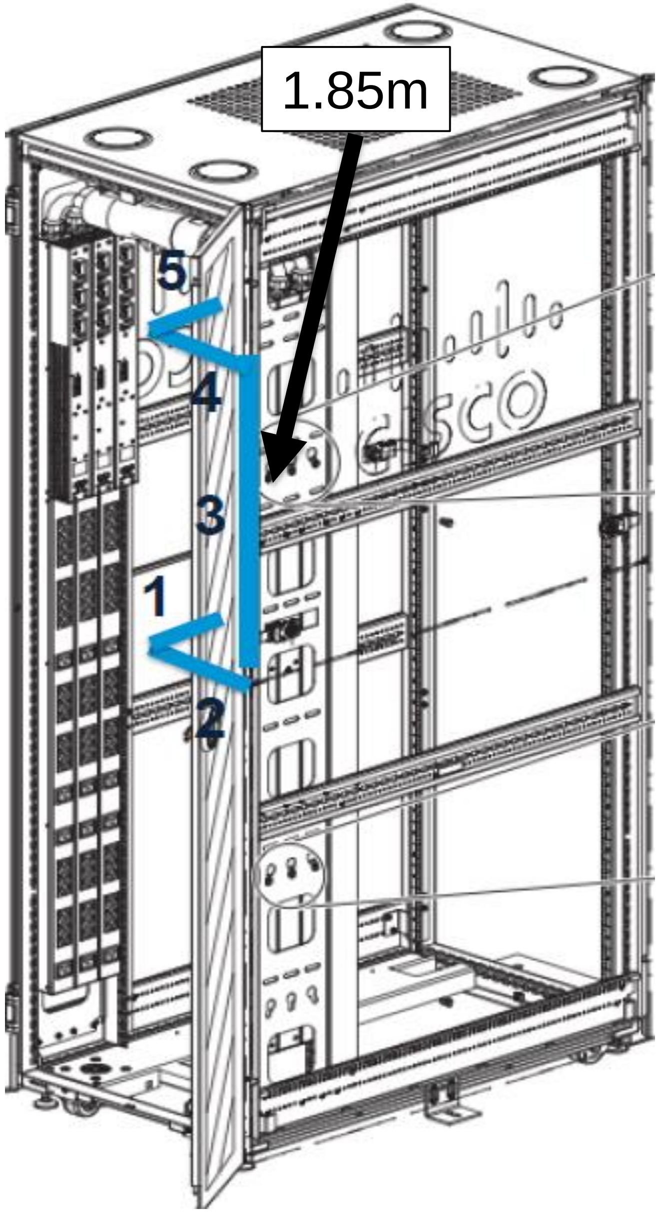
100Gbps Over 2m+ Passive Copper Cables

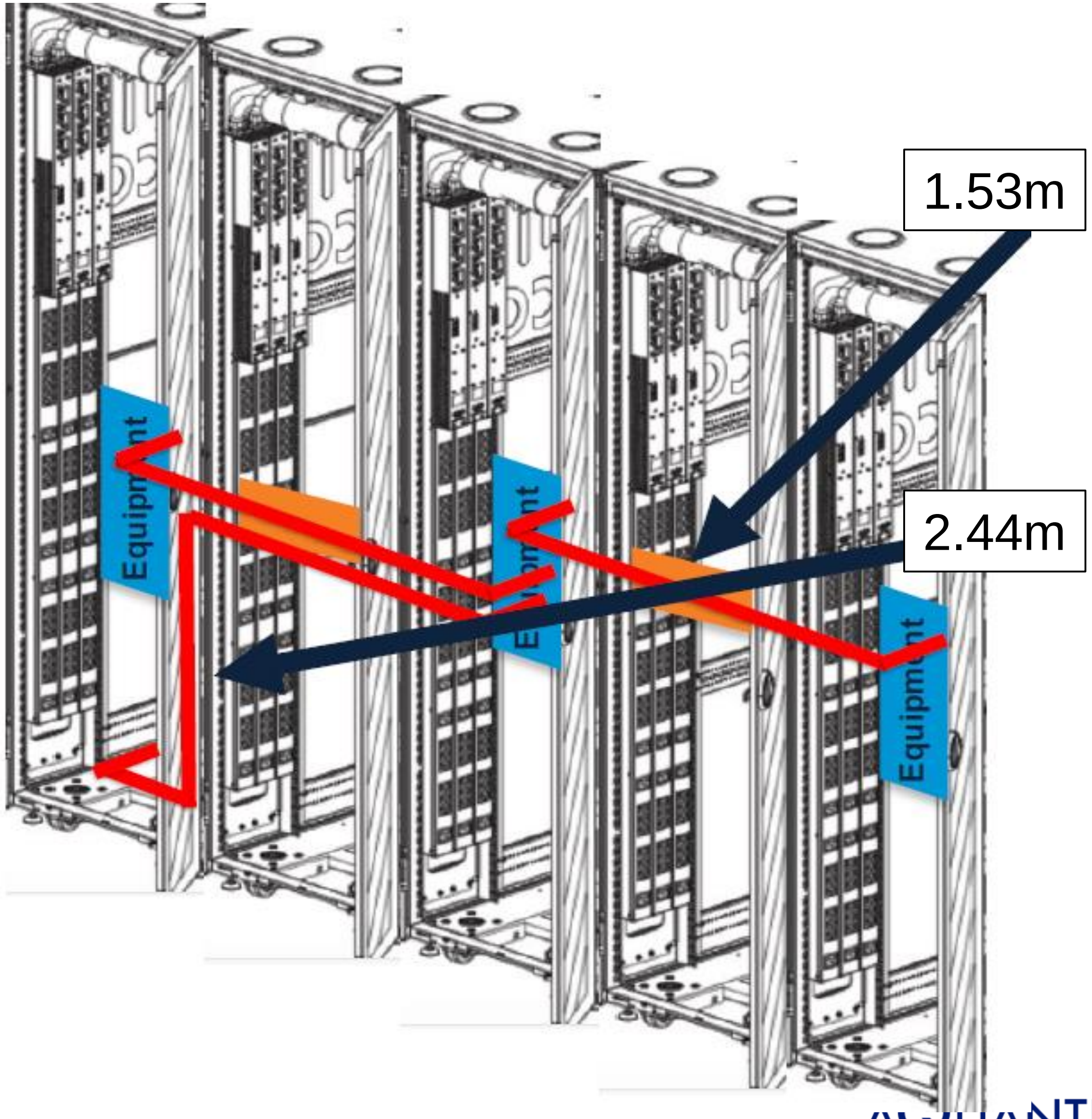
- The committee has mostly focused on technical feasibilities of Chip-to-Module & Chip-to-Chip solutions

- One of the key 8032.3ck objectives still remains to define single-lane 100 Gb/s PHY for operation over passive copper cables with lengths up to at least 2m

- 53Gbaud PAM4 signaling has not provided a reliable solution (with a practical SNR margin) over any of the proposed copper cable channels with at least 2m length
  - To further complicate the matter, to cover majority of existing applications of passive copper cables, we need at least ~2.5m reach
- Should the committee consider alternative signaling schemes that can provide a practical solution for the passive copper cable objective as well?

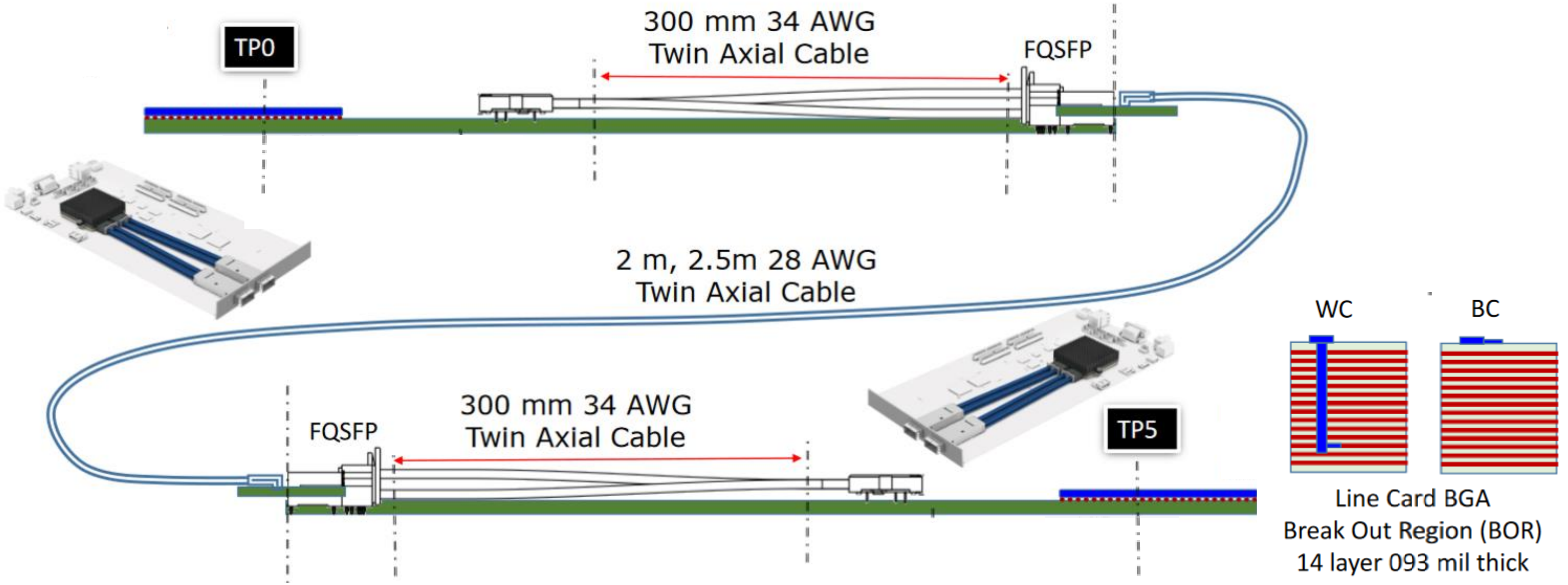
Common Data Center Cabling Installation Topologies





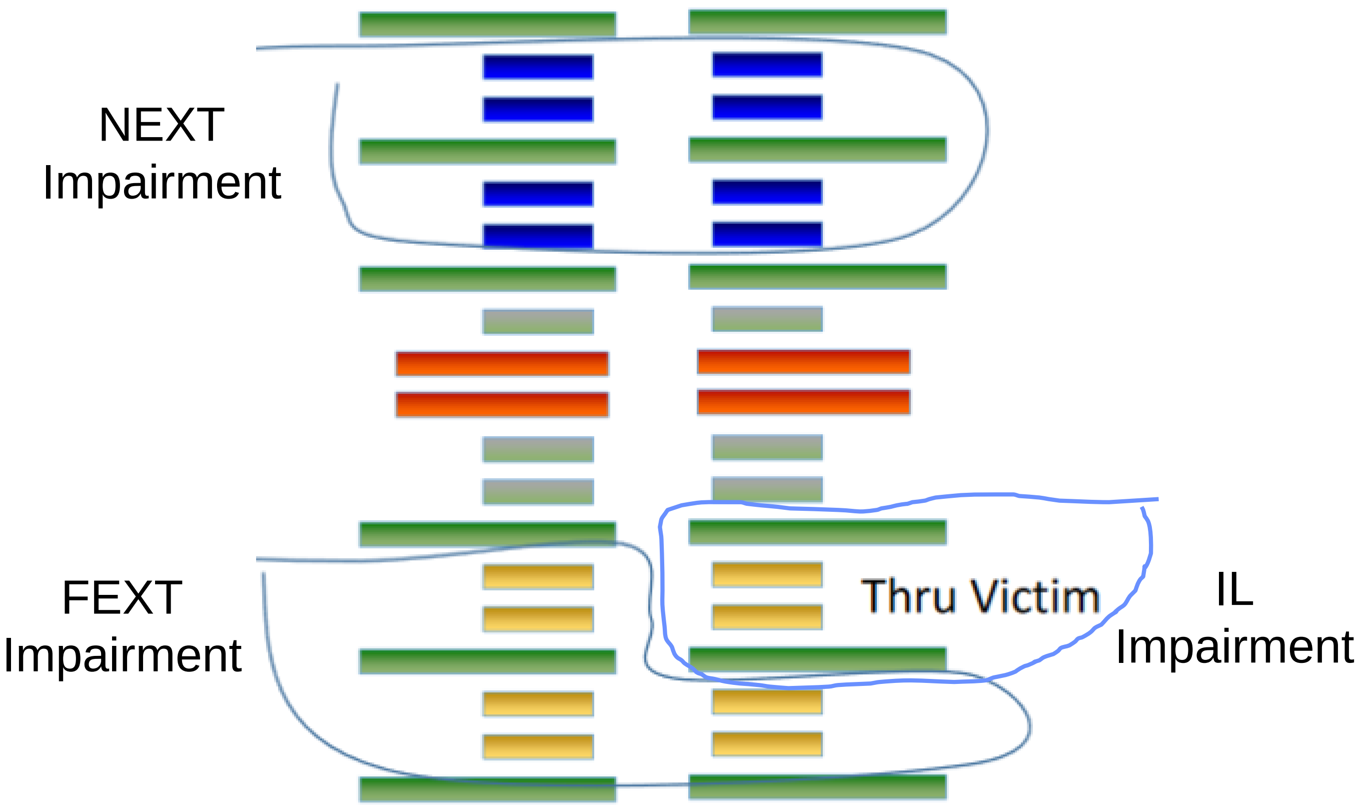
Common installation topologies presented in goergen_100GEL_01_0318 (Cisco)

Selected Passive Copper Cable Channel Topology



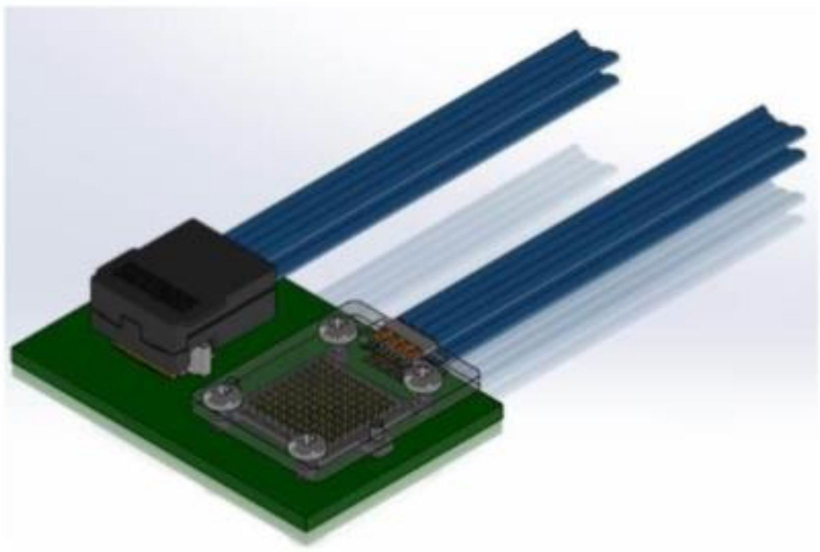
- Channel model used is the proposed topology in mellitz_100GEL_adhoc_01_021218 :
  - 2.5m of 28-AWG Cable + 2 x 0.3m 34-AWG Cable → Total Cable Length = 3.1m
- Worst-Case (WC) and Best-Case (BC) line card break-out considered
  - Total of 32 S-parameters per case with all mutual crosstalk sources (NEXT & FEXT) included

Thru & Crosstalk Channels in Single-Duplex Mode



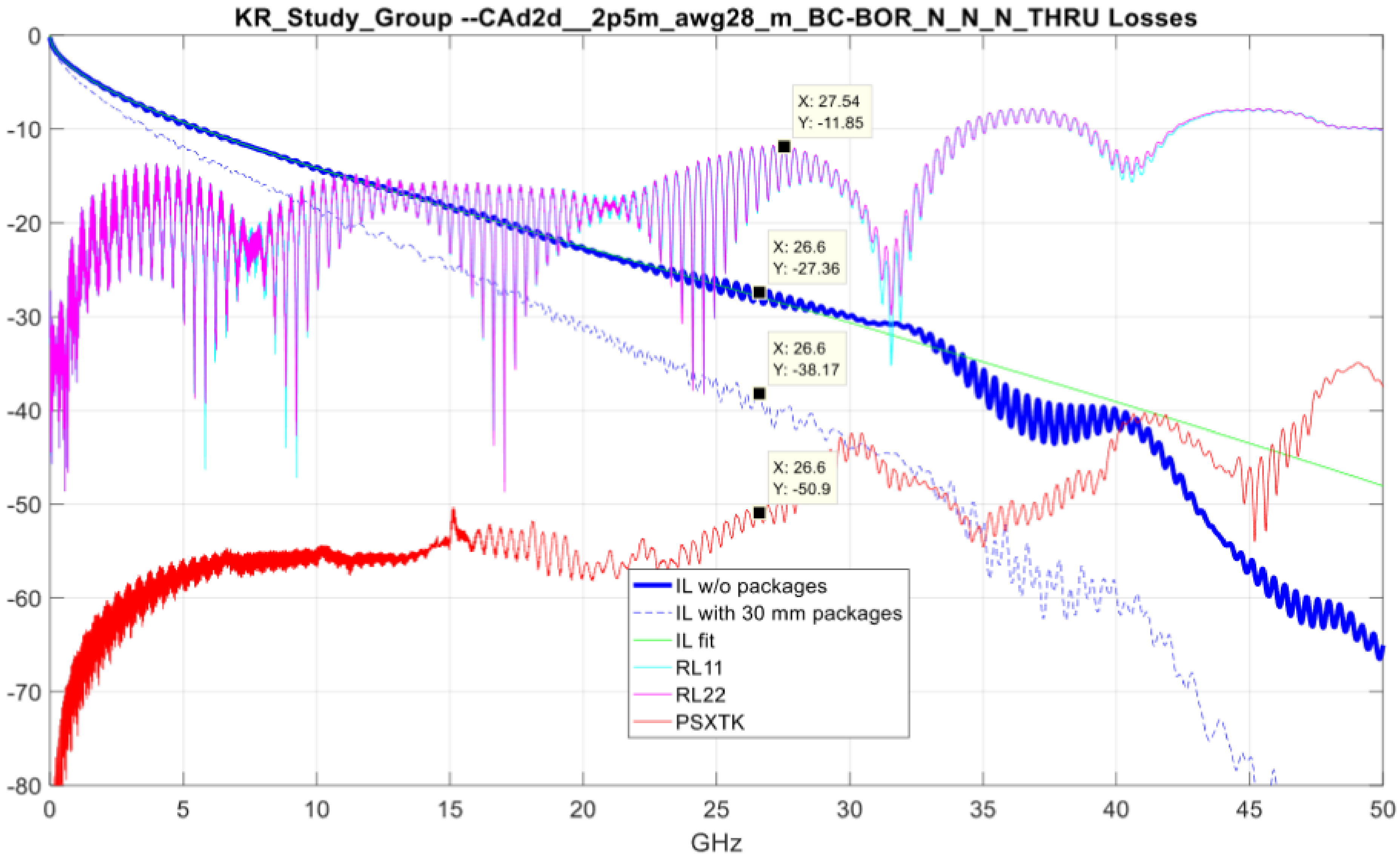
Receive signal runs over separate cable bundle from transmit, therefore NEXT magnitude will be negligible

mellitz_3ck_02_0518



Single Duplex (SD): Simultaneous transmit & receive over separate physical channels

Selected Channel Frequency Transfers

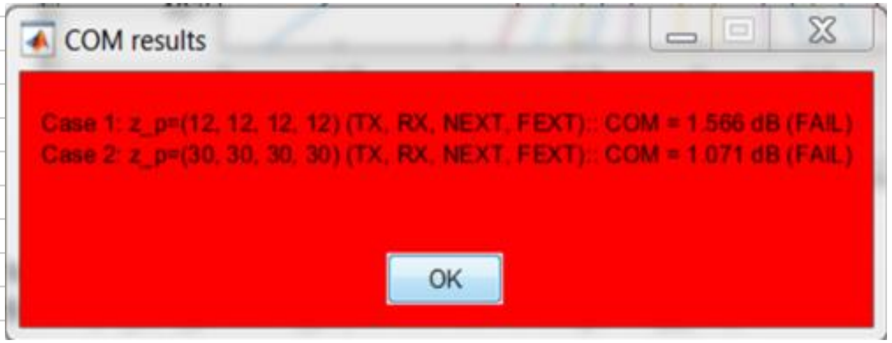


53Gbaud PAM4-SD SNR Results for 2.5m BC Channel

A	B	C	D
Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.5e-4 1.5e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 30]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[0.08e-4 0.08e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.45	V	
A_fe	0.45	V	
A_ne	0.63	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		[min:step:max]
c(-3)	[-0.1:0.025:0]		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	0		[min:step:max]
N_b	1	UI	
b_max(1)	0.7		
g_DC	[-16:0.5:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-12:1:-6]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	4	UI	
ffe_post_tap_len	27	UI	

F	G	H
I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	AQ_check_001	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
DER_0	1.00E-04	
Include PCB	0	Value
T_r	7.00E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.18**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	35	dB
R_LM	0.96	

J	K	L
Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	90	Ohm (tdr sel)
Table 92–12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	110	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm



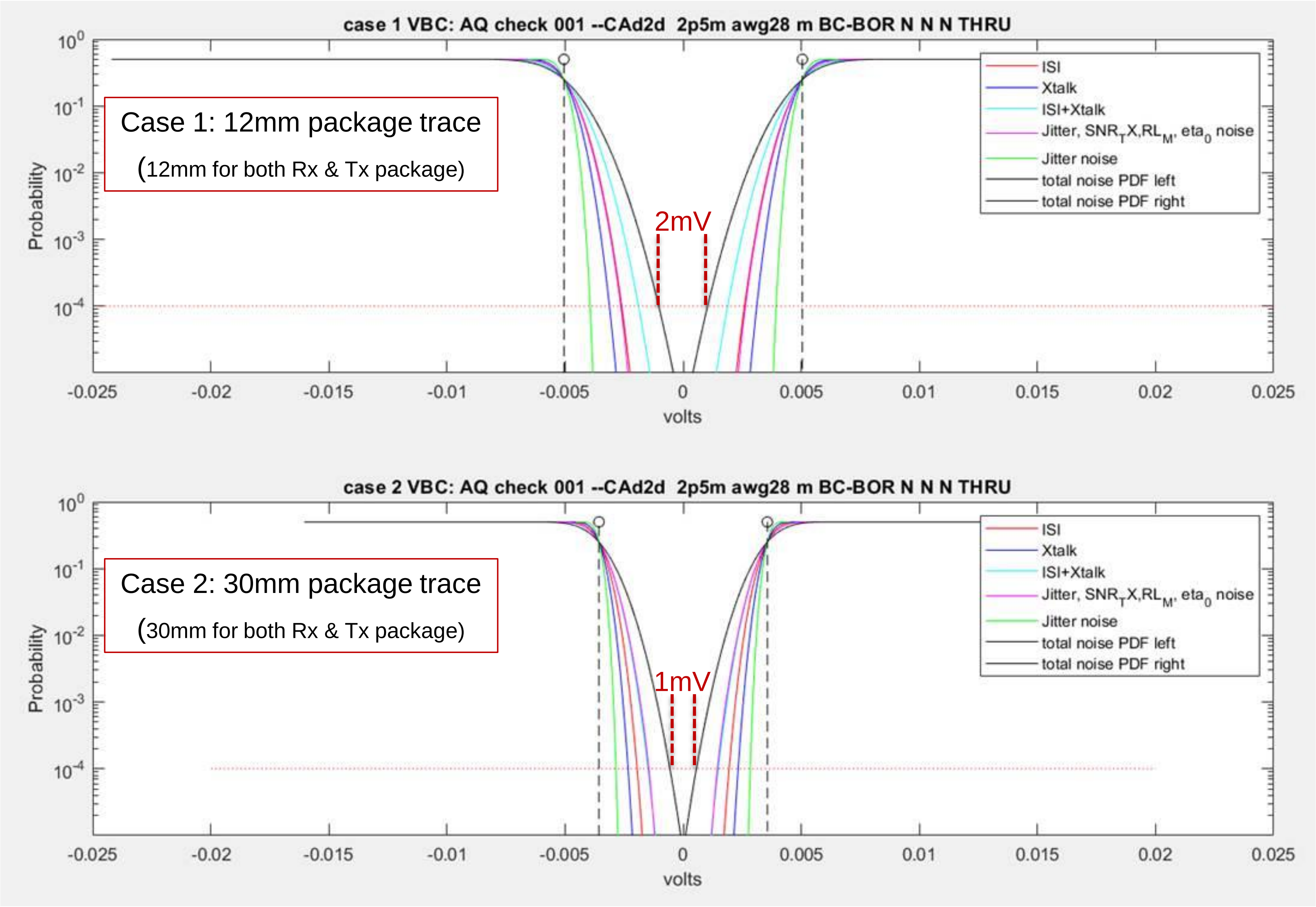
Fails to meet minimum 3dB SNR margin with

– 32-tap FFE + 1-tap DFE

Case 1: 12mm package trace

Case 2: 30mm package trace

53Gbaud PAM4-SD Vertical Eye Opening Results for 2.5m BC



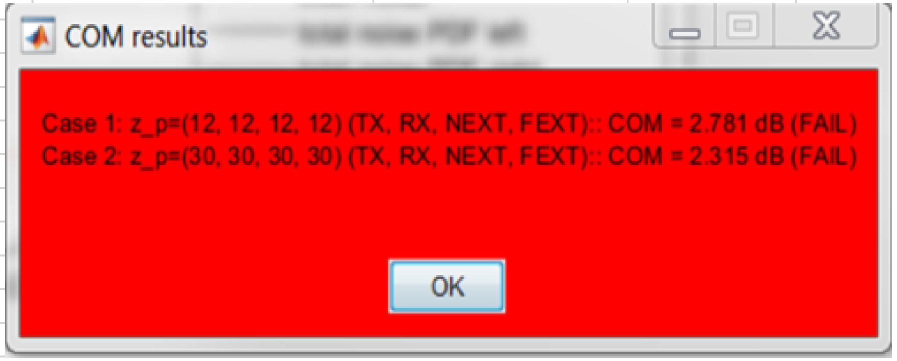
53Gbaud PAM4-SD SNR Results for 2.5m BC Channel

A	B	C	D
Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.5e-4 1.5e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 30]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[0.08e-4 0.08e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.45	V	
A_fe	0.45	V	
A_ne	0.63	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		[min:step:max]
c(-3)	[-0.1:0.025:0]		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	0		[min:step:max]
N_b	32	UI	
b_max(1)	0.7		
g_DC	[-16:0.5:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-12:1:-6]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	4	UI	
ffe_post_tap_len	60	UI	

F	G	H
I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	AQ_check_001	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
DER_0	1.00E-04	
Include PCB	0	Value
T_r	7.00E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.18**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	35	dB
R_LM	0.96	

J	K	L
Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	90	Ohm (tdr sel)

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	110	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm



Comes barely close to the required 3dB SNR margin with

- 64-tap FFE + 32-tap DFE
- Definitely not a practical solution!

53Gbaud PAM4-SD SNR Results for 2.0m BC Channel

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.5e-4 1.5e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 30]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[0.08e-4 0.08e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.45	V	
A_fe	0.45	V	
A_ne	0.63	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		[min:step:max]
c(-3)	[-0.1:0.025:0]		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	0		[min:step:max]
N_b	1	UI	
b_max(1)	0.7		
g_DC	[-16:0.5:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-12:1:-6]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	4	UI	
ffe_post_tap_len	27	UI	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	AQ_check_001	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
DER_0	1.00E-04	
Include PCB	0	Value
T_r	7.00E-03	ns
FORCE_TR	1	logical

TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.18**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	35	dB
R_LM	0.96	

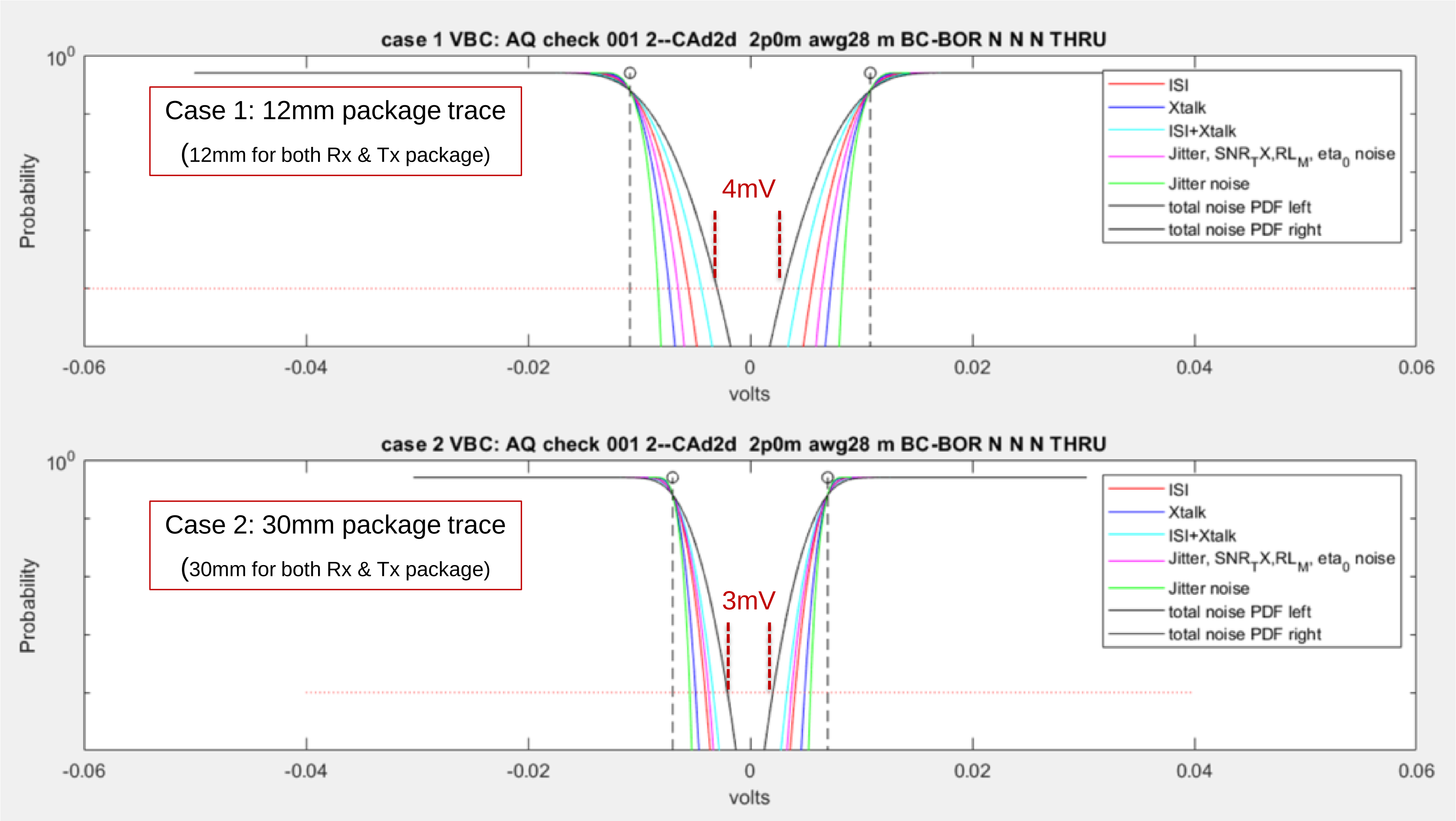
Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	90	Ohm (tdr sel)

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	110	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

Fails to meet minimum 3dB SNR margin at 2.0m cable as well with

– 32-tap FFE + 1-tap DFE

53Gbaud PAM4-SD Vertical Eye Opening Results 2.0m for BC



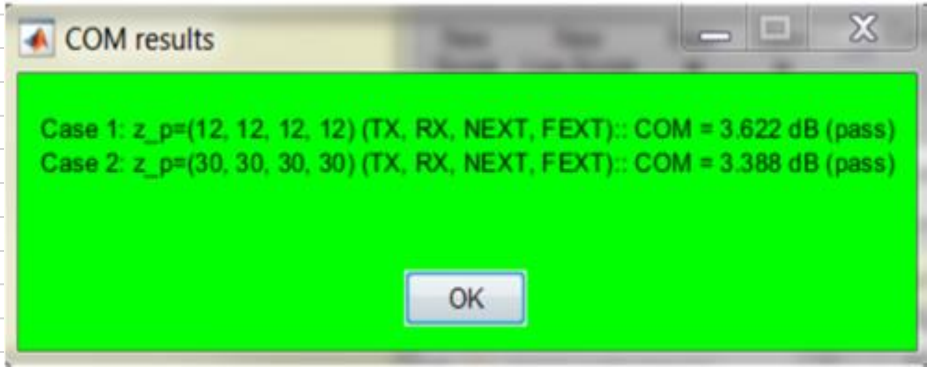
53Gbaud PAM4-SD SNR Results for 2.0m BC Channel

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.5e-4 1.5e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 30]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[0.08e-4 0.08e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.45	V	
A_fe	0.45	V	
A_ne	0.63	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		[min:step:max]
c(-3)	[-0.1:0.025:0]		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	0		[min:step:max]
N_b	32	UI	
b_max(1)	0.7		
g_DC	[-16:0.5:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-12:1:-6]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	4	UI	
ffe_post_tap_len	60	UI	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	AQ_check_001	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
DER_0	1.00E-04	
Include PCB	0	Value
T_r	7.00E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.18**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	35	dB
R_LM	0.96	

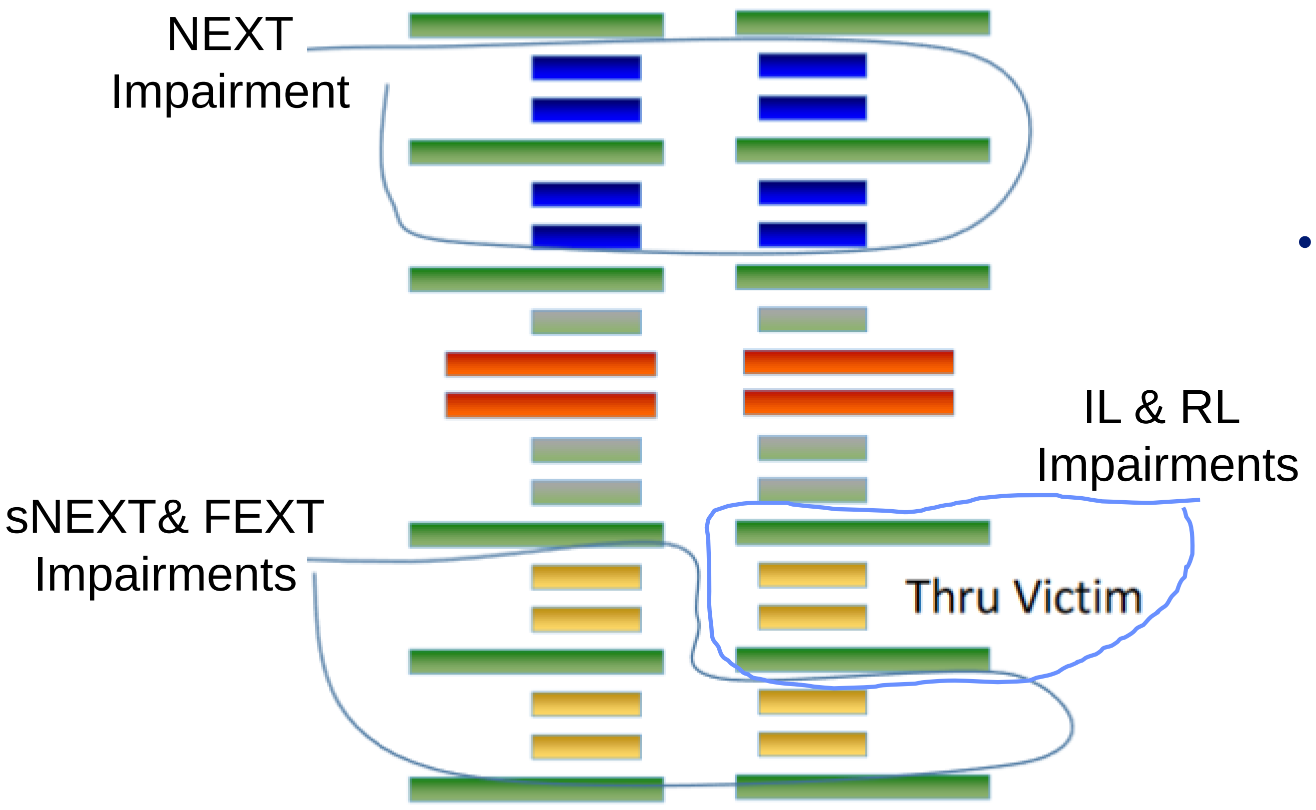
Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	90	Ohm (tdr sel)

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	110	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm



- Barely passes the required 3dB SNR margin using excessively long filters:
  - 64-tap FFE + 32-tap DFE
  - Definitely not a practical solution either

Thru & Crosstalk Channels for 26.5Gbuad PAM4 Dual Duplex

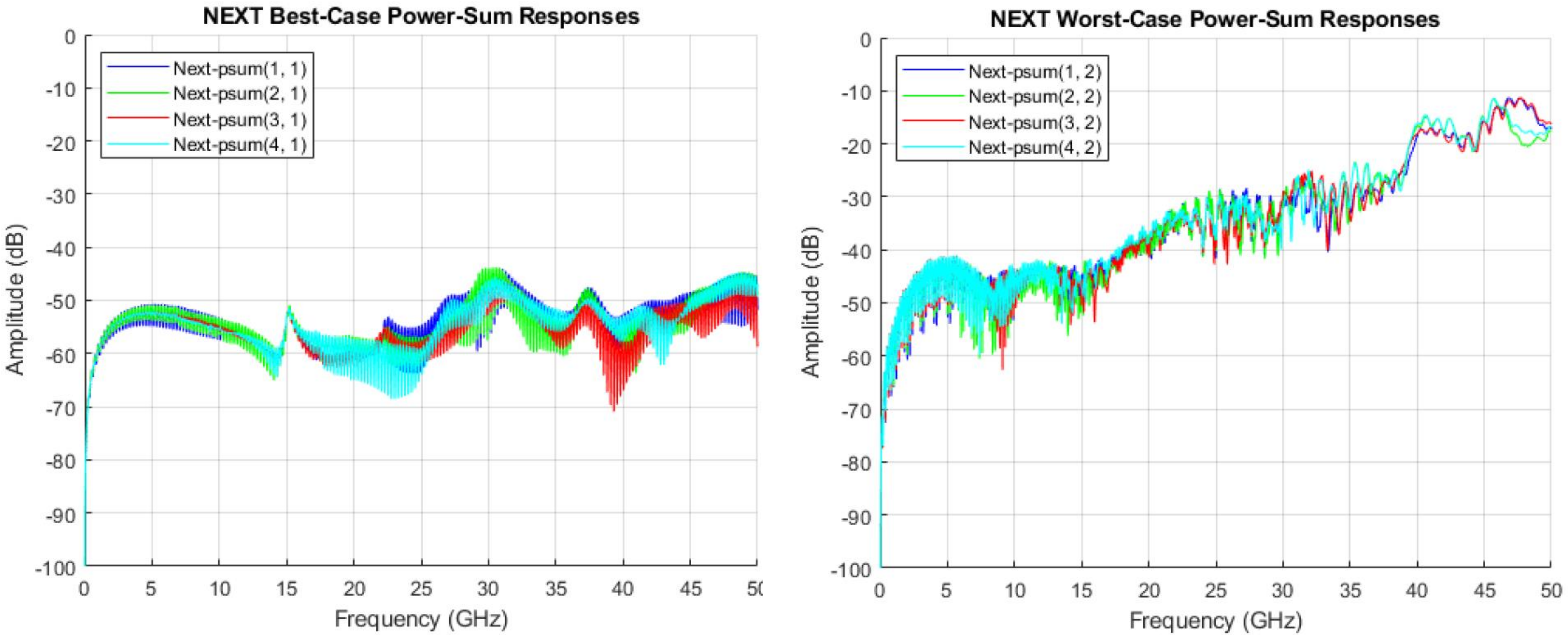


- A dual-duplex transceiver is exposed to two additional signal impairments:
  - Echo: reflection signals from its own transmitter
  - sNext: self near-end xtalk signals from transmitters in the same bundle

- Depending on the magnitude of these extra impairments, we may have to cancel them or accept their SNR degradation.
  - In the selected channel (at MDI input)
    - Signal/Echo=~10dB
      ➔ Echo canceller are necessary
    - Signal/Xtalk=30-40dB
      ➔ Evaluate if Xtalk cancellers are necessary

Dual Duplex (DD): Simultaneous transmit and receive over same physical channel

sNEXT Power-Sum in Dual Duplex Mode



- Compare the 100Gbps SNR performance of 26.5Gbaud DD (with sNEXT impairment) versus the SNR performance of 53Gbaud SD over the BC channel using the COM tool

26.5Gbaud PAM4-DD SNR for 2.5m BC Channel + sNEXT

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	26.5625	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.5e-4 1.5e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 30]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[0.08e-4 0.08e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.45	V	
A_fe	0.45	V	
A_ne	0.63	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.25:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.15]		[min:step:max]
c(-3)	0		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	0		[min:step:max]
N_b	1	UI	
b_max(1)	0.7		
g_DC	[-16:0.5:0]	dB	[min:step:max]
f_z	5.3125	GHz	
f_p1	5.3125	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-12:1:-6]		[min:step:max]
f_HP_PZ	0.66406	GHz	
ffe_pre_tap_len	2	UI	
ffe_post_tap_len	13	UI	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	AQ_check_001	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
DER_0	1.00E-04	
Include PCB	0	Value
T_r	7.00E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.18**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	5.55E-08	V^2/GHz
SNR_TX	35	dB
R_LM	0.96	

Table 93A–3 parameters		
Parameter	Setting	Units
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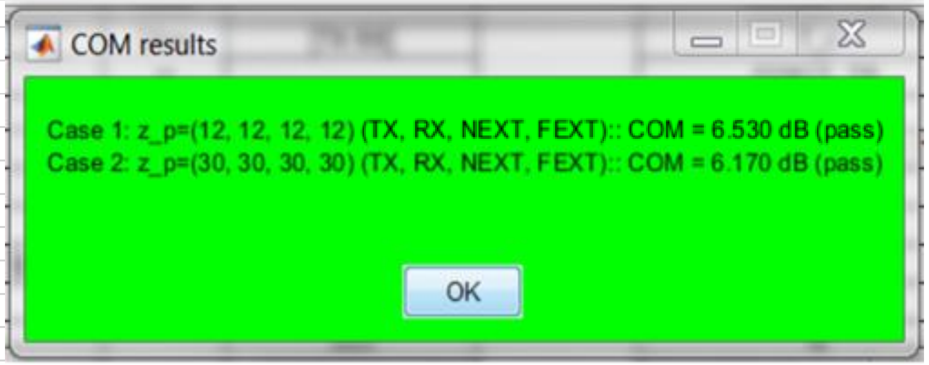
package_tl_tau	6.141E-03	ns/mm
package_Z_c	90	Ohm (tdr sel)

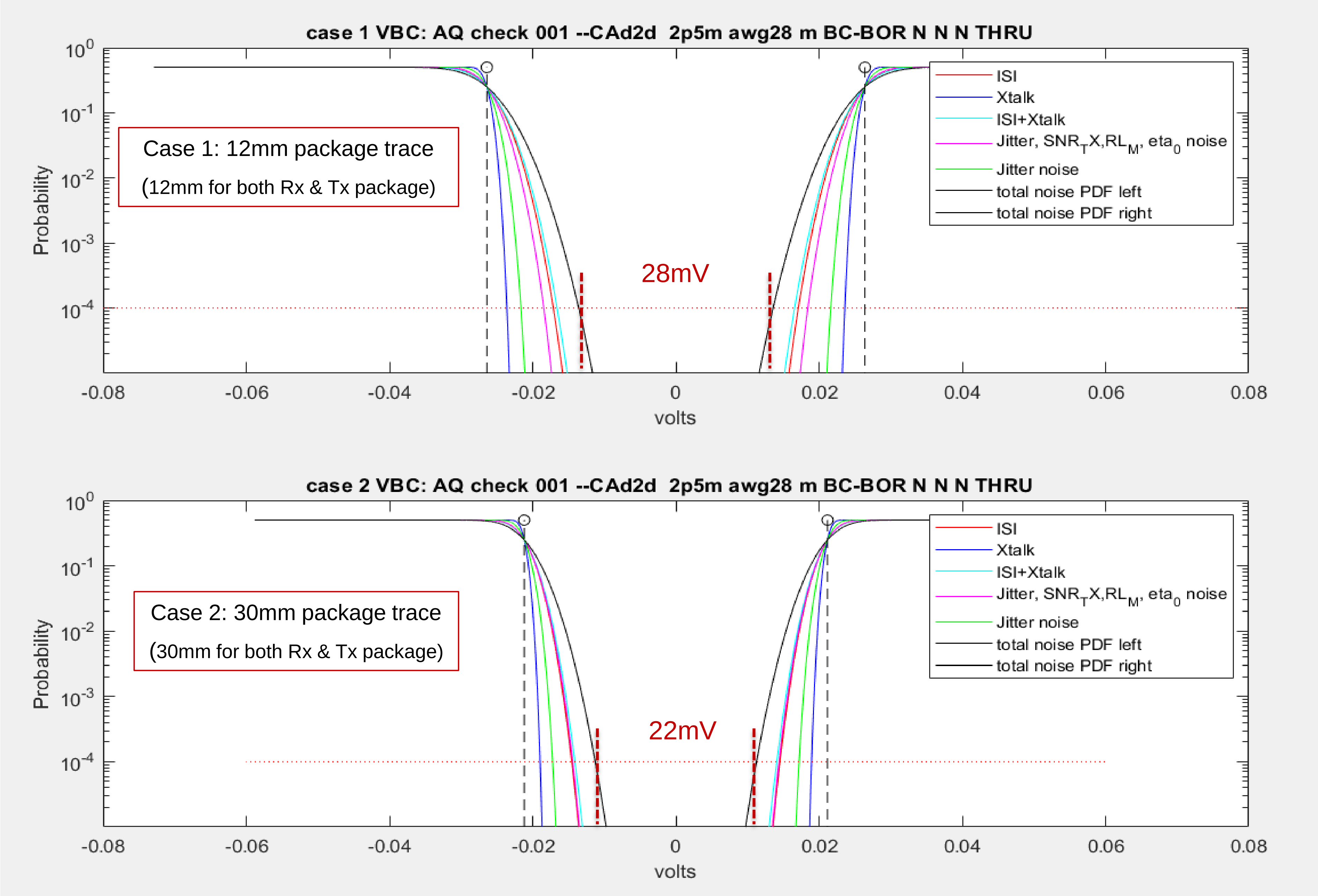
Table 92–12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	110	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm



- Passes by more than 6dB SNR margin
  - Needs only <u>16-tap FFE</u> + <u>1-tap DFE</u>

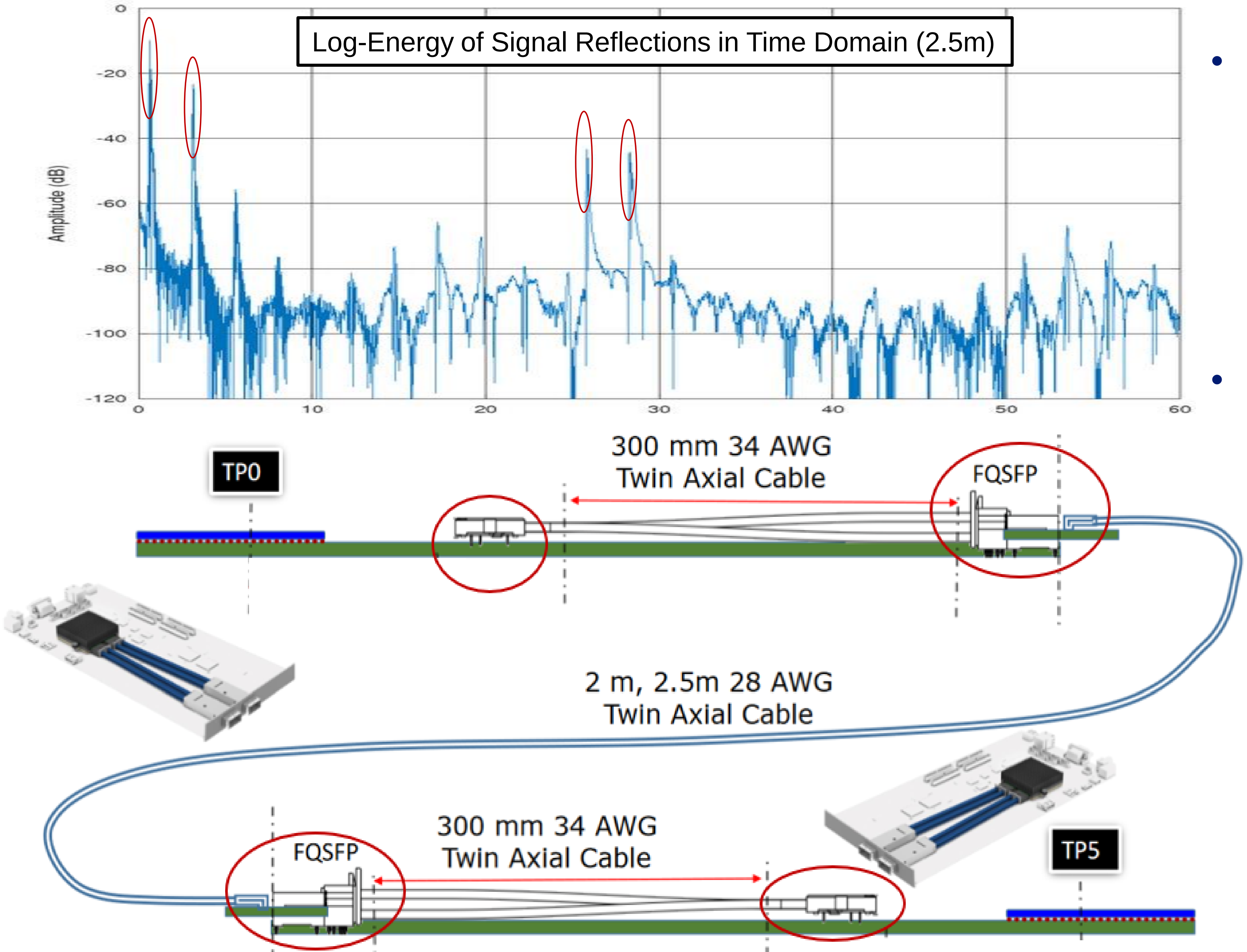
- Case 1: 12mm package trace
- Case 2: 30mm package trace

26.5Gbaud PAM4-DD Vertical Eye Opening for 2.5m BC + sNEXT



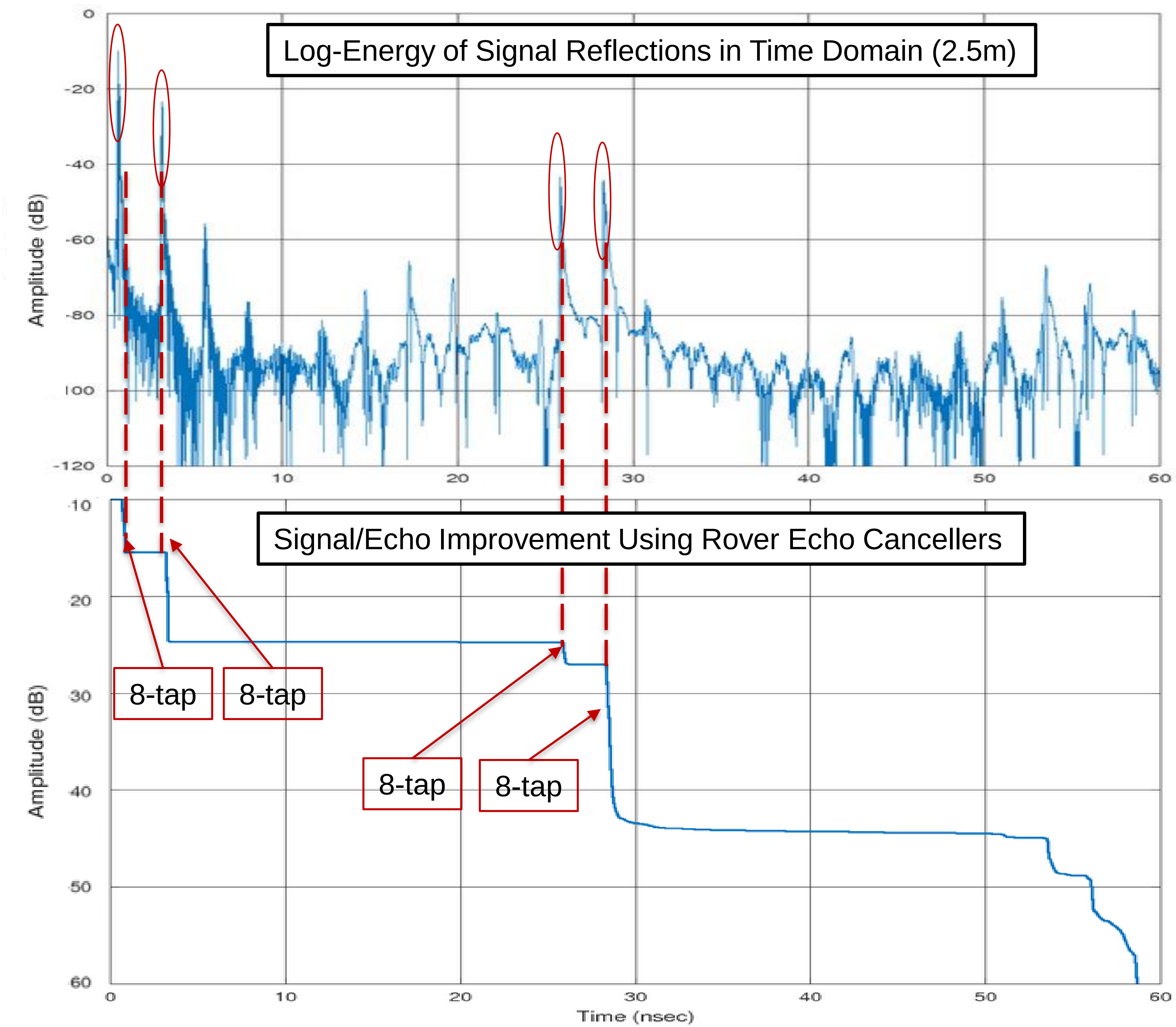
- 26.5Gbaud DD signaling shows more than 10x larger vertical eye opening versus 53Gbaad SD mode even after adding sNEXT impairment

Echo Impairment for 26.5Gbaud PAM4-DD Mode (2.5m)



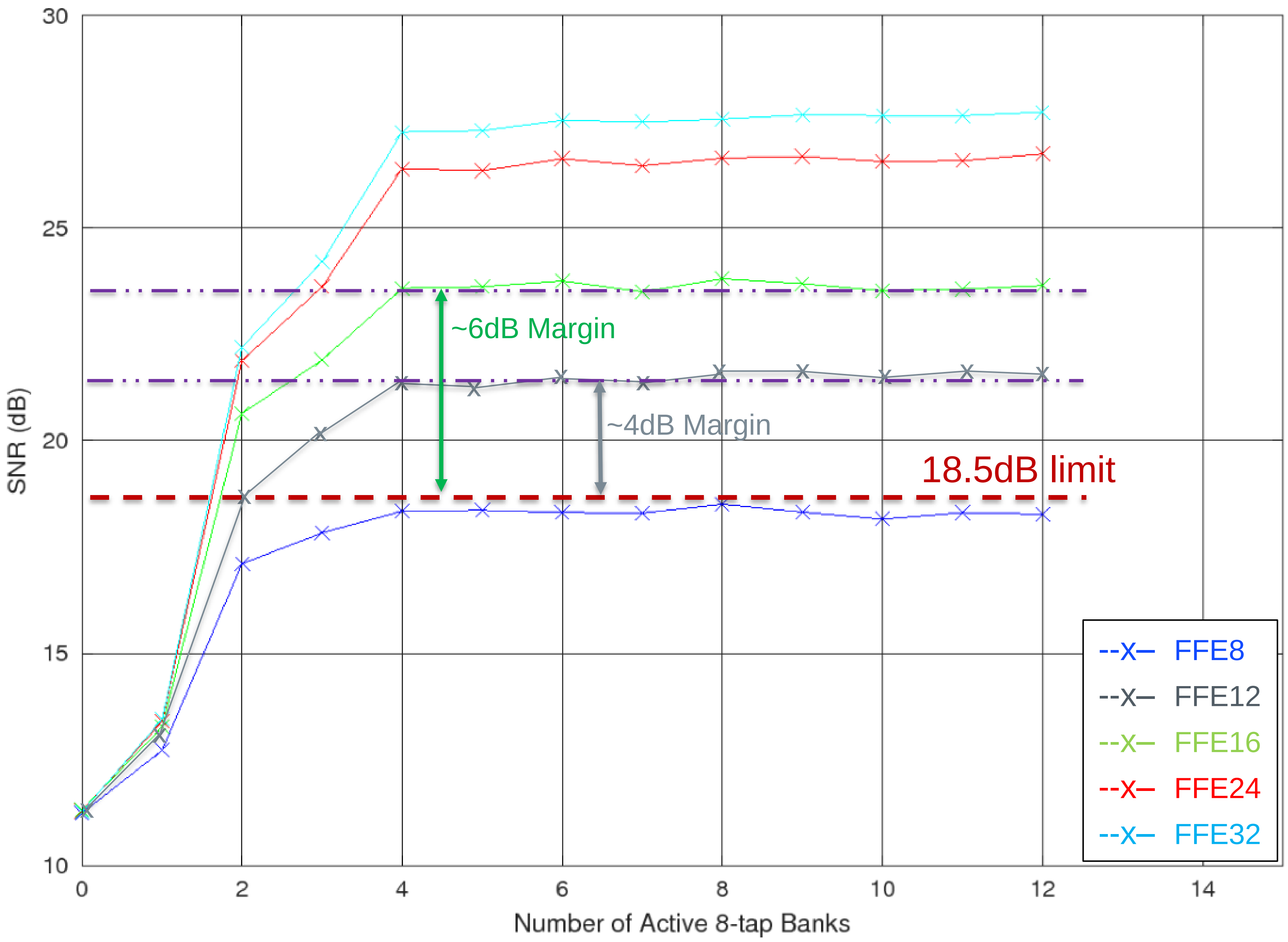
- The dominant reflections happen at the connectors, while there is very minimal echo power along the cable length itself
- Echo cancellation at connector locations removes majority of the echo power

Echo Impairment for 26.5Gbaud PAM4-DD Mode (2.5m)



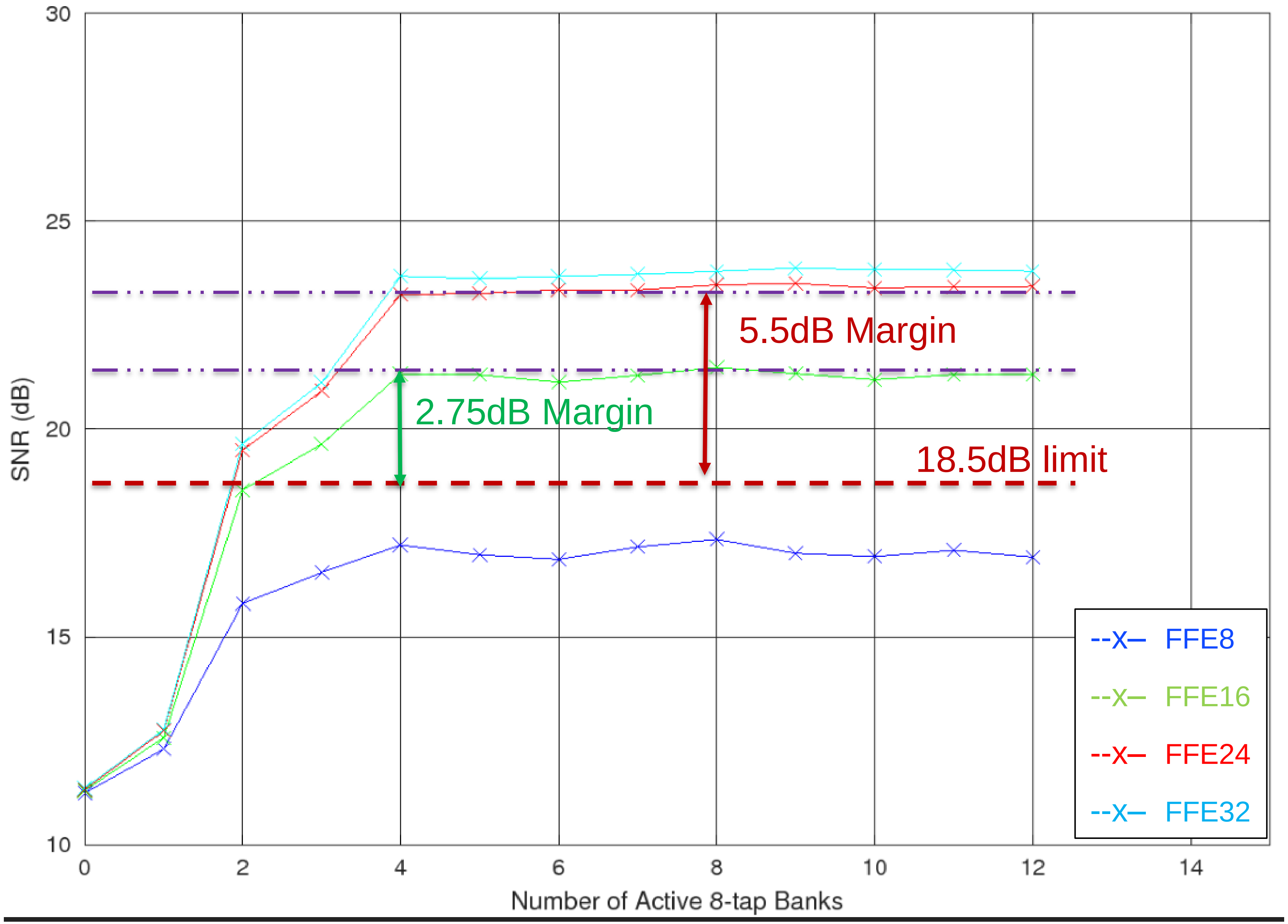
- To achieve DER<1E-4, the total link SNR including all impairments must be >18.5dB
- Separate Rover Echo Canceller segments can be independently moved to cancel each major discontinuity in the RL channel
- A total of four 8-tap Rover Echo Cancellers is shown to considerably improve the Signal/Echo (S/E) ratio for Mellitz 2.5m channel:
  - No Echo Canceller→ S/E=~10dB
  - 4 Echo Cancellers→ S/E=~45dB
- S/E=~45dB is significantly below the required SNR=18.5dB to degrade the link performance

26.5Gbaud DD SNR with Different FFE/Echo Filters Over 2.5m BC Channel

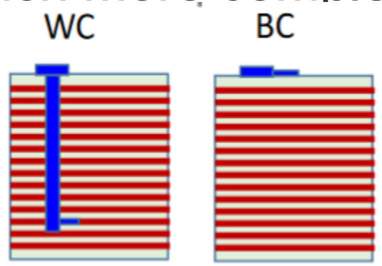


- All cases use 1-tap DFE
- SNR performance curves are for different FFE lengths and increasing # of active 8-tap Echo canceller segments
- As shown by COM tool,16-tap FFE provides 6dB SNR margin
- 12-tap FFE has +1dB margin to the required 3dB SNR margin
- These SNR curves further prove that after 4th 8-tap Echo Canceller segment, there is hardly any more SNR improvement.
- 53Gbaud SD SNR, even with 32-tap FFE, has -2dB to the required 3dB margin

26.5Gbaud DD SNR with Different FFE/Echo Filters Over 2.5m WC Channel



- All cases use 1-tap DFE
- Even over WC channel with extra 10dB sNEXT, 26.5Gbaud DD link can provide enough SNR margin with 16 to 24 taps (e.g. 20 taps) FFE and same size Echo filter
- 53Gbaud SD link ends up with completely negative SNR margin over this WC channel even with much more complex FFE/DFE



Line Card BGA
Break Out Region (BOR)
14 layer 093 mil thick

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100Gbps AFE/Clocking Power for 2.5m Passive DAC

2x AFE at 26.5Gbaud PAM4 for 100Gbps Passive DAC DD PHY

- 7-bit ADCs = 200mW
  - 2x ADC= 2 x 100mW
- PGAs & CTLEs = 70mW
  - 2x PGE/CTLE = 2 x 35mW
- 6-bit DACs = 70mW
  - 2x DAC= 2 x 35mW
- PreDrivers/Drivers = 90mW
  - 2x PreDriver/Driver (1V_{pp})= 2 x 45mW
- Hybrid Echo Canceller = 80mW
  - 2x Hybrid Echo Canceller = 2 x 40mW

➔ 100Gbps DD-PHY AFE (2.5m)= ~510mW*

farjadrad_100GEL_01a_0318 → Power (100G SD AFE) = Power (100G DD AFE) + ~100mW

*Clocking/CDR power not included, as it is very similar for 100Gbps DD and SD PHY

100Gbps DSP Power for 2.5m Passive DAC

2x DSP at 26.5Gbaud PAM4 for a 100Gbps Transceiver

- Assumptions:
  - FIR Power: 0.04mW/tap/Gbaud/data_res
  - Crosstalk: (Mellitz 2.5m)
    - 3 sNEXT + 3 FEXT + 4 aNEXT
  - Equalization:
    - 1-Tap DFE
    - 12-Tap FFE
  - Echo Cancellation
    - Four 8-Tap Canceller Segments

- DSP Power Calculations*:

→DFE Power = 20mW
  - 1-Tap DFE=10mW→Total DFE= 2x10mW= 20mW

→FFE Power = 180mW
  - 12 Taps→ 0.04*12tap*7bit*26.5Gbaud=~90mW
  - Two Channels→ Total FFE=2 x 120mW=~180mW

→Echo Canceller power = 132mW
  - 4 x 8 Taps→0.04*32tap*2bit*26.5Gbaud=~66mW
  - Two Channels→ Total Echo= 2 x 66mW=~132mW

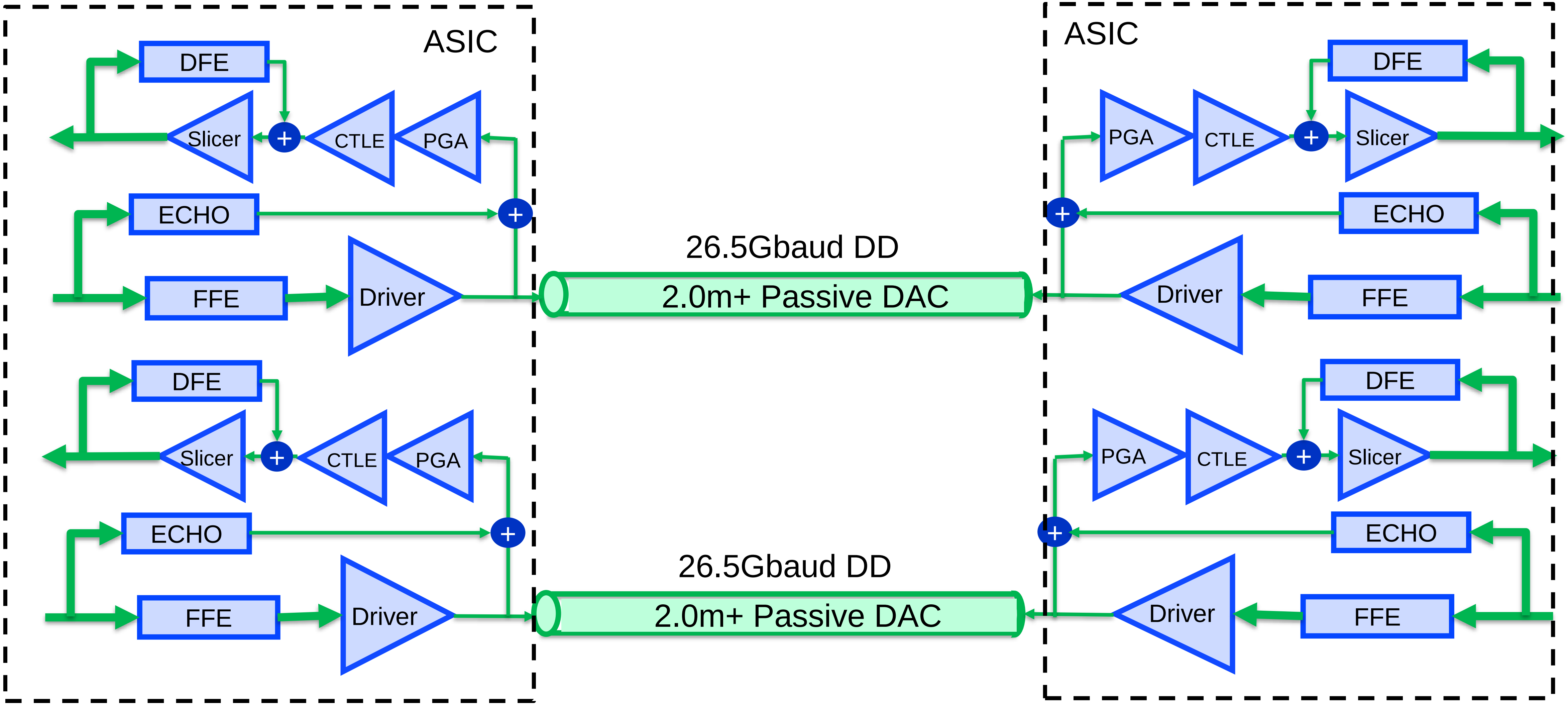
→100Gbps DD DSP Power= ~332mW

- Power (100Gbps SD-PHY DSP) = Power (32-tap FFE @53Gbaud) = ~480mW

→ Even at ~150mW higher DSP power, 100G SD fails to meet the SNR margin for 2.0m BC channel!

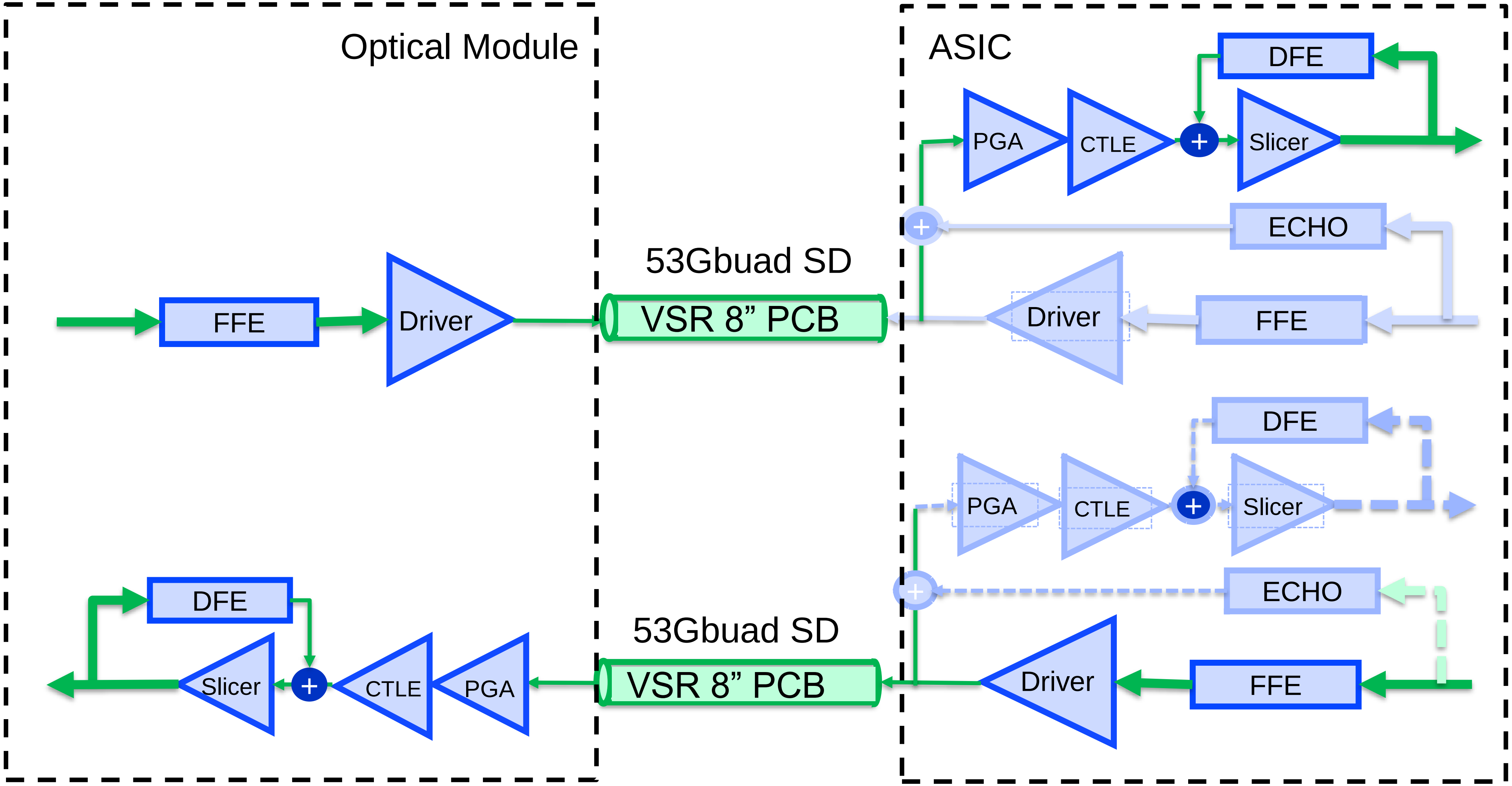
* Assuming BC channel & 7nm process node

A DD-PHY Can Support Both DD & SD Operation Modes



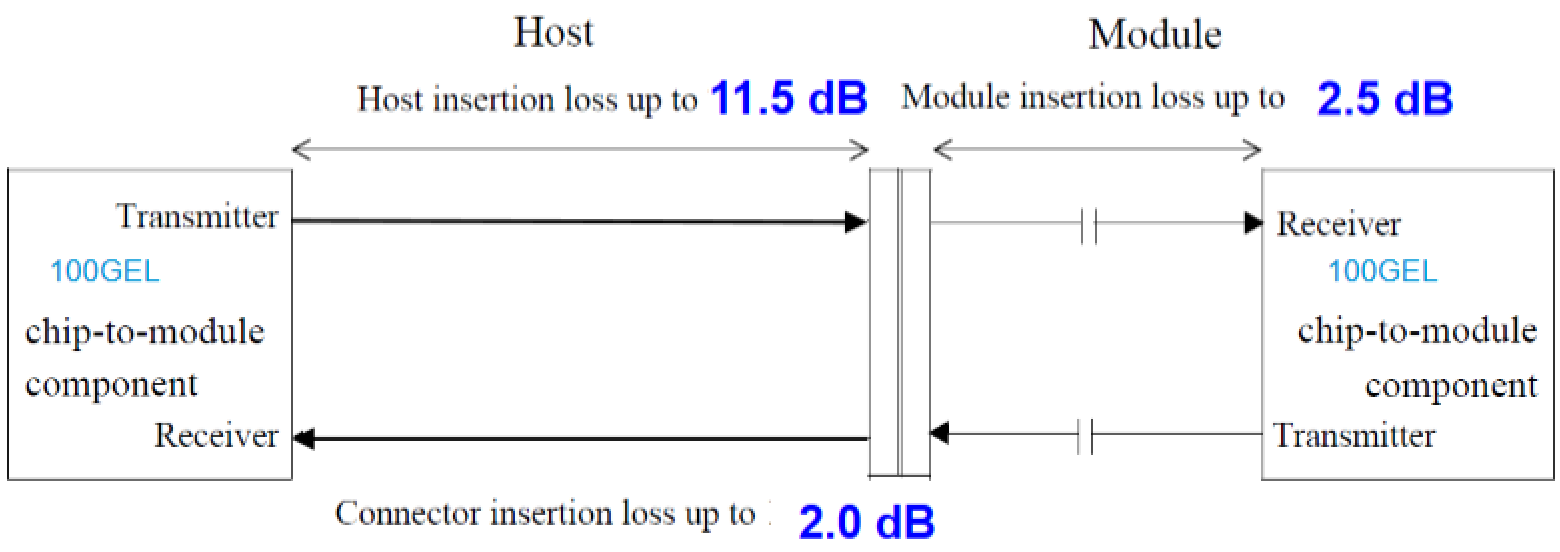
- 2.0m+ Passive Cable→ 26.5Gbaud Dual-Duplex mode on both sides of cable

A DD-PHY Can Support Both DD & SD Operation Modes



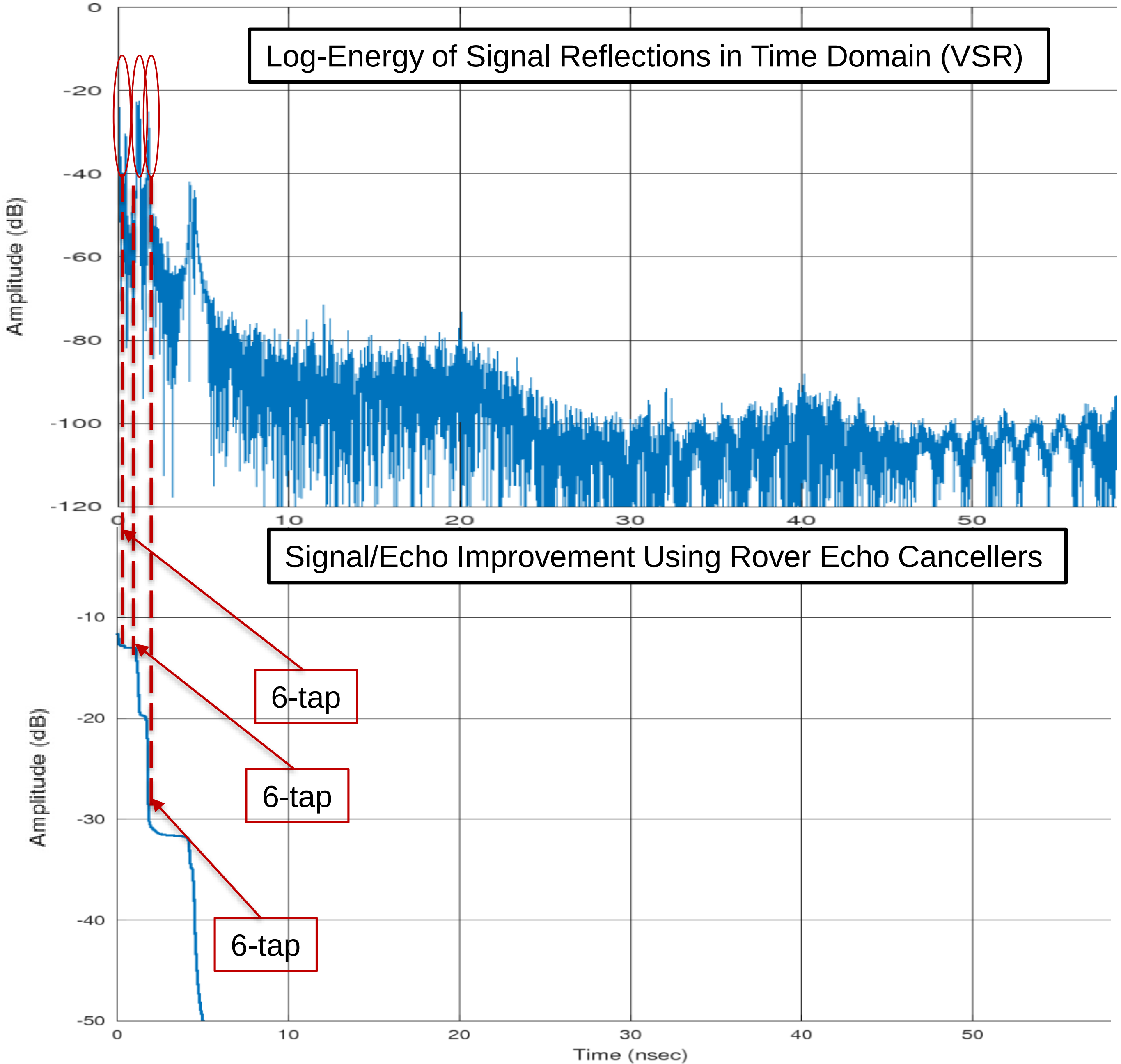
- Chip-Module/AUI → Switch ASIC PHY to 53Gbaud Single-Duplex mode and Module PHY stays as a VSR 53Gbuad Single-Duplex PHY

Selected Chip-Module/AUI Channel (8” PCB)



- Channel model used is the proposed channel in lim_3ck_01b_0718
  - VSR channel with IL=16dB @26.5GHz

Echo Impairment for 26.5Gbaud PAM4-DD Mode (8” PCB)



- To achieve DER<1E-6, the total link SNR including all impairments must be >20.6dB
- A total of three 6-tap* Rover Echo Cancellers considerably improve the Signal/Echo (S/E) ratio for Lin 16dB VSR channel:
  - No Echo Canceller→ S/E=~11dB
  - 3x Echo Cancellers→ S/E=~32dB
- S/E= 32dB is significantly below the required SNR=20.6dB to degrade the link performance

*Each 6-tap canceller covers 20mm of channel

100Gbps AFE/Clocking Power for 16dB@26.5GHz VSR Channel*

2x AFE at 26.5Gbaud PAM4 for 100Gbps VSR DD PHY

- PAM4 Slicers= 30mW
  - 2x Slicers= 2 x 15mW
- CTLEs = 40mW
  - 2x CTLE = 2 x 20mW
- PAM4 Drivers = 60mW
  - 2x PAM4 Driver (0.8V_{pp})= 2 x 30mW
- Hybrid Echo Canceller = 50mW
  - 2x Hybrid Echo Canceller = 2 x 25mW

→ 100Gbps DD AFE (VSR)= ~180mW

* VSR 16dB channel as presented in → lim_3ck_01b_0718

100Gbps DSP Power for 16dB@26.5GHz VSR Channel*

2x DSP at 26.5Gbaud PAM4 for 100Gbps VSR DD-PHY

- Assumptions:
  - FIR Power: 0.04mW/tap/Gbaud/data_res
  - Crosstalk:
    - 3 FEXT+4 aNEXT & 3 sNEXT (Mellitz)
  - Equalization:
    - CTLE
    - 4-Tap FFE (Tx)
  - Echo Cancellation
    - Two 8-Tap Canceller Segments

- DSP Power Calculations:

➔FFE Power = ~16mW
  - 4 Taps→ 0.04*12tap*2bit*26.5Gbaud=~8mW
  - Two Channels→ Total FFE=2 x 8mW=~16mW

➔Echo Canceller power = ~72mW
  - 3 x 6 Taps→0.04*18tap*2bit*26.5Gbaud=~38mW
  - Two Channels→ Total Echo= 2 x 32mW=~72mW

➔100Gbps DD DSP Power= ~88mW

→ VSR DD-PHY Power (AFE + DSP) = ~270mW

* VSR 16dB channel as presented in → lim_3ck_01b_0718

Conclusion

- A DD-PHY makes 100Gbps/Lane over 2.5m+ passive cables a practical reality
  - 26.5Gbaud PAM4 signaling is same as in 50GBASE-CR
    - Operates over existing 50G systems & eliminates the need for new costly channels
    - Same Mux/Demux Datapath and FEC/PCS as 50GBASE-CR2 can be used
  - Dual-duplex architecture does not lead to higher power than SD architecture
    - Echo canceller operates on 2-bit input data & needed at the connector locations
    - Equalizer + Echo Canceller power in DD-PHY < Equalizer power in SD-PHY
  - A DD-PHY can be configured to provide both modes of DD and SD
    - DD (@26.5Gbaud) for Chip-Chip over 2m+ Passive Cables
    - SD (@53Gbaud) for VSR Chip-Module over 8" PCB
- A VSR DD-PHY can also deliver 100Gbps over at least ~8" PCB at < 400mW
  - VSR DD-PHY Power (AFE+DSP) = ~270mW

Thank you.

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