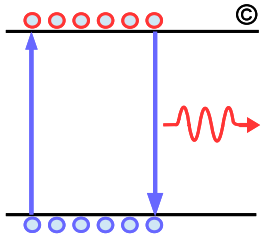


Methodology and Architectural Considerations for C2M

Ali Ghiasi

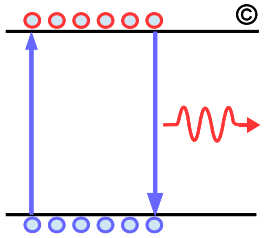
Ghiasi Quantum LLC

IEEE 802.3ck Task Force Meeting

Spokane

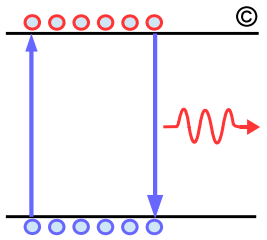
Sept 14, 2018

Background

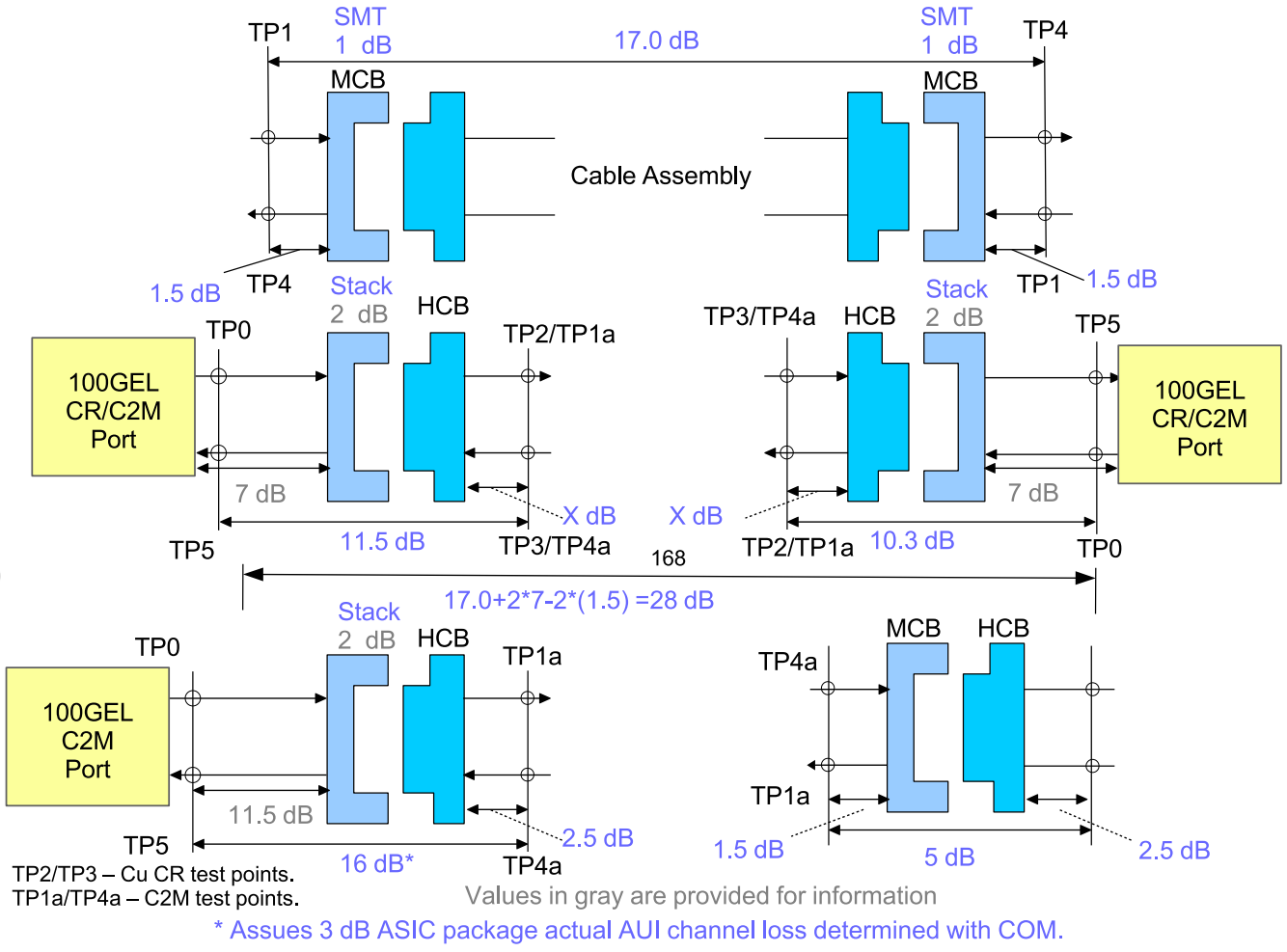


- **During July plenary meeting lim_3ck_01b_0718.pdf and ghiasi_3ck_01a_0718.pdf investigated C2M and Cu MDI applications**
  - C2M application in support of high density linecards require up to 16 dB channel loss
  - Cu MDI ports loss must be limited to 11.5 dB in order to support 2 m Cu cable
- **During July plenary sakai_3ck_01_0718.pdf provided lack of correlation between channel loss and EH/EW and suggested using COM as informative tool**
  - In spoken Ghiasi_3ck_02_0918 results further enforces lack of correlation between channel loss and COM, where a 10 dB channel fails but 16 dB channels passes
- **The C2M application is growing in dimension and complexity with the range of connectors [1 to 8 lanes] and package sizes [6 to 32 mm] that must be supported**
- **Back channel training has been proposed for C2M in sun_3ck_adhoc_01_082918.pdf which dramatically increases complexity of C2M applications and may not save power!**

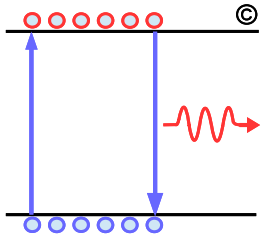
Overview of Symmetric Dual-Port Types



- **Symmetric dual-port type allow building a superset port supporting passive Cu cable and optical port/AOC or build an optical/AOC/Active Cu ports if passive Cu cable support not required**
- **As the figure illustrate the normative compliance points TP2/TP3 and TP1a/TP4a can support multiple MDIs and each of the MDIs may have distinct MCB/HCBs**
- **As sakai_3ck_01_0718.pdf and Ghiasi_3ck_01_0918 indicate C2M channel impairments are dominated by other than insertion loss**
  - A well constructed 16 dB C2M channel can operate with margin with just 4 TX FFE taps and RX with CTLE+5 taps FFE (no-precursors) but in case of high crosstalk channels even 10 dB may work
  - To support high crosstalk channels longer FFE as proposed by Sun may not be sufficient, better option is an RX with 5T FFE+1T DFE
  - However adding DFE likely outside our power envelop
  - Better option is to use COM on mated board+traces to determine max trace loss such that COM/VEC/EH are not violated without resorting to DFE.



Current C2M CL120E Specifications



- **The normative TP1a/TP4a EW/EH historically measured with reference EQ on the scope**
  - Clause 120E defines C2M loss *up to 10.2 dB*
- **In practice any host/SerDes that deliver the TP1a EW/EH is compliant to the specifications, then why use COM?**
  - Clause 83E and 120E simulations were based on QSFP28 mated boards then we assumed the lower crosstalk SFP28 also works
  - AUI Specifications provides recommended insertion loss and the normative output differential/common-differential mode conversion return losses
  - If an implementer followed guideline below there is reasonable confidante EW/EH would be met for a compliant chip.

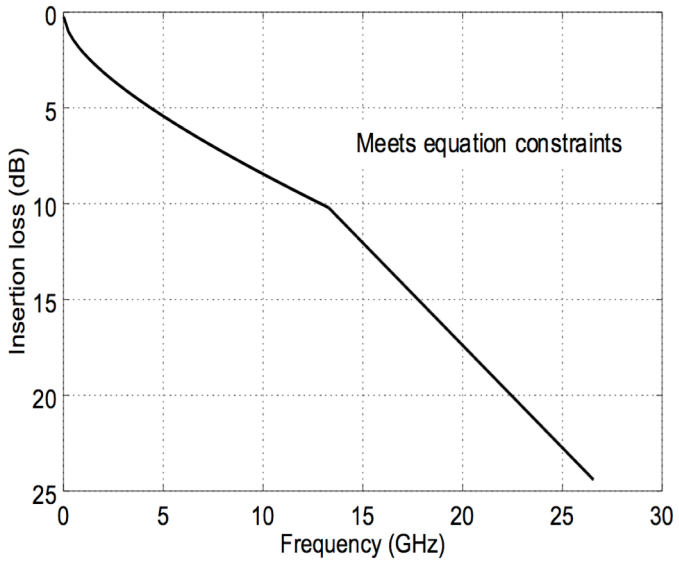


Figure 120E–4—Recommended 200GAUI-4 or 400GAUI-8 chip-to-module channel insertion loss

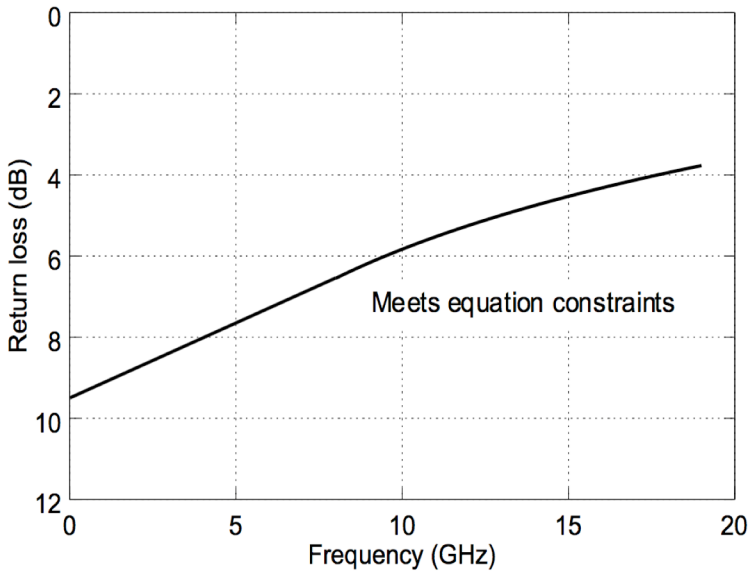


Figure 83E–7—Output differential return loss

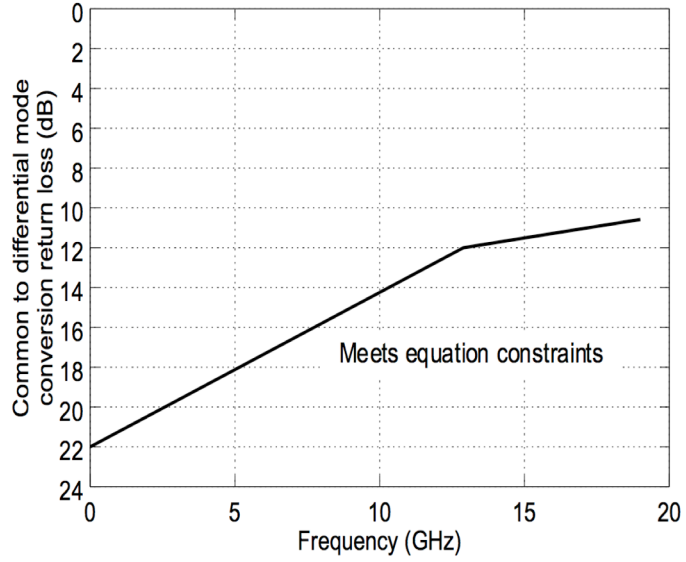
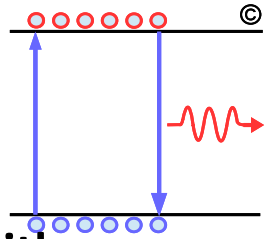


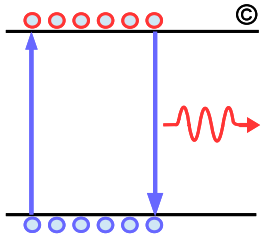
Figure 83E–8—Output common to differential mode conversion return loss

The expected connectors that must be supported

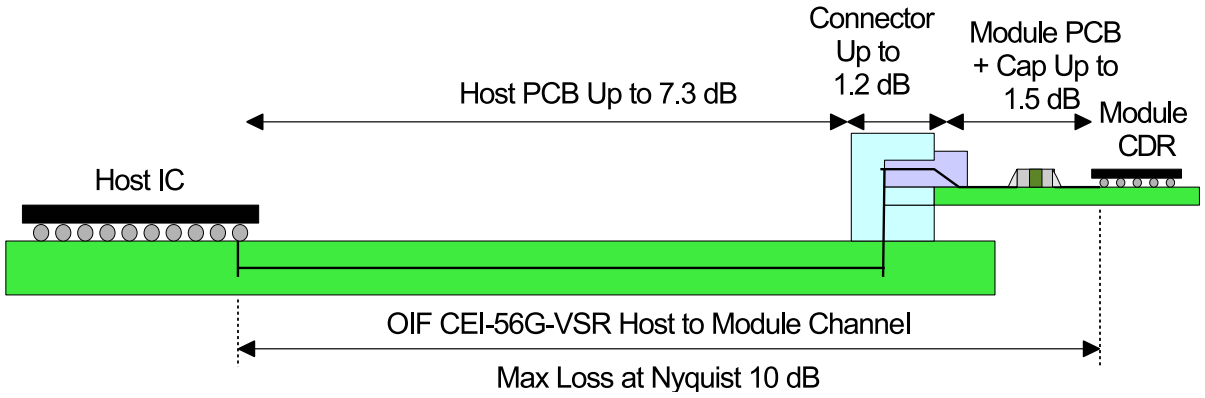


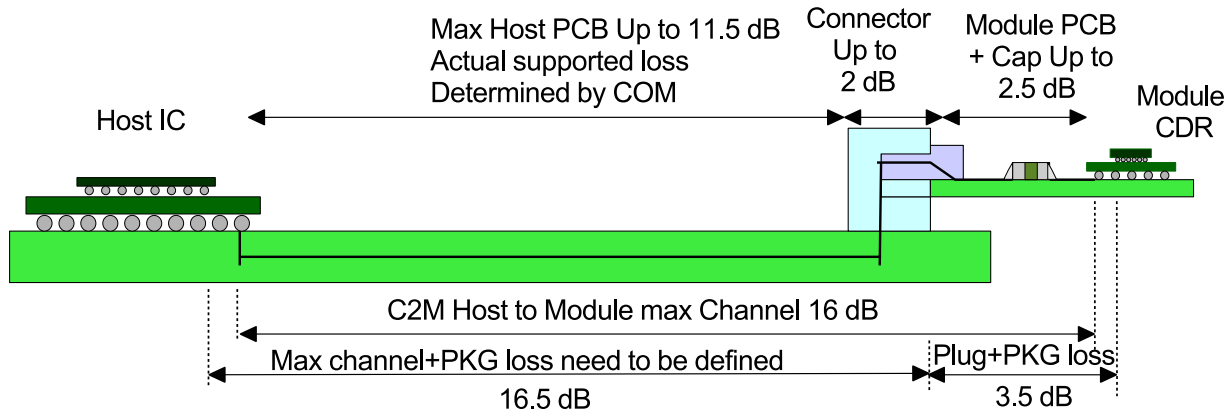
- **Historically QSFP28 connectors were used for 28G-VSR/56G-VSR simulations to arrive with a degree of confidence the recommended channel loss**
- **The connector and channel 112G-VSR expected to support are:**
  - SFP112 1 lane
  - SFP-dd 2 lanes http://sfp-dd.com
  - DSFP 2 lanes https://www.dsfpmsa.org
  - QSFP112 4 lane
  - μQSFP 4 lanes http://www.microqsfp.com
  - QSFP-dd 8 lanes http://www.qsfp-dd.com
  - OSFP 8 lanes http://osfpmsa.org
- **The crosstalk, ILD, return loss of the above 7 connectors could be very different where the recommended channel could be <10 dB or even >16 dB**
- **For a reasonable-low power equalizer no longer we can define one recommended channel loss, our options are:**
  - Define a set of rigid masks such as ICR, ILD, and return loss which will penalize some working channels
  - Use COM for channel compliance.

Using COM for C2M Compliance

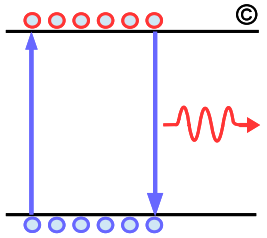


- **At 112G crosstalk, ILD, and return losses are the dominant impairments**
  - Arriving at a simplified loss vs ILD/PSXT/RL would be multi-dimensional and complex
- **COM already utilized for 56G-MR/LR can be used for C2M to determine recommended channel based on**
  - Connector PSXT, ILD, return loss, and package loss
  - Informative Max bump-bump loss 20 dB excluding capacitive effects
  - Host PKG IC/channel informative losses can be traded off with max loss of 17.5 dB
  - Plug PCB and module CDR PKG informative loss can be traded off with max loss of 3.5 dB
  - For specific connector mated board (QSFP, QSFP-dd, OSFP, etc) the max channel loss supported is determined by increasing host PCB traces in COM without violating COM/VEC/EH limits and staying with above guideline.





Example of Low Power FFE Suitable for 100G AUI



- **Momtaz analog FFE implementation is a 40 GBd 7-Tap T/2 FFE with 2 pre-cursor and a power of just 80 mW in 65 nm CMOS based on clever design of using transconductance amplifier instead of delay line**
  - The implementation uses an innovative passive-active delay element which are process invariant
  - Baseline FFE for 100GEL is 5 taps T-Spaced with no pre-cursors
  - Momtaz FFE with 20 GHz BW would not need to increase the BW by more than 30%
  - The delay T can be increased from 12.5 ps to 18.8 ps by adjusting transconductance amplifier
  - With 16 nm process fast enough most of the inductors would be elimianted
  - The estimated above circuit in 16 nm CMOS would be ~40 mW
- **The estimated 7 Tap FFE with 2 pre-cursor to support PAM4 in 16 nm CMOS would be about 60 mW.**

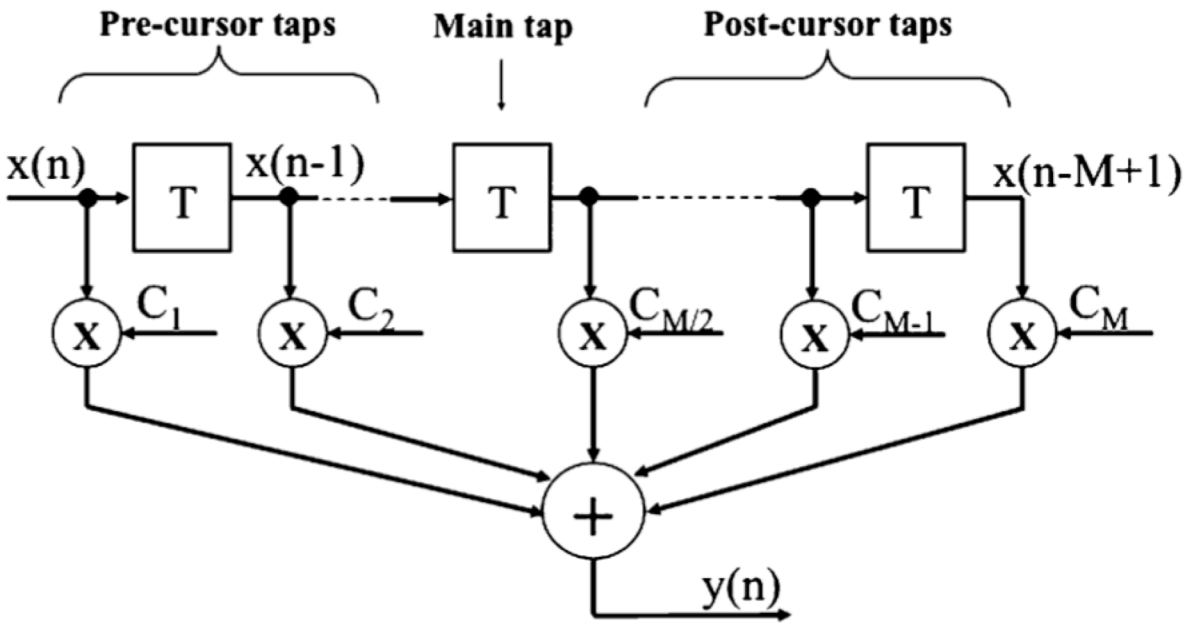
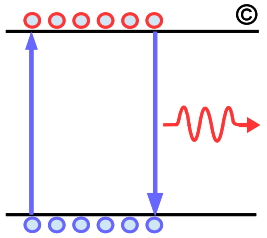


Fig. 1. M-tap FFE block diagram.

Afhsin Momtaz, An 80 mW 40 Gb/s 7-Tap *T*/2-Spaced Feed-Forward Equalizer in 65 nm CMOS IEEE Journal of Solid-State Circuit, Vol. 45, No. 3, march 2010.

Adding Analog Low Power FFE EQ to sun_3ck_adhoc_01_082918

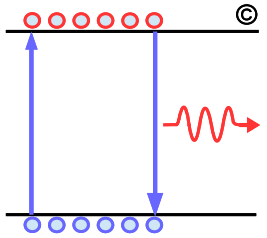
- Power for non-DAC TX implementation should be based on conventional current summing implementation [5*] instead of scaling down higher power DAC implementations
- Asymmetric balanced EQ also need to include Mux/De-mux and LT/PCS related logic power including additional latency.



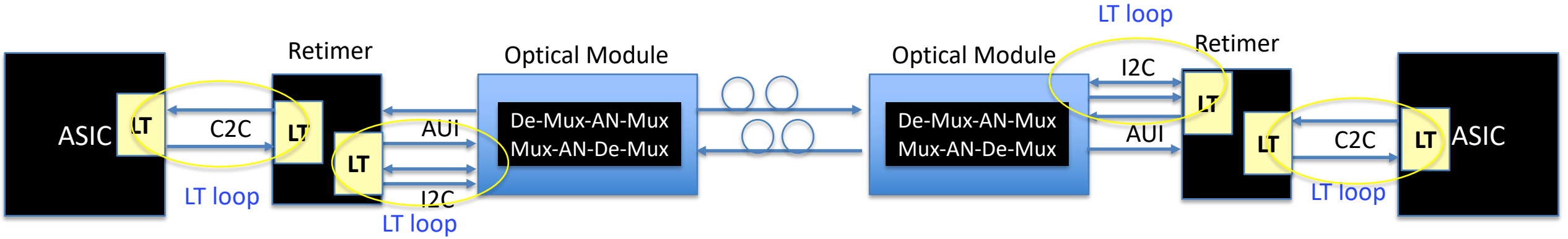
Architecture	Balanced EQ (1. Asymmetric, 2. symmetric)*	3. Direct Feedback**	4. ADC Based	5. Analog FFE (Momtaz)
Equalization	TX: FIR (2/4 taps for asymmetric structure, 2/11 taps for symmetric structure) RX: CTLE	TX: FIR (2/4) RX: CTLE, 8-tap direct-feedback DFE	TX: FIR (2/4) RX: CTLE, 6-bit ADC, 8 postcursor digital FFE	TX: FIR(2/4) RX:CTLE, Analog 5-7 tap FFE
TX Power (mW)	~~247~~ (asymmetric structure) *157mW 277 (symmetric structure) (by scaling TX FIR of [7])	~~247~~ *157mW (by scaling TX FIR of [7] to 4 taps)	~~247~~ *157mW (by scaling TX FIR of [7] to 4 taps)	157 mW (by scaling TX of [5] from 64 Gb/s to 112 Gb/s)
RX Power (mW)	220 (by scaling [6] to 112G)	460 (by scaling [3] to 112G, 2 DFE tail tap power is very low)	763 (568 by scaling [5] to 112G; 115 for FFE by scaling FIR of [7] for 6b input; 80 for PLL, deserializer and CDR)	220 mW (by scaling [6] to 112G) +60 mW for 7 T FFE Total RX Power=280 mW
Relative total Power (mW)	**0** (467 as Baseline for asymmetric) **30** (497 for symmetric)	**240** (total 707)	**543** (total 1010)	-90 mW (total power 437 mW)
Power Difference for 800G Module C2M (mW)	**0** (Total 3736)	**1,920** (Total **5656**)	**4,344** (Total **8080**)	-720 mW (total 3496)

For list of Sun reference please see http://www.ieee802.org/3/ck/public/adhoc/aug29_18/sun_3ck_adhoc_01_082918.pdf.

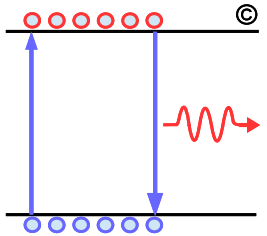
Complexity of adding Link Training (LT) to CMIS



- **As previous slide showed a balanced approach for C2M based on analog FFE could have lower power and without additional complexity associated with asymmetric balanced approach requiring back channel LT adaptation**
  - LT on the backplane or CR are point-point with DME exchange
  - C2M links are segmented, each end of the link would require LT through slow-unpredictable module I2C
  - 4 segmented link with 8 LT engine need to work seamlessly as shown in diagram below just to to bring up an optical link
  - LT operational stability/Interop are performed today by small number of system OEMs
  - A module CDR implementing backchannel LT would require full Mux/De-mux with AN/PCS logic ruling out serial CDR implementations and non-CMOS implementations
  - An optical module with back channel LT will be significantly more complex to qualify, mange, and diagnose
  - Given that the interface is pluggable with potentially 4 cascaded LTs that will increase further the difficulty to bringing up the link!



Summary



- **Dual port symmetric offers practical solution to support C2M and CRx applications**
  - The proposed C2M budget can support up to 16 dB with 3 dB package consistent with lim_3ck_01b_0718.pdf
  - TX based on 4 Taps FFE with RX having CTLE+5 taps FFE offers attractive module PMA power
- **802.3ck is defining PMDs for a diverse set of connectors: SFP112, SFP-dd, DSFP, QSFP112, µQSFP, QSFP-dd, and OSFP**
  - No longer we have the luxury of extra margin to have one shoe fit all approach, given the diverse set of connector ILD, ICN/ICR, return loss, and channel loss need to be traded-off
  - One option is to define a set of complex limits for ICN/ICR, return loss, ILD, and channel
  - A better option is use let COM do the complex trade off based on channel output limits of COM/VEC/EH
- **Propose balanced asymmetric implementation using long TX FFE with back channel dramatically increases link complexity and interop**
  - The proposed balanced asymmetric scheme not only is more complex but actually would not be lower power and require full mux/de-mux with AN/PCS implemented in the module PMA
  - Analog RX FFE implementation with ≤ 7 taps offers lower power, lower latency, without requiring full mux/de-mux and AN/PCS, and without subtle host-module dependencies
  - Proposed balanced asymmetric proposal does not address high crosstalk channels as a DFE could do.