Ethernet 100 Gb/s Per Lane VSR Studies: Typical TX FFE + RX CTLE/FFE vs. Longer TX FFE + RX CTLE

For IEEE 802.3ck

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Intel

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- Device and Link Configuration
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Objective

- This study intents to conduct independent simulation/modeling under similar conditions and channels (only publically available ones) of healey_3ck_01b_0718, and to achieve better understanding of the problem under study.

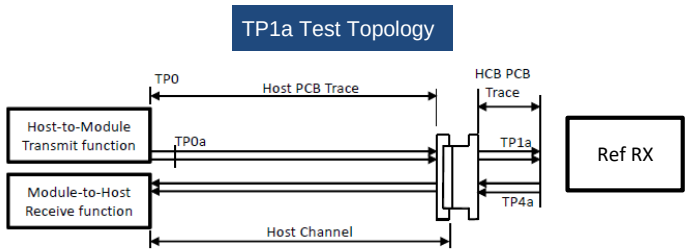
100 Gb/s VSR Link Simulations

Link & Device Configurations

- **Data Rate: 106.25 Gbps, PAM-4**
- **Test Pattern:**
  - QPRBS13-CEI: TP1a simulations
- **TX Die**
    - VOD: 800 mV-pp
    - 20%-80% Rise/Fall Time: 6 ps
    - TX FIR:
      - Configuration 1
        - » 4 taps, 2 pre-taps and 1 post-tap
      - Configuration 2
        - » 7 taps: 2 pre-taps and 4 post-taps
      - Range: Pre-tap 1 and post-tap 1: 0 to -0.20
        other taps: +/- 0.1
      - Step size: 0.02
      - RLM (level mismatch): 0.95
      - TX termination: 55 ohms
      - TX Capacitance: 100 fF (RL~=8dB @ Die)
      - Jitter:
        - BUJ: 0.04 UI-pp, DCD: 0.019 UI-pp, RJ: 0.01 UI-rms
      - Noise:
        - RN: ~9mV-rms (TX SNR=33dB) @ TP0

TX Package

- Package model (Typ., IL ≈ 3.15 dB @ 28 GHz)
- Package crosstalk is < -60 dB (by design)



100 Gb/s VSR Link Simulation

Link & Device Configuration *(cont.)*

TP1a Reference RX

- Die Termination: 50 ohms
- Capacitance: 0 fF
- AFE Filter and CTLE
  - Parameter scaled from IEEE 802.3cd ref. CTLE

$$H_r(f) = \frac{1}{1-3.414214\cdot\left(\frac{f}{f_r}\right)^2+\left(\frac{f}{f_r}\right)^4+j\cdot 2.613126\cdot\left(\frac{f}{f_r}-\left(\frac{f}{f_r}\right)^3\right)}$$

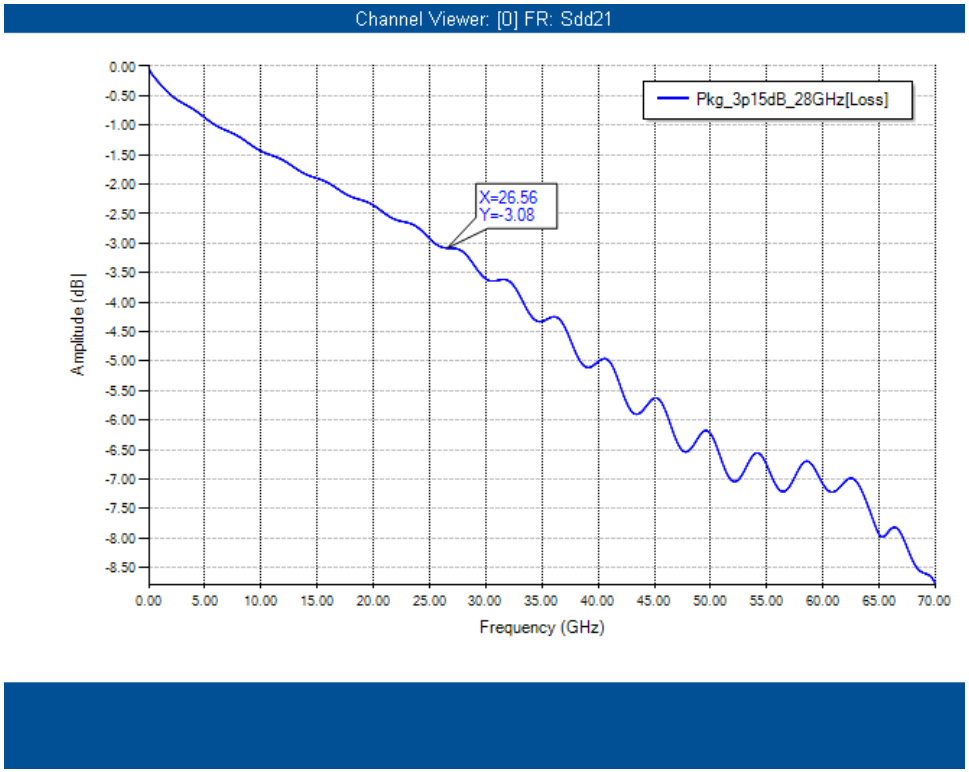
$$H_{CTF}(f)=G\cdot\frac{\left(10^{\frac{g_{dc2}}{20}}+j\frac{f}{f_{z2}}\right)}{\left(1+j\frac{f}{f_{zp}}\right)}\cdot\frac{\left(10^{\frac{g_{dc}}{20}}+j\frac{f}{f_{z1}}\right)}{\left(1+j\frac{f}{f_{p1}}\right)\left(1+j\frac{f}{f_{p2}}\right)}$$

  - Baud: 56 Gsym/s
  - fp1 / fp2 / fz1 / fz2 / fzp = Baud ÷ 2.5 / 1.0 / 2.5 / 80 / 80
  - g_{DC}: 0 to -15 dB
  - g_{DC2}: 0 to -4 dB
  - G: 1.0 (constant)
- FFE:
  - Configuration 1
    - 5 Taps: 4 post-taps
  - Configuration 2
    - No FFE
  - Range: First 2 post-cursors: +/-0.2 others: +/-0.1
  - Step size: 0.02
- CDR
  - Optimal phase based EH and PAM symbol SNDR
- Noise:
  - Input noise: 8.2e-9 V^2/GHz (~-157.85 dBm/Hz)
- Jitter: None

RX Package: None

Equalization Optimization: SNDR maximization

100 Gb/s Package Model

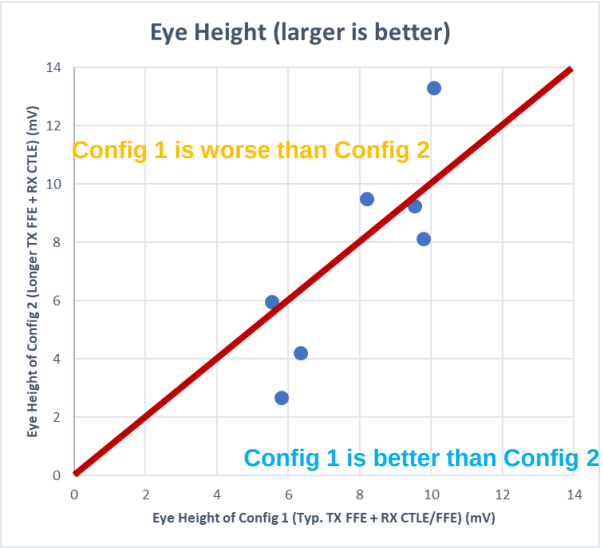


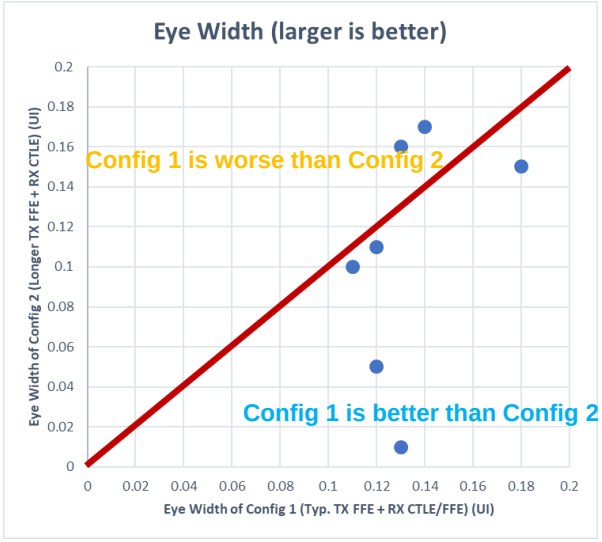
Test Channel Summary

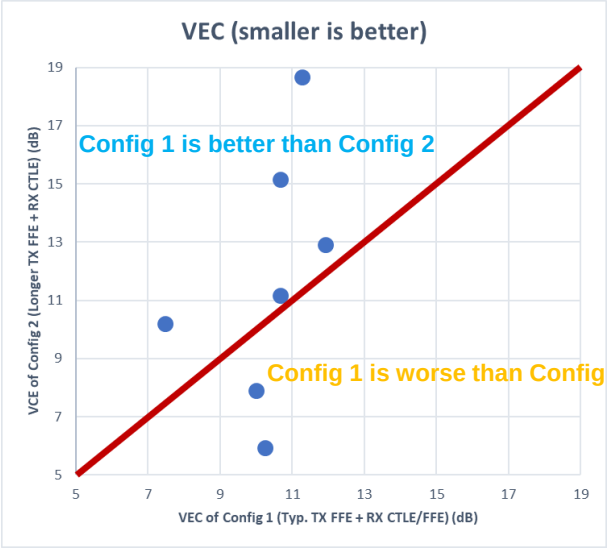
Channel	Description	Insertion Loss (dB) @ 26.56 GHz	ICN (mV-rms)*
CH1	Lim_100GEL_C2M 10dB + Tx Pkg	10.02 + TX Pkg	3.26
CH2	Lim_100GEL_C2M 12dB + Tx Pkg	12.11 + TX Pkg	2.88
CH3	Lim_100GEL_C2M 14dB + Tx Pkg	13.95 + TX Pkg	2,61
CH4	Tracy_100GEL_06_0118 RX6 + Tx Pkg	14.58 + TX Pkg	1.03
CH5	Tracy_100GEL_06_0118 RX5 + Tx Pkg	14.56 + TX Pkg	1.13
CH6	Tracy_100GEL_02_0118 TX6 + Tx Pkg	16.09 +TX Pkg	1.10
CH7	Tracy_100GEL_02_0118 TX5 + Tx Pkg	16.45 + TX Pkg	1.12

**: Channel files' fmax is less than fbaud. ICN results are informative.*

Simulation Results Summary







Channel	Description	Insertion Loss (dB) @ 26.56 GHz	Simulation Results @ BER = 1e-5					
			Configure 1: Typical TX FFE + RX CTLE/FFE			Configure 2: Longer TX FFE + RX CTLE		
			EH (mV)	EW (UI)	VEC (dB)	EH (mV)	EW (UI)	VEC (dB)
CH1	Lim_100GEL_C2M 10dB	10.02 + TX Pkg	10.09	0.13	10.26	13.29	0.16	5.93
CH2	Lim_100GEL_C2M 12dB	12.11 + TX Pkg	9.55	0.12	10.69	9.25	0.11	11.15
CH3	Lim_100GEL_C2M 14dB	13.95 + TX Pkg	5.54	0.11	11.94	5.96	0.10	12.89
CH4	Tracy_100GEL_06_0118 RX6	14.58 + TX Pkg	8.21	0.14	10.01	9.49	0.17	7.88
CH5	Tracy_100GEL_06_0118 RX5	14.56 + TX Pkg	9.8	0.18	7.49	8.11	0.15	10.19
CH6	Tracy_100GEL_02_0118 TX6	16.09 +TX Pkg	6.35	0.12	10.67	4.2	0.05	15.14
CH7	Tracy_100GEL_02_0118 TX5	16.45 + TX Pkg	5.81	0.13	11.28	2.67	0.01	18.67
Variation Range (max – min)			4.55	0.07	4.45	10.62	0.16	12.74

- *Notes 1. VEC Threshold (max): 12dB 2. Better Worse*

Summary and Conclusion

- Config 1 outperforms Config 2 (5 channels out of 7 for EW and VEC, and 4 channels out of 7 for EH)
- Config 1 VEC variation among 7 channels is much smaller than Config 2 (4.5dB vs. 12.7dB)
  - Large variation range implies worse robustness

Thoughts and Reasoning

- Rely on TX FFE solely will more likely decrease signal amplitude (*due to TX peak power constraint*) at the receiver input which affects final SNR at slicer
  - *Note that our TP1a simulations have small receiver input noise. With presence of more RX noises, RX FFE will outperform TX FFE*
- Config. 1 offers longer effective tap length (8 taps) when combining/convolving TX FFE (2+1+1) and RX FFE (0+1+4), than Config. 2 with TX FFE only (2+1+4) (7 taps)