

112 Gbp COM Investigations for Backplane with a 20 mm Reference Package Addition

For IEEE 802.3ck

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Intel

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- Proposed 112Gbps LR COM
- 20mm Package
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- Summary

Proposed 112Gbps LR COM

- Baseline
 - 802.3cd COM
 - http://www.ieee802.org/3/cd/public/adhoc/archive/mellitz_080217_3cd_01_adhoc.pdf
 - http://www.ieee802.org/3/cd/public/adhoc/archive/mellitz_3cd_0817_COM.zip
- Change Summary
 - TX
 - Scale: TX rise/fall time (T_r), jitter (A_{DD} , σ_{RJ})
 - Same: TX EQ (2 pre- + 1 post-taps), RLM, noise (SNR_{TX})
 - Pre-tap1 and post-tap1 min. = -0.3
 - RX
 - RX input referred noise (η_0): $8.2e-9$ V²/GHz
 - Equalization
 - CTLE
 - » Scale f_z , f_{p1} , f_{p2}
 - $f_{p2} = 56$ GHz (= baud rate)*
 - » F_{HP_PZ} : 0.7 GHz (= $f_b / 80$)
- Support long FFE + short DFE architecture
 - FFE Configuration
 - 3 pre- and 12-post cursor taps
 - Main cursor: 1
 - Pre-tap 1 coef: ≤ 0.5
 - Post-tap 1 coef.: ≤ 0.5
 - Other taps: ≤ 0.125
 - DFE Configuration
 - 1 post-tap
 - DFE tap coef. ≤ 0.7
- Package / TX/RX Capacitance and Termination
 - Length: max 20 or 30mm
 - TL: No change
 - Cd: 130fF
 - Cp: 110fF
 - Rd: 50 Ohms

**: In 802.3cd COM, f_{p2} is 2x baud rate (112GHz) which We believe it might be too high for today's CMOS technology. Further, f_r (RX noise filter) is set at 0.75x baud rate which will reduce the effectiveness of higher f_{p2} .*

Proposed 112Gbps LR COM Spreadsheet

Table 93A-1 parameters

Parameter	Setting	Units	Information
f_b	56	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.3e-4 1.3e-4]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[12 20 30]	mm	[test cases]
z_p (NEXT)	[12 20 30]	mm	[test cases]
z_p (FEXT)	[12 20 30]	mm	[test cases]
z_p (RX)	[12 20 30]	mm	[test cases]
C_p	[1.1e-4 1.1e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX] or selected
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.025:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		[min:step:max]
c(1)	[-0.3:0.025:0]		[min:step:max]
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	22.4	GHz	
f_p1	22.4	GHz	
f_p2	56	GHz	
A_v	0.41	V	tdr selected
A_fe	0.41	V	tdr selected
A_ne	0.6	V	tdr selected
L	4		
M	32		
N_b	1	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
sigma_RJ	0.01	UI	
A_DD	0.02	UI	
eta_0	8.20E-09	V ² /GHz	
SNR_TX	32.5	dB	tdr selected
R_LM	0.95		
DER_0	1.00E-04		
Operational control			
COM Pass threshold	3	dB	
Include PCB	0	Value	0, 1, 2

g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.7	GHz	

I/O control

DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
Display frequency domain	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\D1p2_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	v165_d1p0a	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
IDEAL_TX_TERM	0	logical
T_r	0.006160714	ns
FORCE_TR	1	logical

Table 93A-3 parameters

Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	90	Ohm (tdr sel)

Table 92-12 parameters

Parameter	Setting	Units
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	110	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

Red: New or modified entries

RX FFE

ffe enable	1	logical
ffe_pre_tap_len	3	
ffe_post_tap_len	12	
ffe_tap_step_size	0	
ffe_main_cursor_min	1	
ffe_pre_tap1_max	0.5	
ffe_post_tap1_max	0.5	
ffe_tapn_max	0.125	

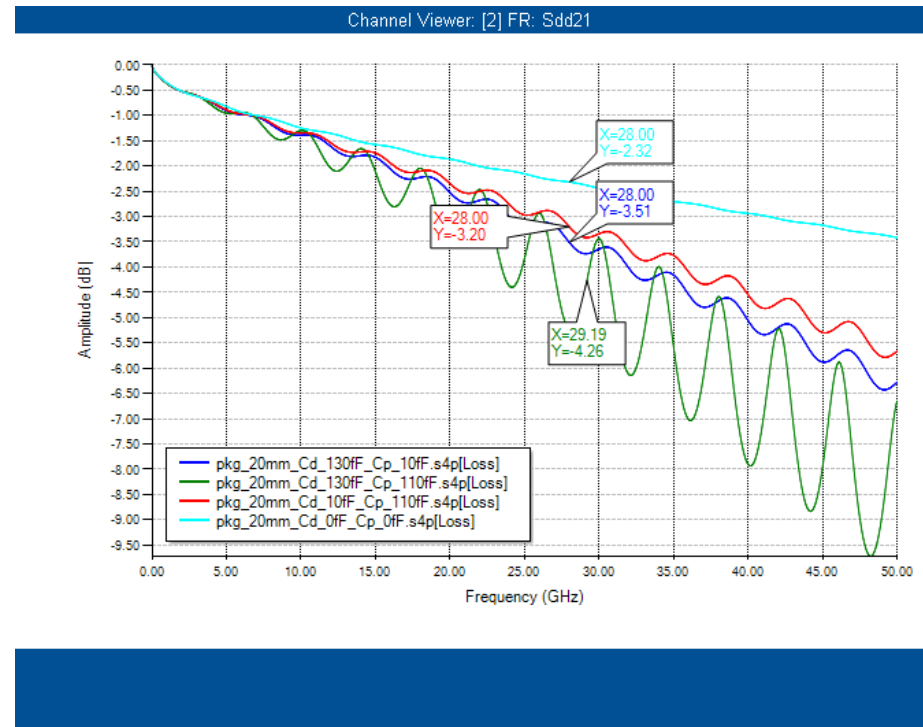
112Gbps 20mm COM Package Model

- Modified from 802.3cd COM package model

- Length: 20mm
- TL: No change
 - Zc: 90 ohms
- Cd: **130 fF** (Changed from 802.3cd)
- Cp: 110 fF
- Rd: 50 Ohms

- Insertion loss @ 28GHz

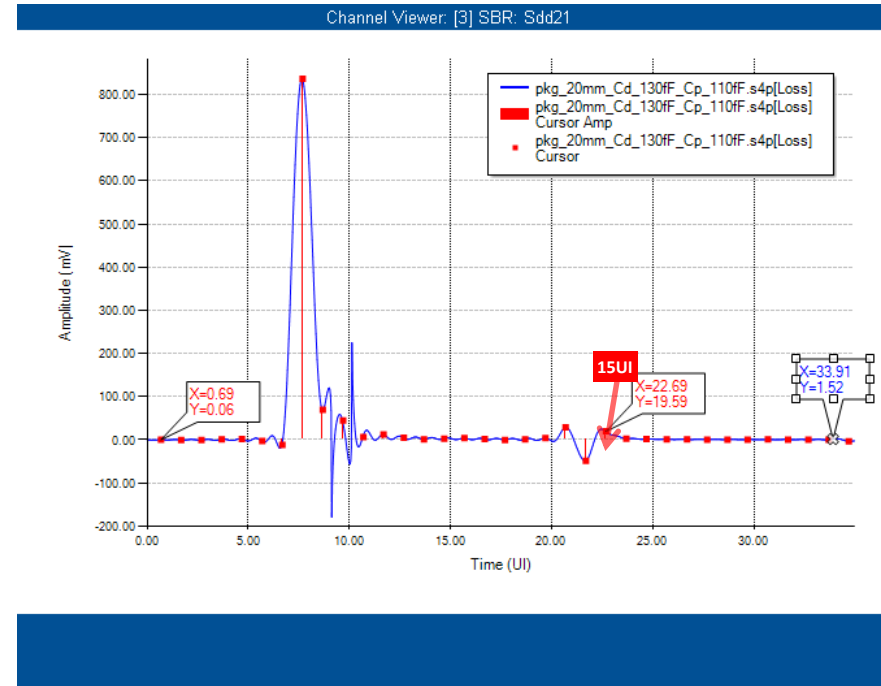
- TL: ~2.3 dB
- TL w/ 10% Cd + full Cp: ~3.2 dB**
- TL w/ full Cd + 10% Cp: ~3.5 dB
- TL w/ full Cd + full Cp: ~4.3 dB



112Gbps 20mm COM Package Model

(cont.)

- Potential ISI/EQ issue from the package
 - 20mm package has discontinuities at $\sim >15\text{UI}$ location (56Gbaud)
 - Indicate the need for >15 post-cursor EQ taps



100GEL Test Channel COM Results

w/ 30mm Packages w/o Crosstalk

Vendor	Channel w/o XTLK	FFE Tap Length (Post-tap Length)				
		16 (12)	20 (16)	24 (20)	28 (24)	32 (28)
Intel	BP_2conn_85ohm_30dB_Nom_t	-0.65	-0.36	0.19	1.35	1.6
Intel	BP_2conn_85ohm_30dB_HzLzHz_t	-1.08	-0.77	-0.17	1.35	1.8
Intel	BP_2conn_85ohm_30dB_LzHzLz_t	-0.53	-0.28	0.47	1.52	1.71
Samtec	BP__Z100sm_IL15to16_BC-BOR_N_N_N_t	0.39	0.42	0.56	3.14	3.25
Sametc	BP__Z100sm_IL25_27_BC-BOR_N_N_N_t	0.46	0.52	0.7	2.3	2.33
Sametc	BP__Z100sm_IL30to32_BC-BOR_N_N_N_t	-0.44	-0.43	-0.27	0.67	0.7
Samtec	CAd2d__2p0m_awg28_m_BC-BOR_N_N_N_t	0.3	0.33	0.35	2.09	2.03
Samtec	CAd2d__2p5m_awg28_m_BC-BOR_N_N_N_t	-0.04	-0.05	0.09	1.49	1.52
TE	G1112_Ortho_t	1.5	1.51	1.16	4.94	5.07
TE	B56_CblBP_t	1.92	2.17	2.72	4.66	4.67

Note: FFE is with 3 pre-taps. DFE tap length is 1.

- RX FFE coefficients are found using DFE-aware MMSE method
- Small solution space with 12~20 FFE/DFE post-taps

100GEL Test Channel COM Results

w/ 20mm Packages w/o Crosstalk

Vendor	Channel w/o XTLK	FFE Tap Length (Post-tap Length)				
		16 (12)	20 (16)	24 (20)	28 (24)	32 (28)
Intel	BP_2conn_85ohm_30dB_Nom_t	-1.93	0.62	1.72	1.94	1.99
Intel	BP_2conn_85ohm_30dB_HzLzHz_t	-2.29	0.45	2.11	2.38	2.43
Intel	BP_2conn_85ohm_30dB_LzHzLz_t	-1.53	0.99	2.33	2.63	2.69
Samtec	BP__Z100sm_IL15to16_BC-BOR_N_N_N_t	-0.58	1.88	2.45	3.01	3.07
Sametc	BP__Z100sm_IL25_27_BC-BOR_N_N_N_t	-0.56	1.57	2.05	2.55	2.79
Sametc	BP__Z100sm_IL30to32_BC-BOR_N_N_N_t	-1.09	0.56	0.96	1.39	1.56
Samtec	CAd2d__2p0m_awg28_m_BC-BOR_N_N_N_t	-0.06	2.17	2.19	2.2	2.21
Samtec	CAd2d__2p5m_awg28_m_BC-BOR_N_N_N_t	-0.32	1.65	1.69	1.69	1.69
TE	G1112_Ortho_t	1.65	5.42	5.43	5.61	5.75
TE	B56_CblBP_t	0.29	4.29	4.36	4.45	4.47

Note: FFE is with 3 pre-taps. DFE tap length is 1.

- RX FFE coefficients are found using DFE-aware MMSE method
- Small solution space with 12 FFE/DFE post-taps

100GEL Test Channel COM Results

w/ 20mm Packages with Crosstalk

Vendor	Channel w/o XTLK	FFE Tap Length (Post-tap Length)				
		16 (12)	20 (16)	24 (20)	28 (24)	32 (28)
Intel	BP_2conn_85ohm_30dB_Nom_t	-3.48	-1.7	-1.09	-0.99	-0.98
Intel	BP_2conn_85ohm_30dB_HzLzHz_t	-3.8	-1.92	-0.9	-0.83	-0.75
Intel	BP_2conn_85ohm_30dB_LzHzLz_t	-3.14	-1.36	-0.65	-0.48	-0.47
Samtec	BP__Z100sm_IL15to16_BC-BOR_N_N_N_t	-1.24	0.77	1.22	1.62	1.65
Sametc	BP__Z100sm_IL25_27_BC-BOR_N_N_N_t	-2.12	-0.62	-0.32	0.03	0.13
Sametc	BP__Z100sm_IL30to32_BC-BOR_N_N_N_t	-3.74	-3.02	-2.77	-2.59	-2.63
Samtec	CAd2d__2p0m_awg28_m_BC-BOR_N_N_N_t	-1.28	0.46	0.47	0.48	0.48
Samtec	CAd2d__2p5m_awg28_m_BC-BOR_N_N_N_t	-1.58	-0.27	-0.24	-0.24	-0.23
TE	G1112_Ortho_t	1.57	5.19	5.21	5.38	5.5
TE	B56_CbIBP_t	0.19	4.11	4.17	4.25	4.26

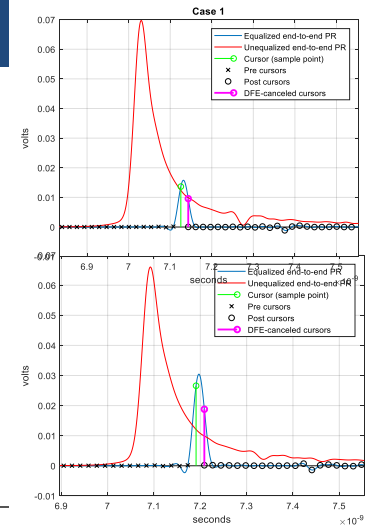
Note: FFE is with 3 pre-taps. DFE tap length is 1.

- RX FFE coefficients are found using DFE-aware MMSE method
- Small solution space with 12 FFE/DFE post-taps

100GEL Test Channel COM Results

w/ TX 30mm and RX 20mm Packages w/o Crosstalk

Vendor		Channel w/o XTLK	FFE Tap Length (Post-tap Length)				
			16 (12)	20 (16)	24 (20)	28 (24)	32 (28)
Intel		BP_2conn_85ohm_30dB_Nom_t	-1.36	-0.08	0.92	1.8	1.86
Intel		BP_2conn_85ohm_30dB_HzLzHz_t	-1.56	-0.13	1.15	2.03	2.07
Intel		BP_2conn_85ohm_30dB_LzHzLz_t	-1.12	-0.03	1.18	2.18	2.29
Samtec		BP_Z100sm_IL15to16_BC-BOR_N_N_N_t	1	1.83	2.38	3.8	3.92
Samtec		BP_Z100sm_IL25_27_BC-BOR_N_N_N_t	1.16	1.98	2.26	3.16	3.38
Samtec		BP_Z100sm_IL30to32_BC-BOR_N_N_N_t	0.16	0.82	1.06	1.55	1.63
Samtec		CAd2d__2p0m_awg28_m_BC-BOR_N_N_N_t	1.25	1.91	1.95	2.5	2.5
Samtec		CAd2d__2p5m_awg28_m_BC-BOR_N_N_N_t	0.93	1.57	1.63	2.11	2.11
TE		G1112_Ortho_t	2.59	3.68	3.65	5.4	5.53
TE		B56_CbIBP_t	2.18	4.12	4.42	4.97	4.99



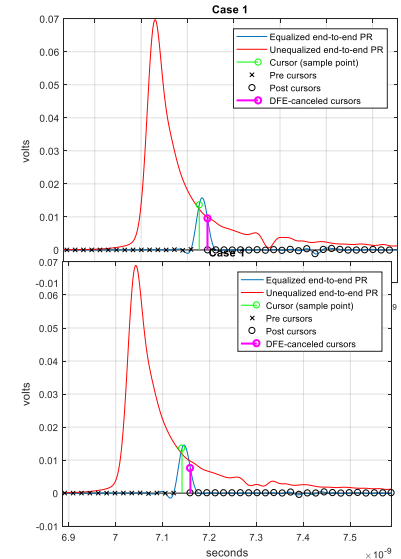
Note: FFE is with 3 pre-taps. DFE tap length is 1.

- RX FFE coefficients are found using DFE-aware MMSE method

100GEL Test Channel COM Results

w/ TX 22mm and RX 20mm Packages w/o Crosstalk

Vendor	Channel w/o XTLK	FFE Tap Length (Post-tap Length)				
		16 (12)	20 (16)	24 (20)	28 (24)	32 (28)
Intel	BP_2conn_85ohm_30dB_Nom_t	-0.36	0.73	2.18	2.27	2.29
Intel	BP_2conn_85ohm_30dB_HzLzHz_t	-0.51	0.64	2.27	2.34	2.35
Intel	BP_2conn_85ohm_30dB_LzHzLz_t	-0.17	0.9	2.43	2.62	2.66
Samtec	BP_Z100sm_IL15to16_BC-BOR_N_N_N_t	1.79	2.11	3.31	4.11	4.26
Samtec	BP_Z100sm_IL25_27_BC-BOR_N_N_N_t	1.42	1.89	2.94	3.6	3.77
Samtec	BP_Z100sm_IL30to32_BC-BOR_N_N_N_t	0.37	0.82	1.57	2.06	2.17
Samtec	CAd2d__2p0m_awg28_m_BC-	2.19	2.59	2.81	2.81	2.82
	BOR_N_N_N_t					
Samtec	CAd2d__2p5m_awg28_m_BC-	1.7	2.15	2.44	2.45	2.44
	BOR_N_N_N_t					
TE	G1112_Ortho_t	4.35	4.9	5.34	5.58	5.76
TE	B56_CbIBP_t	3.21	4.12	4.6	4.69	4.7



Note: FFE is with 3 pre-taps. DFE tap length is 1.

- RX FFE coefficients are found using DFE-aware MMSE method
- Greater solution space for channels with <28dB IL and with ≥ 24 (3 pre- + post-) EQ taps

Summary

- Progresses
 - Further improved COM FFE/DFE optimization method to be better align with practical design
 - Introduce 20mm reference package for non-high-density SOC usage for better power/area/cost
 - This enables reducing EQ post-tap length by ~ 7 taps, and associate power/area
- Recommendations
 - COM to include a 20mm reference package to enable better power/area/cost for medium density SOCs

Thank You