A Proposed ADC-DSP Receiver Reference Model for COM (Update)

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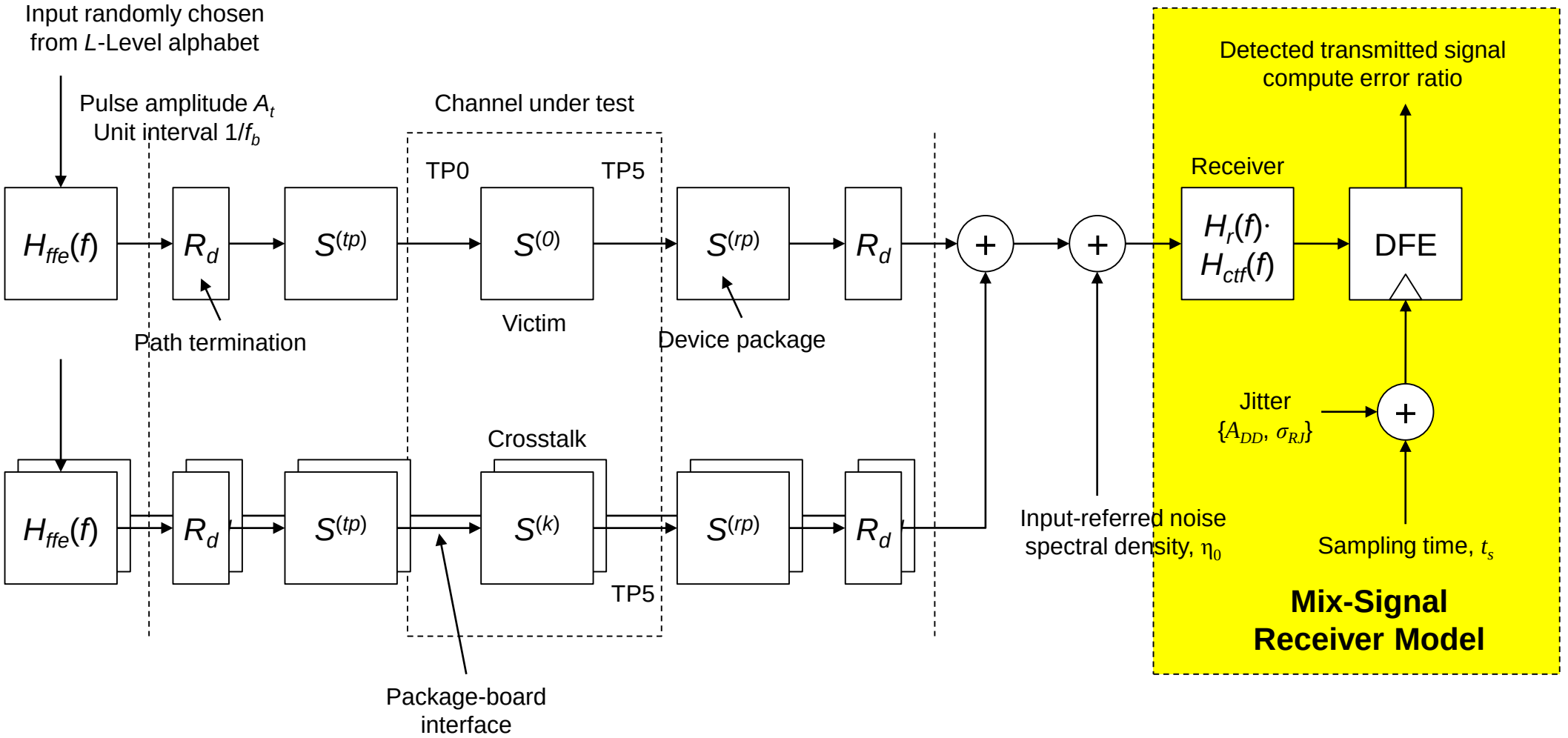
What do we have now?-- Mix-Signal Receiver Model

The model exactly match the reference design.

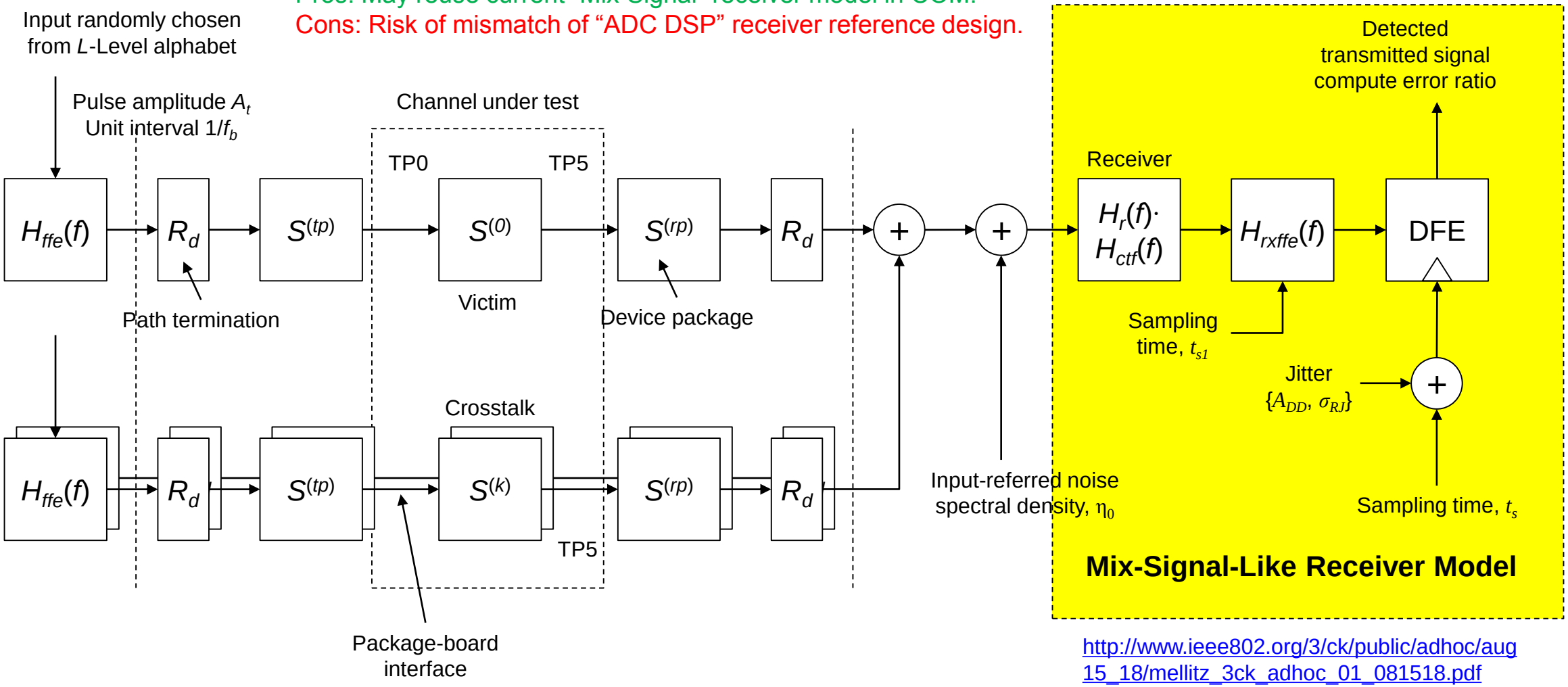


Reference: IEEE Std 802.3-2015, Annex 93A

Model under discussion: Mix-Signal-Like Receiver Model (COM2.41)

Pros: May reuse current “Mix-Signal” receiver model in COM.

Cons: Risk of mismatch of “ADC DSP” receiver reference design.

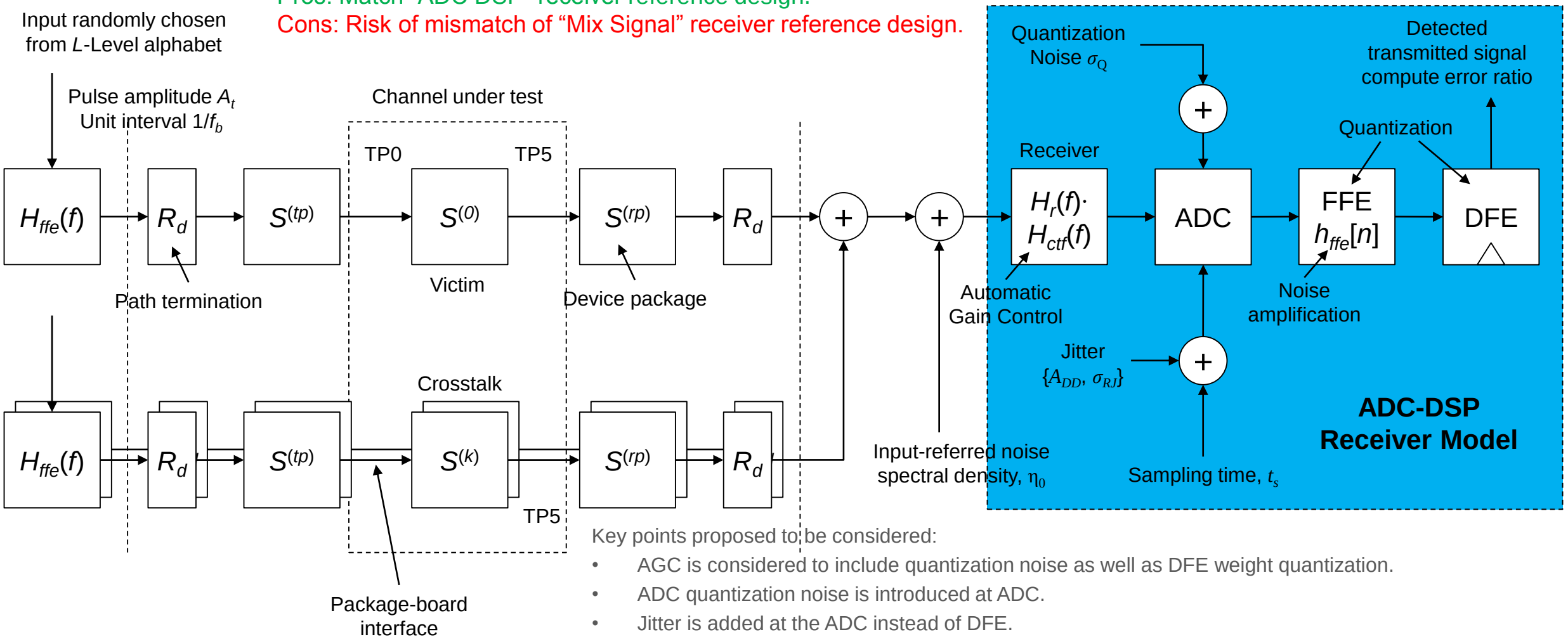


http://www.ieee802.org/3/ck/public/adhoc/aug15_18/mellitz_3ck_adhoc_01_081518.pdf

Proposed ADC-DSP Receiver Model

Pros: Match “ADC DSP” receiver reference design.

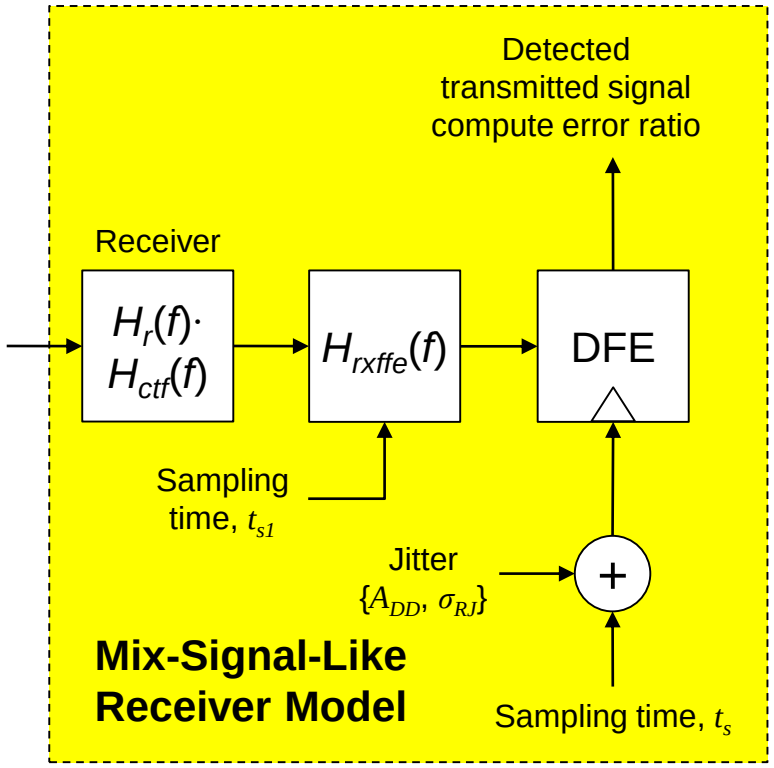
Cons: Risk of mismatch of “Mix Signal” receiver reference design.



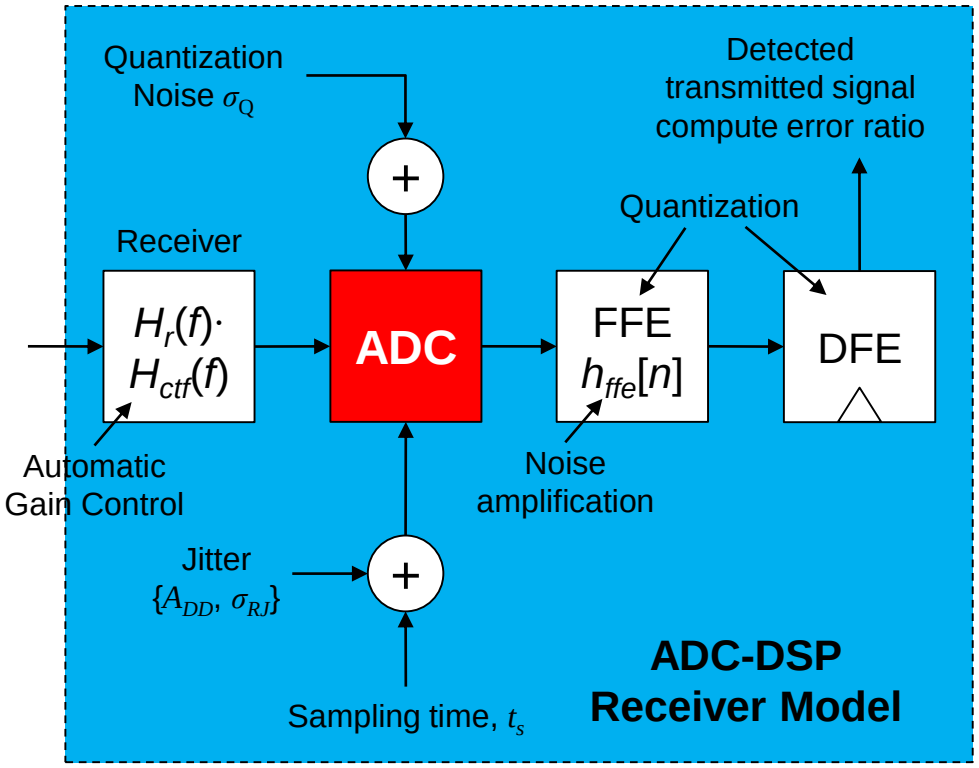
Key points proposed to be considered:

- AGC is considered to include quantization noise as well as DFE weight quantization.
- ADC quantization noise is introduced at ADC.
- Jitter is added at the ADC instead of DFE.
- Noise amplification of FFE is considered in time domain.
- Quantized FFE and DFE models are considered both in signal and weight values.

Key points proposed to be considered



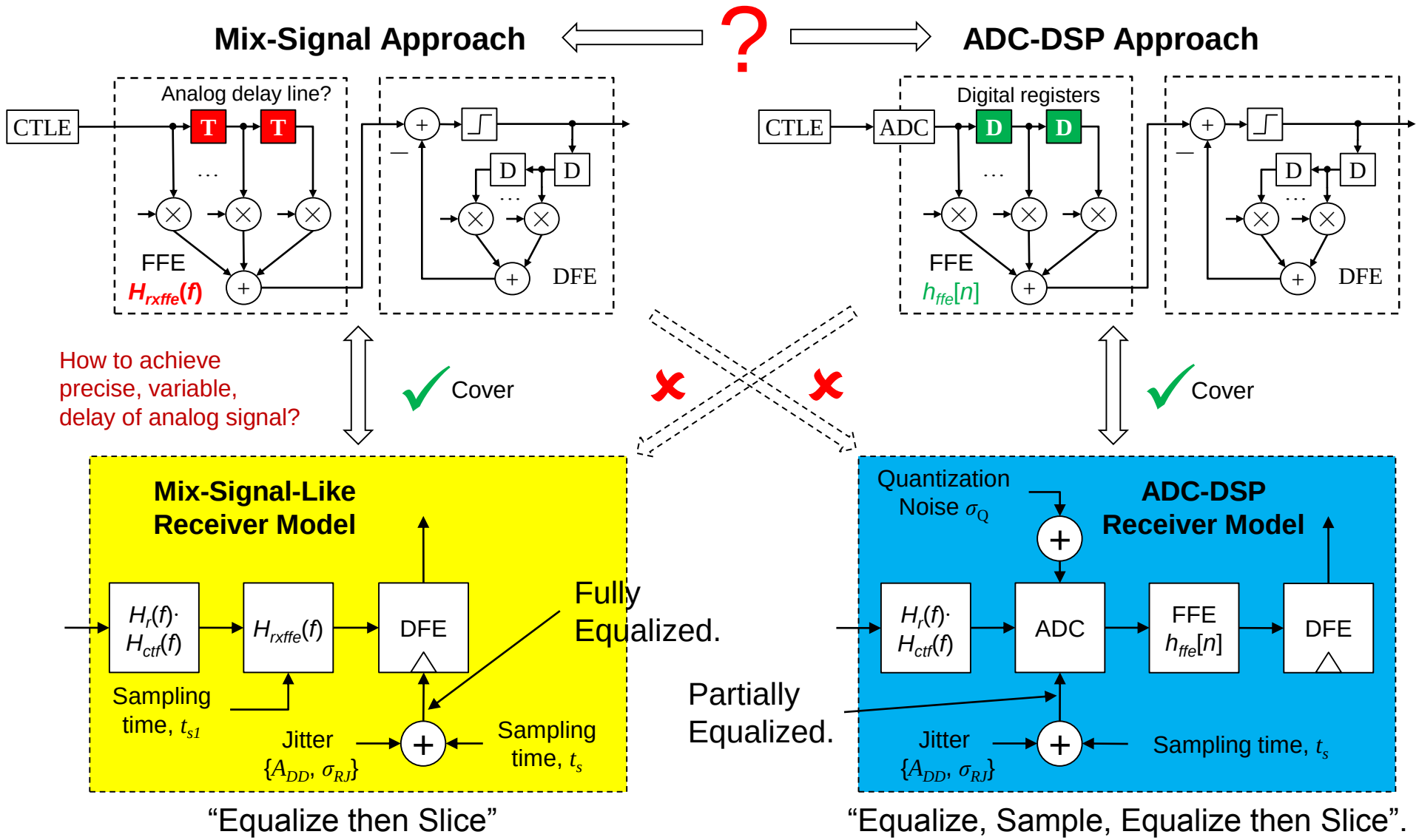
- ADC quantization noise is not considered.
- Automatic gain control is not explicitly considered.
- Quantization of FFE&DFE are considered in analog way.
- Jitter is added at DFE.
- RX FFE is modeled in continuous frequency domain.



- ADC quantization noise is considered.
- Automatic gain control is considered.
- Quantization of FFE&DFE are considered in digital way.
- Jitter is added at ADC instead of DFE.
- RX FFE is modeled in discrete time domain.

The proposed ADC DSP receiver model is not implementation-oriented, but considers a minimum set of parameters.

Recommend Explicit Model: Symbols should have Specific Meanings

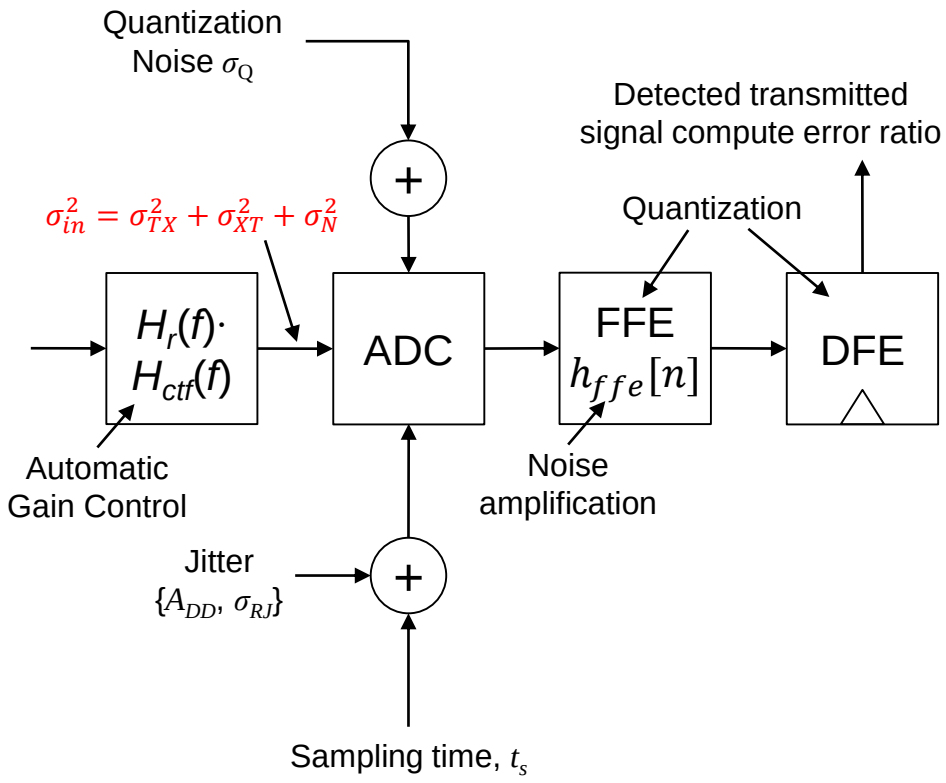


Parameters in Proposed ADC DSP Receiver Model

Parameter	Symbol	Units	Equivalent COM2.41 parameters	Values	Units	Mapping to ADC DSP model
ADC input amplitude	A_{adc}	**mV**	**Not considered**	**N.A.**	**N.A.**	**Not defined in COM2.41**
ADC resolution	N_{adc}	**bit**	**Not Considered**	**N.A.**	**N.A.**	**Not defined in COM2.41**
FFE weight bit number	N_{ffe}	bit	ffe_tap_step_size	0.01	Normalized to main tap=1	$N_{\mathrm{ffe}} = log2\left(\frac{2}{\mathbf{0.01}}\right) = \mathbf{7.6}$ bits $N_{\mathrm{ffe}} = 7$ means $\frac{1}{64}$ step size.
DFE weight bit number	N_{dfe}	bit	N_b_step	0.0115	Normalized? Equivalent to AGC?	$N_{\mathrm{dfe}} = log2\left(\frac{2}{\mathbf{0.0115}}\right) = \mathbf{7.4}$ bits?
FFE Post Tap Number*	$N_{\mathrm{post\_ffe}}$	--	ffe_post_tap_len	32	--	Same
FFE Pre Tap Number	$N_{\mathrm{pre\_ffe}}$	--	ffe_pre_tap_len	3	--	Same
DFE Tap Number	N_b	UI	N_b	1	UI	Same
* The FFE Tap Number is changed to FFE Post Tap Number to align with COM 2.41.						

- No new “parameters” are introduced, except for A_{adc} and N_{adc} which are related to “ADC quantization noise”.
  - ADC quantization noise should be considered in ADC DSP receiver. It is too optimistic to ignore ADC quantization noises.
  - “The famous 3dB minimum was allowance for implementation ’penalties’ ” not for modeling “penalties”.
    - Modeling should be accurate. The “penalties” should be allocated to the variation of A_{adc}, N_{adc}, N_{ffe}, N_{dfe}, etc. for different ADC DSP receiver implementation.
- The FFE&DFE weight number N_{ffe} & N_{dfe} are equivalent to the “ffe_tap_step_size” and “N_b_step”.
  - No difference in the difficulty of consensus building. But N_{ffe} & N_{dfe} are the natural language for ADC DSP receivers.
  - N_{ffe} & N_{dfe} make a lot of sense to ADC DSP receivers. They are directly mapped to the receiver architecture.
  - Even with “Mix-Signal-Like” model, It is hard to define “N_b_step” without defining automatic gain control (AGC).

Formulas for ADC-DSP Reference Receiver Model



Only 4 formulas in red are needed to be added/amended to support ADC-DSP model, while all the others can be reused.

$$h_J(n) = \frac{h(t_s+(n+1/M)T_b) - h(t_s+(n-1/M)T_b)}{2/M}$$

$$\sigma_X^2 = \frac{L^2-1}{3(L-1)^2}$$

$\sigma_{in}^2 = \sigma_{TX}^2 + \sigma_{XT}^2 + \sigma_N^2$, scaled by the AGC gain.

$$\sigma_{TX}^2 = \left[h^{(0)}(t_s)\right]^2 \cdot 10^{-SNR_{TX}/10}$$

$$\sigma_Q^2 = \frac{1}{3}\left(\frac{A_{adc}}{2^{N_{adc}}-1}\right)^2$$

$$\sigma_{ISI}^2 = \sigma_X^2 \cdot \sum_i h_{ISI}^2(i)\,,$$

$$\sigma_J^2 = \left(A_{DD}^2 + \sigma_{RJ}^2\right) \cdot \sigma_X^2 \cdot \sum_n h_J^2(n)$$

$$[\sigma_m^k]^2 = \sigma_X^2 \sum_n \left[h^{(k)}\left((m/M+n)T_b\right)\right]^2$$

$$\sigma_{XT}^2 = \sum_{k=1}^{K-1}\left[\sigma_i^k\right]^2$$

$$\alpha_{\mathrm{FFE}} = \sqrt{\sum_i h_{ffe}[i]^2}$$

$$\sigma_N^2 = \eta_0 \int_0^\infty \left|H_r(f)\cdot H_{ctf}(f)\right|^2 df$$

$$A_{ni}^2 = \alpha_{\mathrm{FFE}}^2 \cdot \left(\sigma_{\mathrm{in}}^2 + \sigma_Q^2 + \sigma_J^2\right) + \sigma_{ISI}^2$$

$$FOM = 20 \cdot \log_{10}\left(\frac{A_s}{A_{ni}}\right)$$

ADC resolution	5	6	7	8
σ_Q in mV @A_{adc}=200mV	3.72	1.83	**0.91**	0.45

Upper bound of σ_N:
$\sqrt{8.2\times10^{-9}\mathrm{V^2/GHz} * 56\mathrm{GHz}} \times 10^3 = 0.6776\mathrm{mV}$

Quantization noise cannot be neglected

All the formulas in “black” are from Annex 93A.

A Comparison List of “Mix-Signal-Like” Model and “ADC DSP” Model

	Mix-Signal-Like Model (COM2.41)	ADC-DSP Model
Applicable receiver architecture	Mix-Signal Receiver	ADC DSP Receiver
ADC quantization	Not Considered	Considered
Sampling phase and Jitter consideration	Sample & Add @ DFE Match Mix-Signal Receiver	Sample & Add @ ADC Match ADC-DSP Receiver
Quantization of FFE&DFE Weight	Match the language of Mix-Signal Design (‘step’)	Match the language of DSP Design (‘bit number’)
# of new parameters	5 (without considering ADC quantization noise)	7 (A_{adc} & N_{adc} are for ADC quantization noise)
# of added/amended formulas	?	4
Implementation Independent?	Yes	Yes

Suggestions and Future Work

- What receiver types do we need? “Mix-Signal”, “ADC-DSP” or both? Select the corresponding reference model for a specific architecture. Mix-up things will lead to confusion even though they may be close to each other in mathematics.
  - “Mix-Signal Model” for “Mix-Signal Receiver”
  - “ADC DSP Model” for “ADC DSP Receiver”
- For ADC-DSP Receiver model
  - ADC Quantization noise should be considered.
  - No “new” parameters are introduced, except for DSP language alignments.
    - The problem will be simplified because the “language” is aligned.
    - “number of bits” is common language for DSP designers.
    - “step” will lead to fractional bit number which is very confusing.
  - The workload of proposed ADC-DSP model is fair.
- Future Work
  - Recommend to do consensus building on the type of receivers.
  - Sensitive study of parameters extracted from the ADC-DSP Receiver Model.
  - Comparative study of “ADC-DSP Receiver Model” and “Monte-Carlo IBIS/AMI model”

Acknowledgement

- We appreciate people reviewed and commented on this model and are looking forward to working together with the group to improve the COM model.

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THANK YOU