Comparison Between Equalization, COM Package Models, and COM For 100G Base KR Channels

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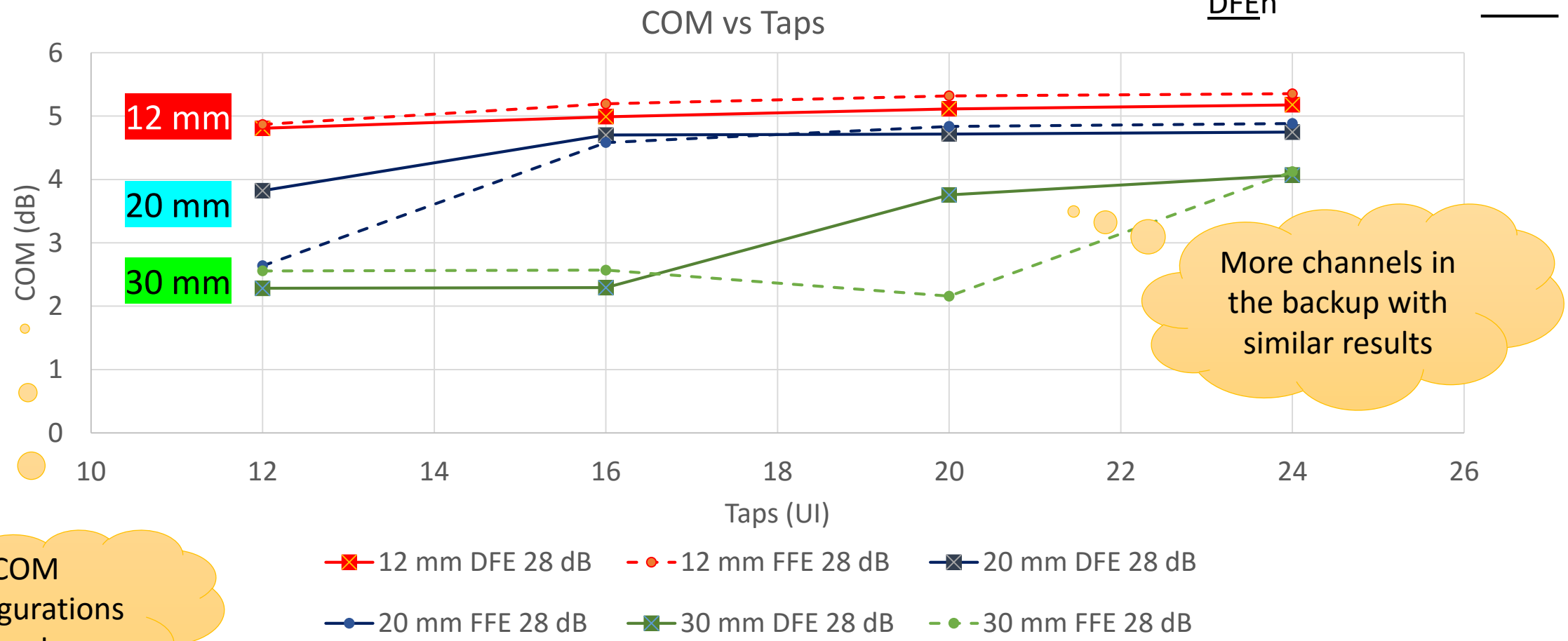
- ❑ Experiment using seven 100G-Base-KR channel models
  - For three 93A style package choices, 12 mm, 20mm, 30 mm
- ❑ Compute COM for 4 selections of post cursors equalization for DFE and DFE1/rx FFEn
- ❑ Compute COM for a finer sweep of number of post cursor taps for a channel with a BGA PCB via reflection
  - For three package choices, 12 mm, 20 mm, 30 mm
  - For a 30 mm “flex” package model
- ❑ Observations
- ❑ Recommendations

mellitz...081518/CaBP_BGAVia_Opt2_28dB (26.3 dB @ 26.6GHz cabled backplane (with BGA vias) with crosstalk and original 93A style package

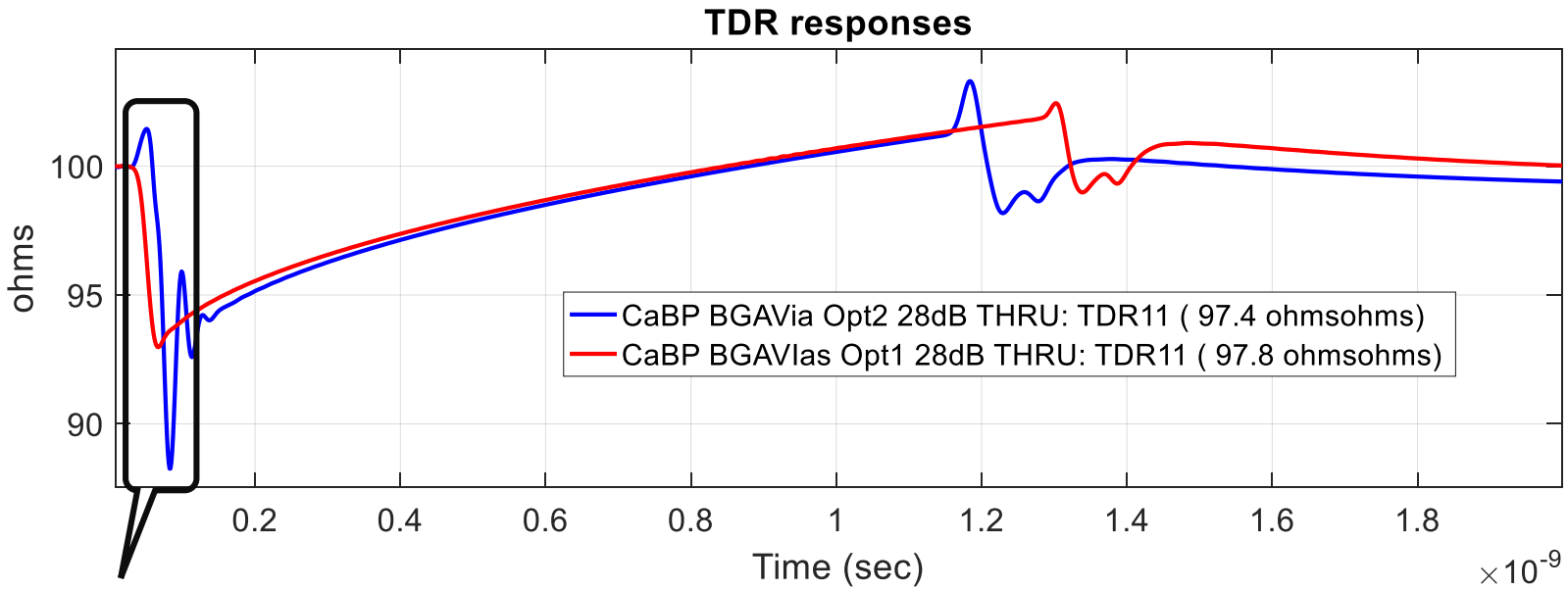
DFE1-Rx FFE(3,1,n) - - - - -
DFEn ——



COM Configurations in backup

A Closer look

- We use a channel with a BGA via to make sure we include re-reflections from the packages
  - ~26 dB cabled backplane Option 2 (mellitz_3ck_02_081518)

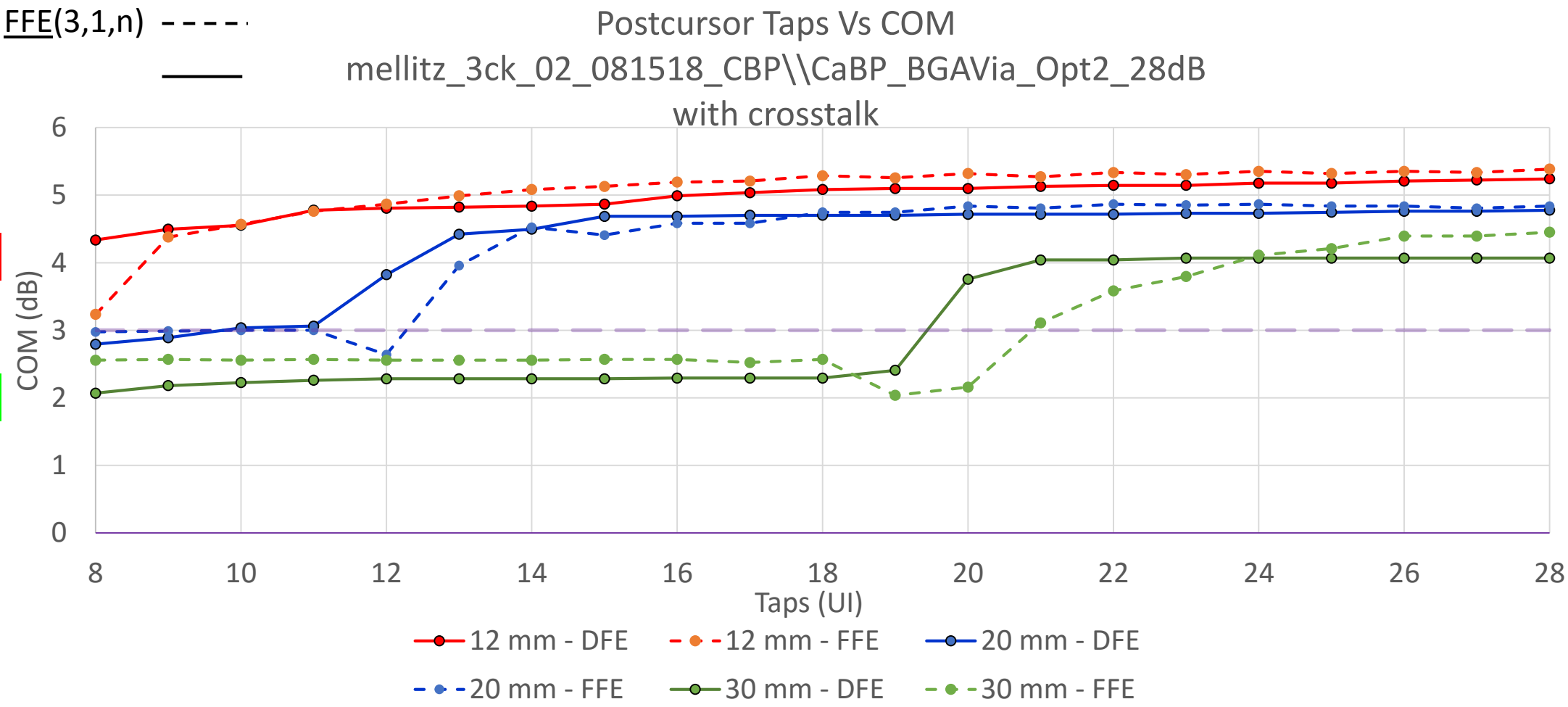


BGA breakout via

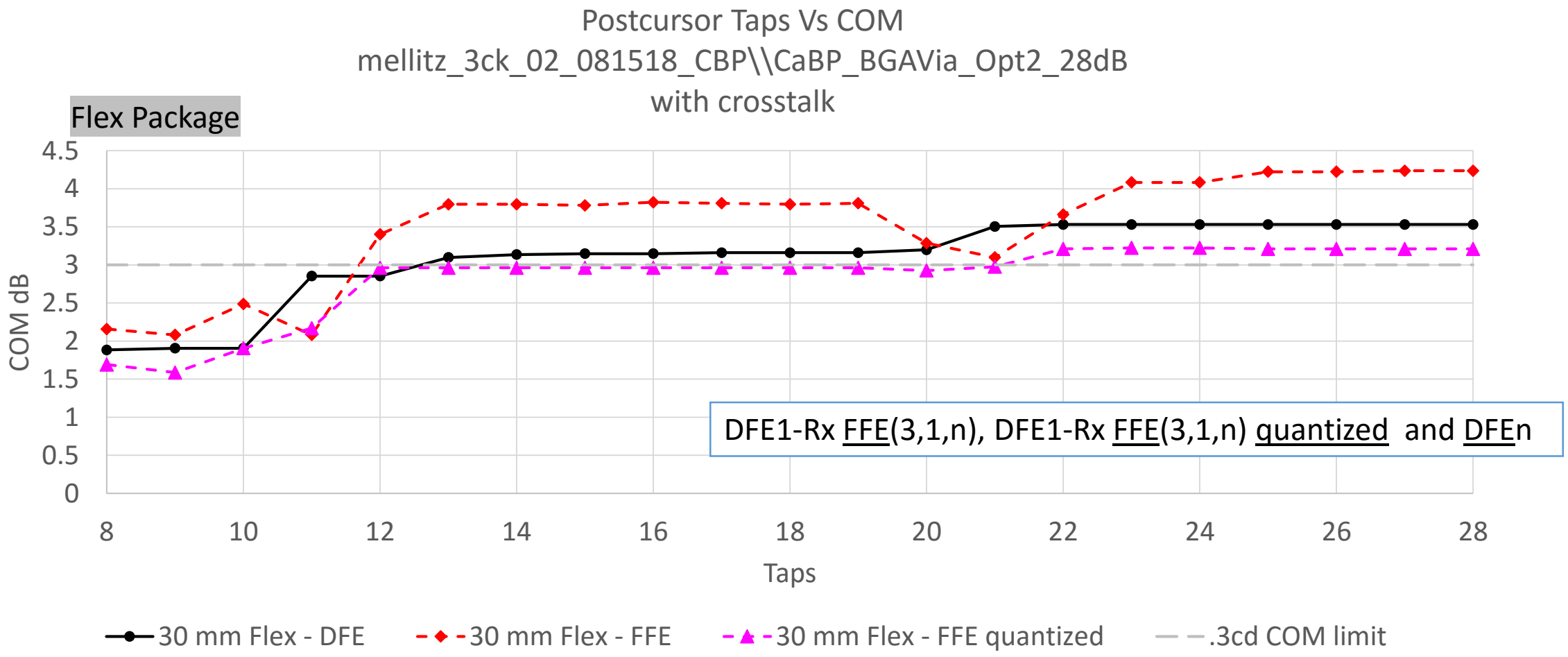
COM vs Single Step Increment for Post Cursor Taps

DFE1-Rx FFE(3,1,n) - - - -
DFEn ———

12 mm
20 mm
30 mm



COM vs single post cursor tap steps for DFE1-Rx FFE(3,1,n) and DFEn FFE Quantized and DFE



Discussion

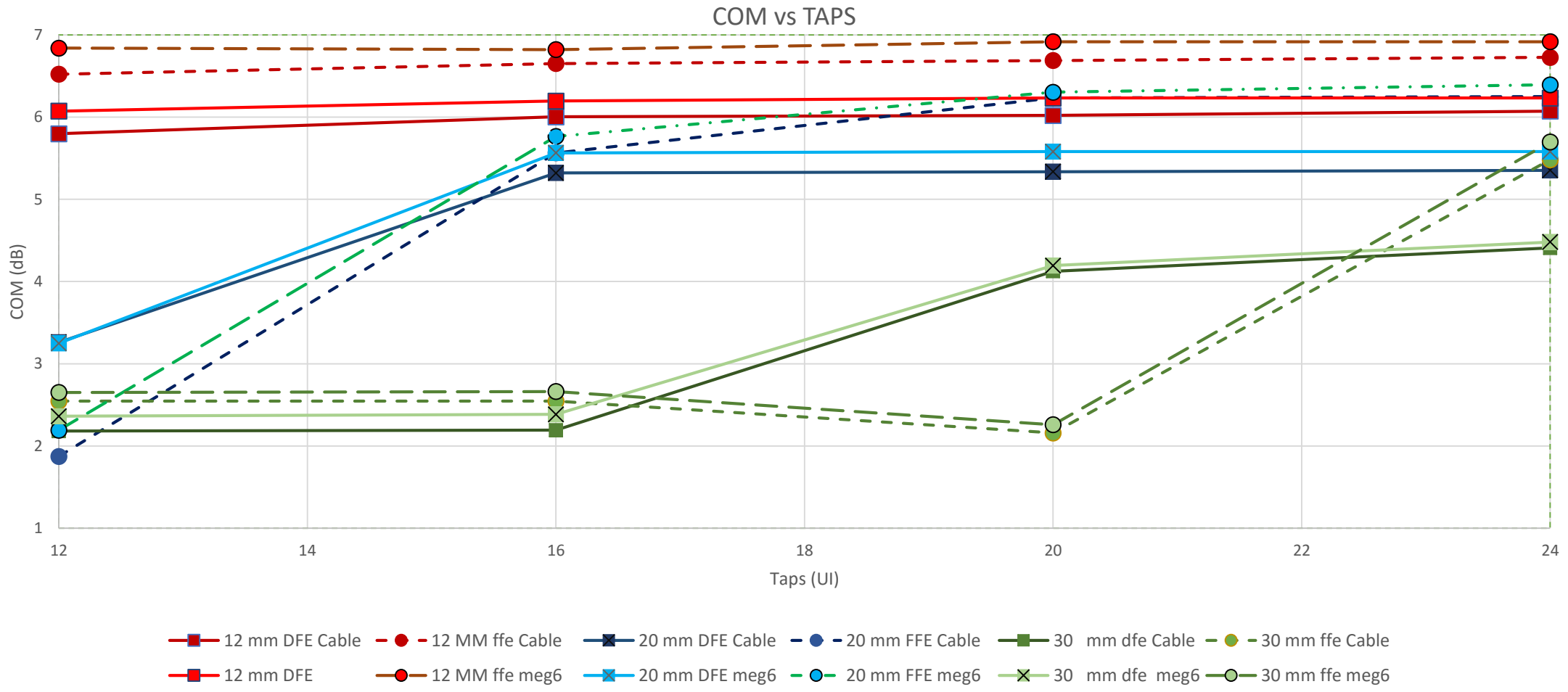
- DFE may not represent some actual designs - is this OK?
  - It was OK in the past – some designs were different
  - COM is not a simulation tool, it is a method for qualifying channels
- Rx FFE reference COM architecture opens up many issues
  - Has to be more complex to match an actual implementation
  - Implementation may still differ; how to choose?
  - Likely to cause .3ck project delays
- Rx FFE may have higher implementation penalty compared to DFE
  - Add more noise terms?
  - Or raise the bar above 3 dB (to what?)
- Flex package looks better
  - Needs fewer taps than current reference package

Recommendation for Qualifying .3ck Channels Using COM Reference Signal architecture

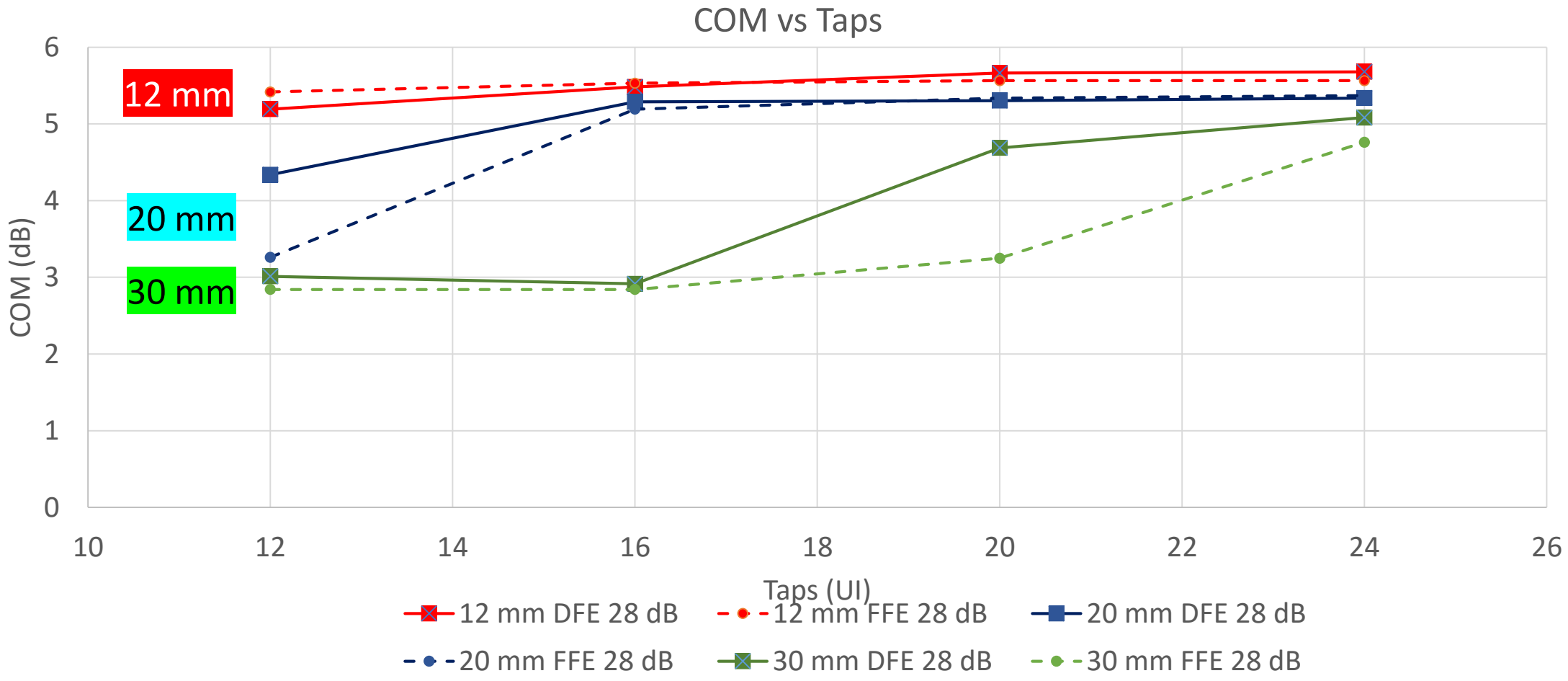
- Use the DFE with N_b=16 for the COM reference receiver
  - A few taps added for N_b to cover other channels and package models variation
  - Assume Flex package
- Entertain proposals for other noise factors for the FOM to cover Rx FFE and ADC-DSP

Backup

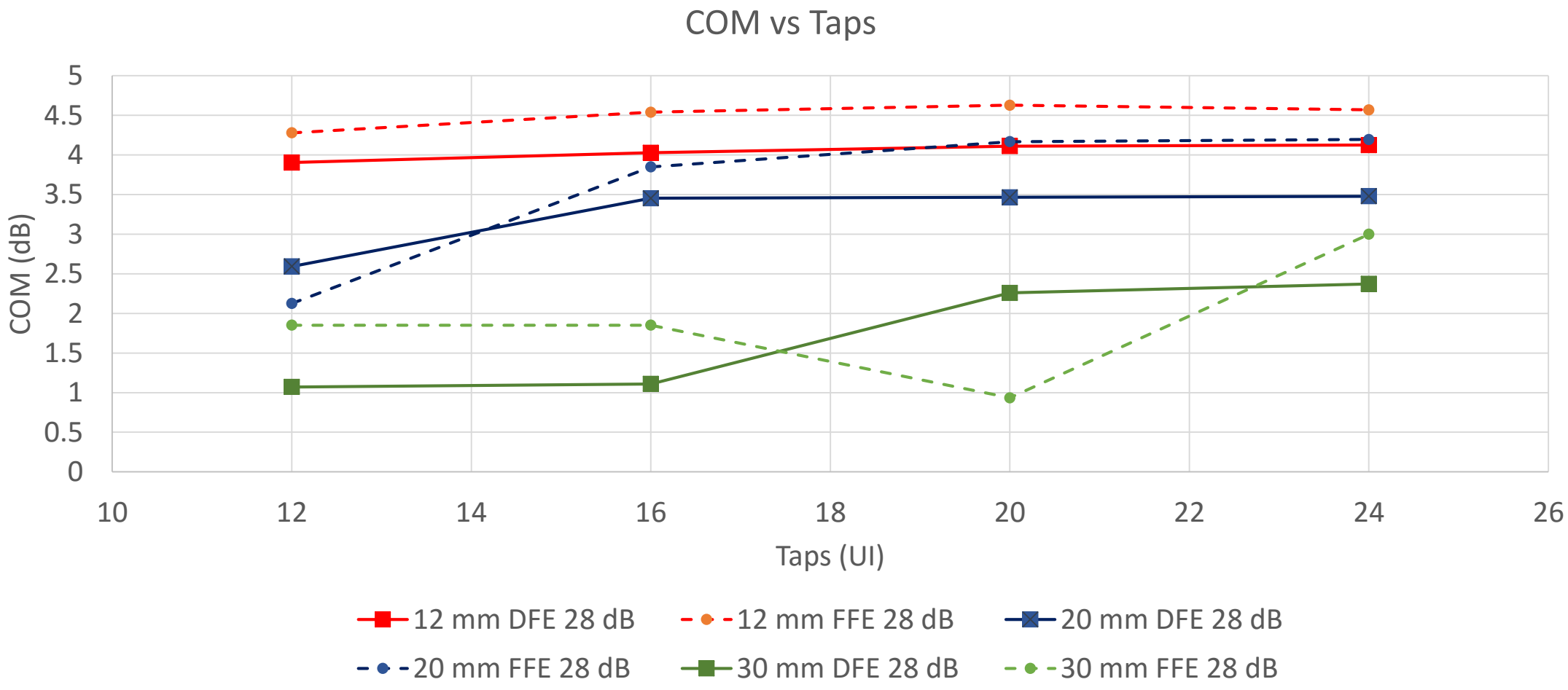
28 dB @ 26.6 GHz Ideal 100 Ω Cable and PCB Transmission Line



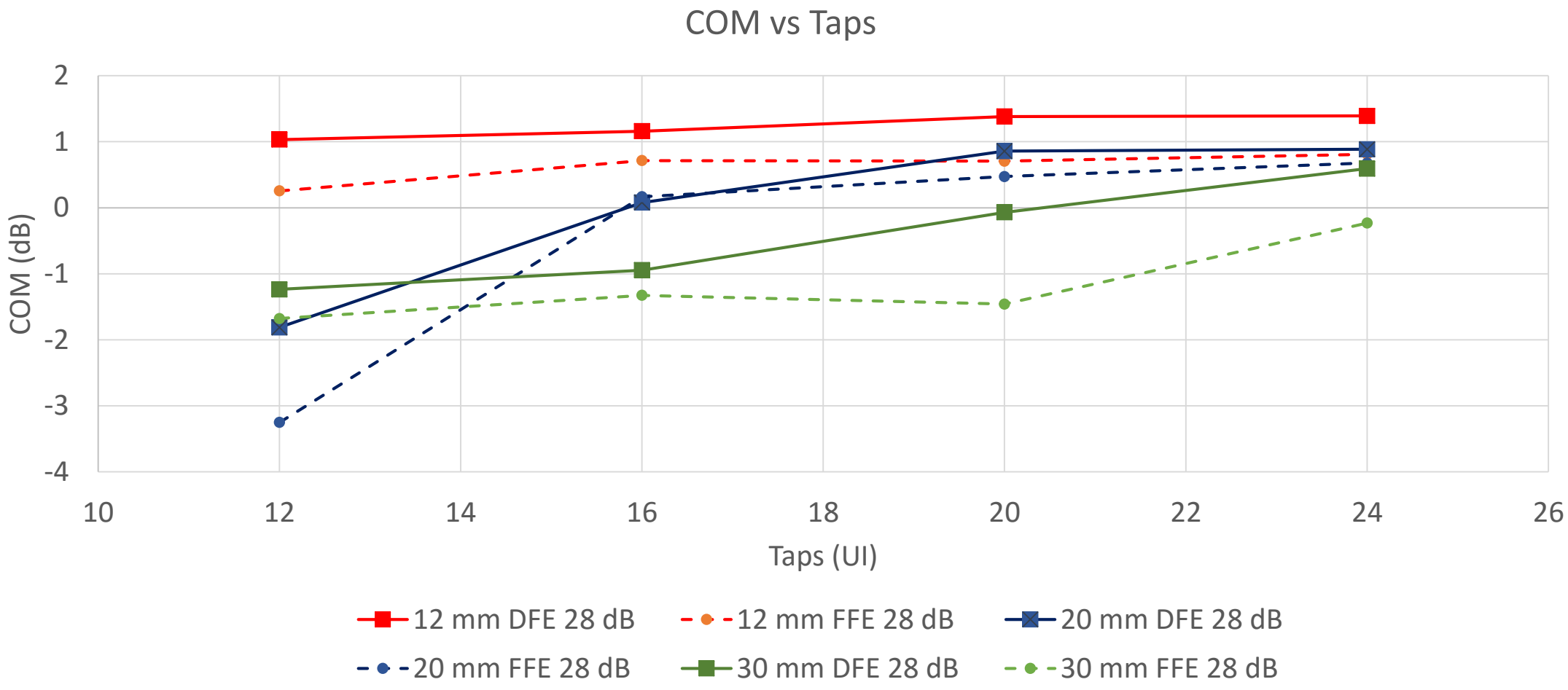
mellitz…081518/CaBP_BGAVia_Opt2_24dB (22.6 dB @ 26.6GHz cabled backplane (with BGA vias)



mellitz...081518/CaBP_BGAVia_Opt2_32dB (28 dB @ 26.6GHz cabled backplane (with BGA vias)



heck_100GEL_85ohm_hlh_01_011718\BP_2conn_85ohm_30dB_HzLzHz_thru.s4p



zambell_100GEL_02_0318\Ortho_C1_Pr_14_to_Pr_5\Thru_Ortho_C1_Pr_14_to_Pr_5.s4p

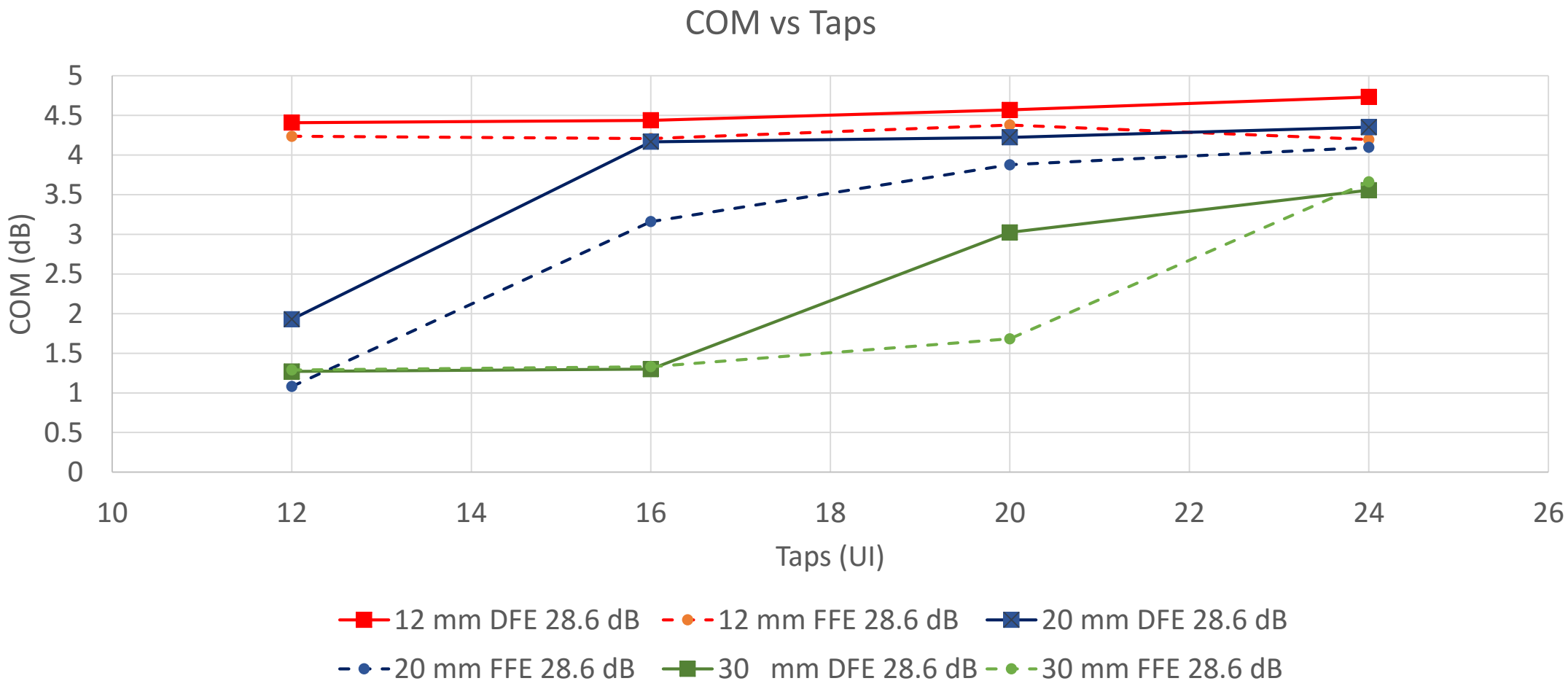


Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.1e-4 1.1e-4]	nF	[TX RX]
z_p select	1		[test cases to run]
z_p (TX)	[15.5; 1.8; 7.5; 7]	mm	[test cases]
z_p (NEXT)	[15.5; 1.8; 7.5; 7]	mm	[test cases]
z_p (FEXT)	[15.5; 1.8; 7.5; 7]	mm	[test cases]
z_p (RX)	[15.5; 1.8; 7.5; 7]	mm	[test cases]
C_p	[0.7e-4 0.7e-4]	nF	[TX RX]
C_v	[5e-6 5e-6]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.41	V	
A_fe	0.41	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		[min:step:max]
c(-3)	[-0.1:0.025:0]		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	[-0.1:0.025:0]		[min:step:max]
N_b	**1 oe n**	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	
ffe_pre_tap_len	**3 or 0**	UI	
ffe_post_+A1:L39tap_len	**n or 0**	UI	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR2_ev al1_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
DER_0	1.00E-04	
Include PCB	0	Value
T_r	6.16E-03	ns
FORCE_TR	1	logical

TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.18**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

ffe_tap_step_size	**0.01 or 0**

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 1.0404e-3 4.201e-4]	
package_tl_tau	6.325E-03	ns/mm
package_Z_c	[87.5 87.5 ; 110 110; 87.5 87.5; 87.5 87.5]	Ohm (Tx Rx)

Table 92–12 parameters	
Parameter	**Setting**
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]
board_tl_tau	6.191E-03 ns/mm
board_Z_c	110 Ohm
z_bp (TX)	151 mm
z_bp (NEXT)	72 mm
z_bp (FEXT)	72 mm
z_bp (RX)	151 mm

COM Spreadsheet: Flex Style Package

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.1e-4 1.1e-4]	nF	[TX RX]
z_p select	[1 2 3]		[test cases to run]
z_p (TX)	[15.5 20 30]	mm	[test cases]
z_p (NEXT)	[15.5 20 30]	mm	[test cases]
z_p (FEXT)	[15.5 20 30]	mm	[test cases]
z_p (RX)	[15.5 20 30]	mm	[test cases]
C_p	[1.1e-4 1.1e-4]	nF	[TX RX]
		nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.41	V	
A_fe	0.41	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		[min:step:max]
c(-3)	[-0.1:0.025:0]		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	[-0.1:0.025:0]		[min:step:max]
N_b	**1 oe n**	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	
ffe_pre_tap_len	**3 or 0**	UI	
ffe_post_+A1:L39tap_len	**n or 0**	UI	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR2_ev al1_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
DER_0	1.00E-04	
Include PCB	0	Value
T_r	6.16E-03	ns
FORCE_TR	1	logical

TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.18**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

ffe_tap_step_size	**0.01 or 0**

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	87.5	Ohm (Tx Rx)

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	110	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

COM Spreadsheet: Original Package Style