Cl 73 AN baseline proposal for 802.3ck

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802.3ck Objectives for Copper Links

- 100GBASE-CR
- 100GBASE-KR
- 200GBASE-CR2
- 200GBASE-KR2
- 400GBASE-CR4
- 400GBASE-KR4

Clause 73 Auto-Negotiation Process

- Provides mechanism for links to negotiate the fastest common rate that both sides advertise.
- Useful for plug-and-play linking up
- Copper PHY type support only

Proposal

- Update Clause 73 AN to support new copper PHY types
- Follow the 802.3by/cd approach of not distinguishing between the Backplane and Copper Cable PHYs during AN.
  - The same SerDes generally supports both Direct Attach Copper (DAC) and Backplane (BP)
  - Implementations know if the Port is DAC or BP so they can take care of all the necessary SerDes setup before starting AN to configure the appropriate PMD operation
- FEC is non-negotiable for these PHYs

Figure 73-1 Update

- Add 400GMII

73.5.1 Update

- For any multi-lane PHY, DME pages shall be transmitted only on lane 0. The transmitters on other lanes should be disabled as specified in 71.6.7, 84.7.7, 85.7.7, 92.7.7, 93.7.7, or 94.3.6.7, 136.8.7, ~~or~~ 137.8.7, KKK.X.Y or CCC.X.Y.

73.10.1 Update

- Add 100GR, 200GR2 and 400GR4 variables and link_status

Table 73-4 Technology Ability Field Updates

Bit	Technology
A13[1]	50GBASE-KR or 50GBASE-CR
A14[1]	100GBASE-KR2 or 100GBASE-CR2
A15[1]	200GBASE-KR4 or 200GBASE-CR4
A16	100GBASE-KR or 100GBASE-CR
A17	200GBASE-KR2 or 200GBASE-CR2
A18	400GBASE-KR4 or 400GBASE-CR4
A19 through A22	Reserved for future technology

1. Added by 802.3cd

Table 73-5 Priority Resolution Updates

Priority	Technology	Capability
1	400GBASE-CR4 or 400GBASE-KR4	400Gb/s 4 lane, highest priority
2	200GBASE-CR2 or 200GBASE-KR2	200Gb/s 2 lane
3	200GBASE-CR4 or 200GBASE-KR4	200Gb/s 4 lane~~, highest priority~~
4	100GBASE-CR or 100GBASE-KR	100Gb/s 1 lane
5	100GBASE-CR2 or 100GBASE-KR2	100Gb/s 2 lane
6	100GBASE-CR4	100Gb/s 4 lane
7	100GBASE-KR4	100Gb/s 4 lane
8	100GBASE-KP4	100Gb/s 4 lane
9	100GBASE-CR10	100Gb/s 10 lane
…	Etc.	

Table 73-7 Timer min/max value summary

Parameter	Min	Value and tolerance	Max	Unit
Link_fail_inhibit_timer (when the link is 100GBASE-KR, 100GBASE-CR, 200GBASE-KR2, 200GBASE-CR2, 400GBASE-KR4 or 400GBASE-CR4)	TBD		TBD	m
Link_fail_inhibit_timer (when the link is 50GBASE-KR, 50GBASE-CR, 100GBASE-KR2, 100GBASE-CR2, 200GBASE-KR4, or 200GBASE-CR4)	3.1		3.2	s
Link_fail_inhibit_timer (when the link is 10GBASE-KR, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, 25GBASE-CR-S, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-KR4, 100GBASE-KP4, 100GBASE-CR4 or 100GBASE-CR10)	500		510	ms
Link_fail_inibit_timer (when the link is 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR or 10GBASE-KX4)	40		50	ms

Conclusion

- The previous 4 slides provide a baseline for how to update Cl 73 to support the new copper PHYs being defined in P802.3ck

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