

Trace and Chassis Tolerances vs. COM

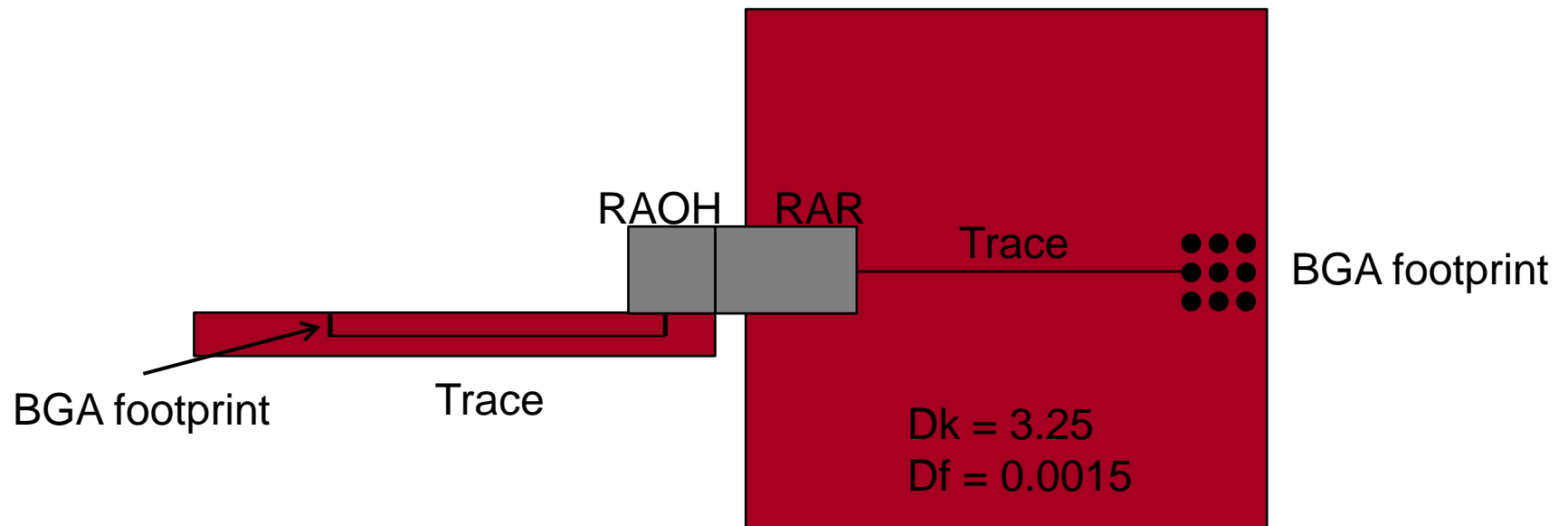
Andy Zambell
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Purpose

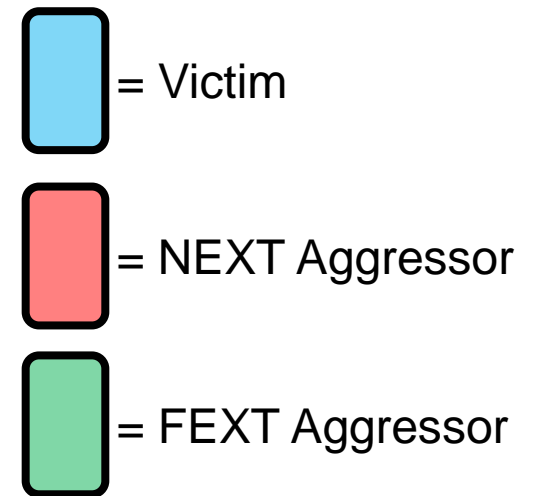
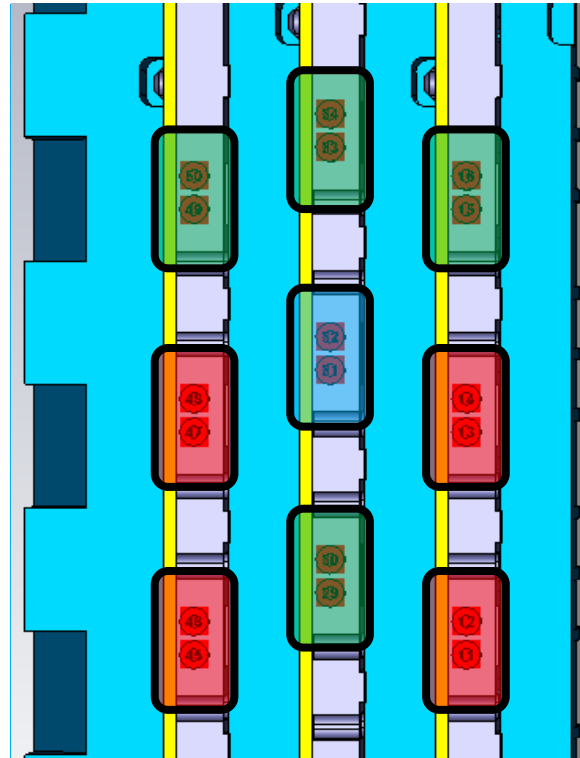
- The purpose of this presentation is to see how varying trace impedance and connector mating due to chassis tolerance affects COM.

Channel Description

- A BGA footprint and an 85 ohm, 92.5 ohm, and/or 100 ohm trace was concatenated to either side of three measured, de-embedded direct-mate orthogonal connectors, which includes the connector footprints.
 - The three de-embedded connector models are all from the same measured connector, except one model is fully mated, one is de-mated 0.5 mm, and the third is de-mated 1.0 mm.
 - Trace lengths were varied based on impedance so the loss of each trace would be the same.
- Due to test fixture loss, the de-embedded connector bandwidth is 35GHz.
 - Test fixture with 50 GHz of bandwidth is in development.



Wiring Pattern



Channels

	Trace 1	Conn	Trace 2
Ch. 1	85	0	85
Ch. 2	92.5	0	92.5
Ch. 3	100	0	100
Ch. 4	85	0.5	85
Ch. 5	92.5	0.5	92.5
Ch. 6	100	0.5	100
Ch. 7	85	1	85
Ch. 8	92.5	1	92.5
Ch. 9	100	1	100

	Trace 1	Conn	Trace 2
Ch. 10	85	0	92.5
Ch. 11	85	0	100
Ch. 12	85	0.5	92.5
Ch. 13	85	0.5	100
Ch. 14	85	1	92.5
Ch. 15	85	1	100
Ch. 16	92.5	0	85
Ch. 17	92.5	0	100
Ch. 18	92.5	0.5	85

	Trace 1	Conn	Trace 2
Ch. 19	92.5	0.5	100
Ch. 20	92.5	1	85
Ch. 21	92.5	1	100
Ch. 22	100	0	85
Ch. 23	100	0	92.5
Ch. 24	100	0.5	85
Ch. 25	100	0.5	92.5
Ch. 26	100	1	85
Ch. 27	100	1	92.5

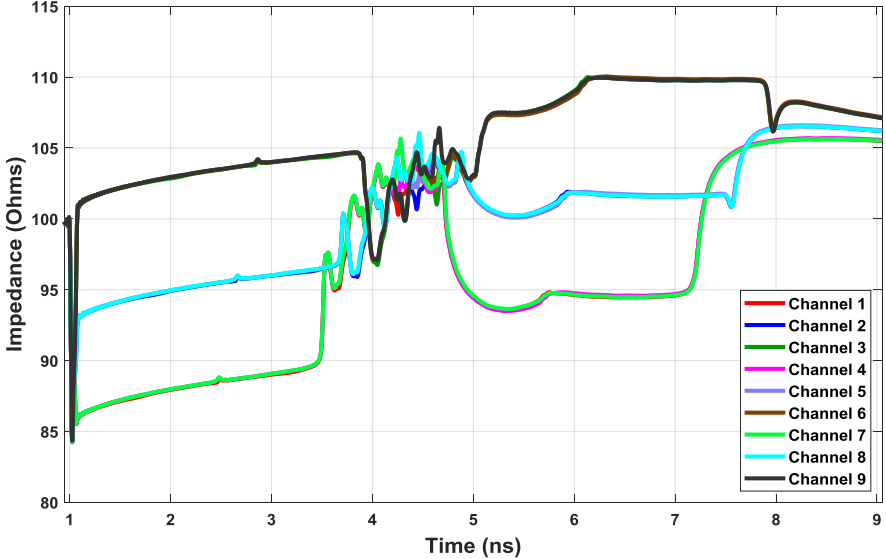
Trace 1 = Trace impedance on RAOH side

Conn = De-mate in mm

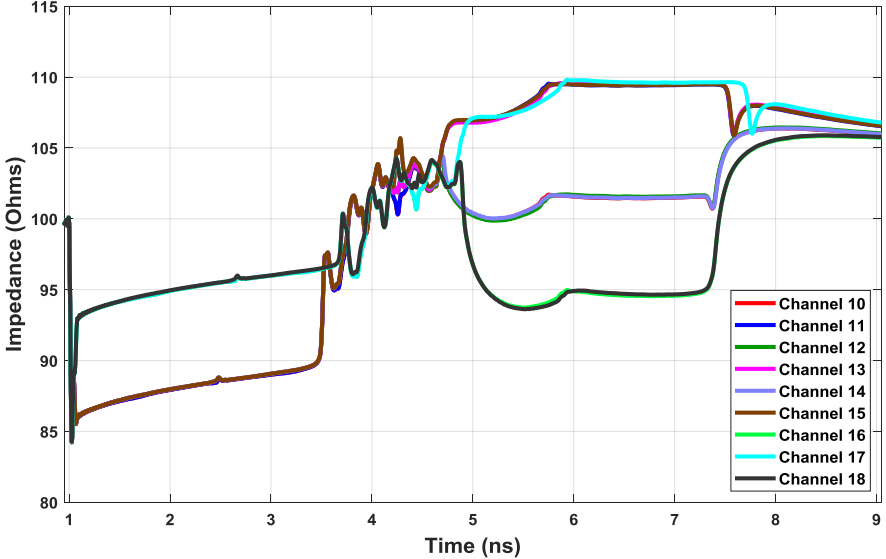
Trace 2 = Trace impedance on RAR side

Differential Impedance

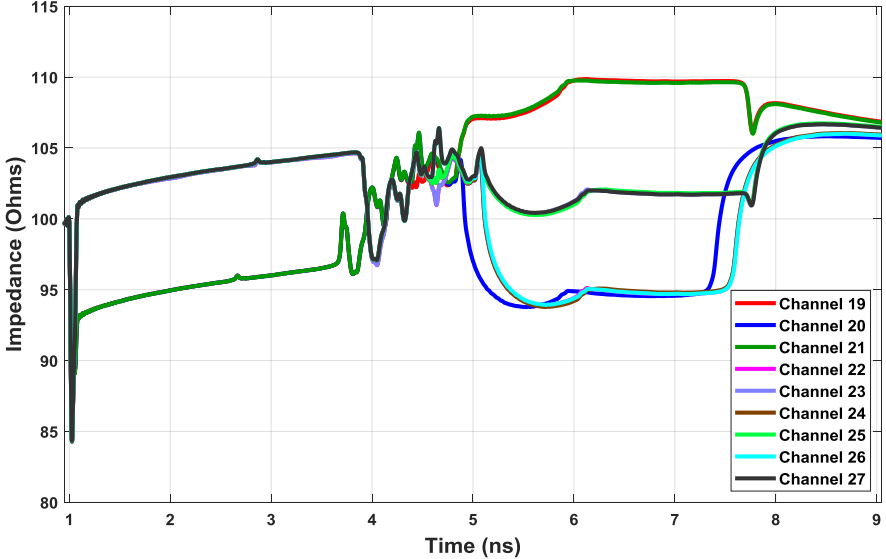
Channels 1-9 - Differential Impedance
Risetime = 15 ps (20-80%)



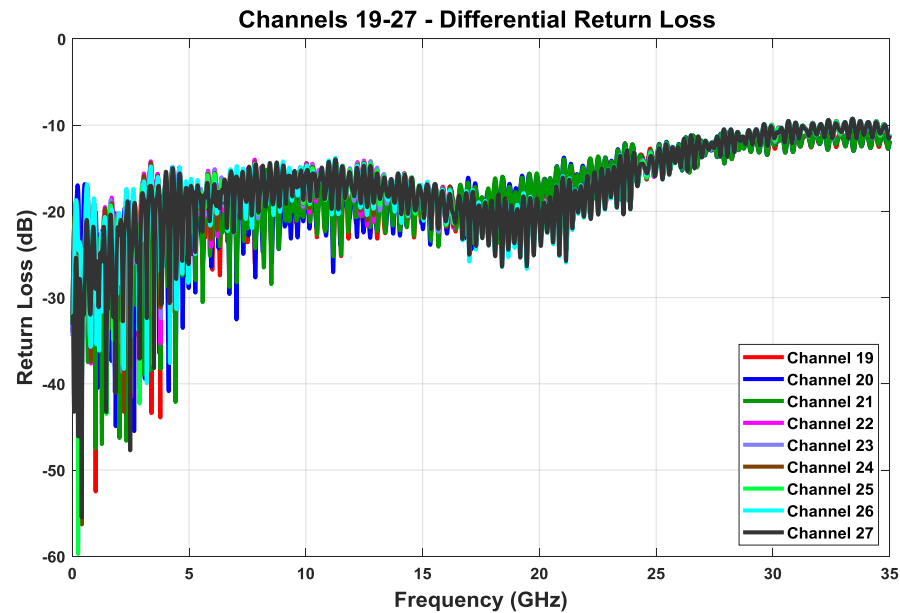
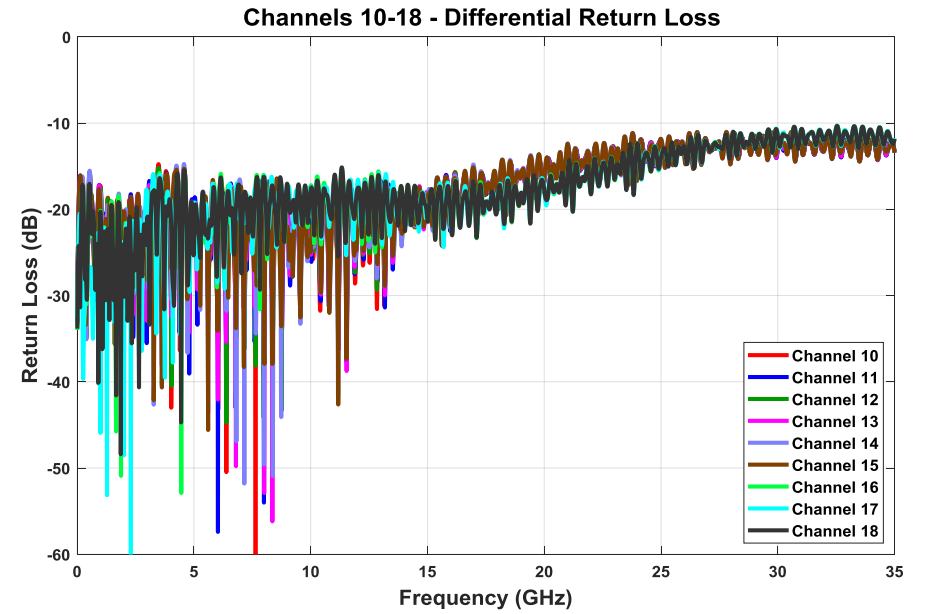
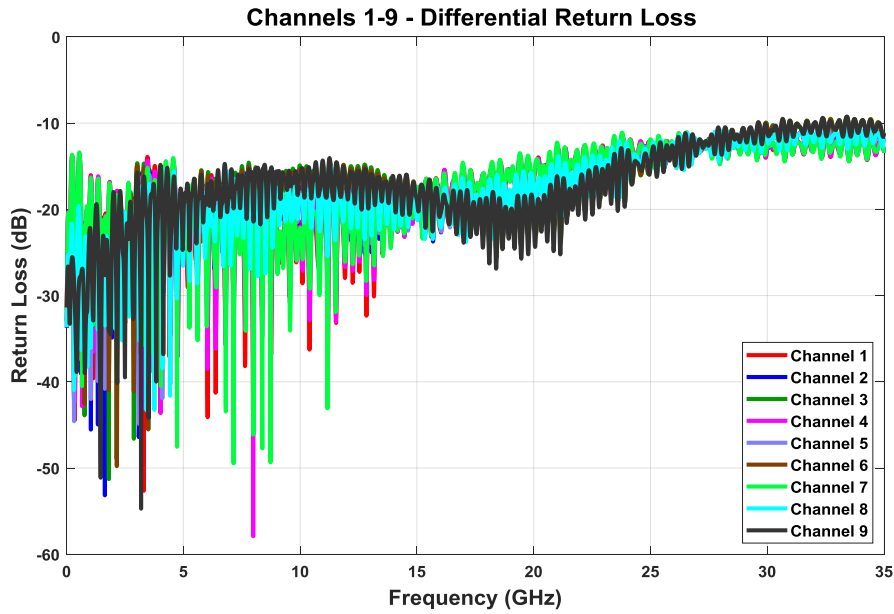
Channels 10-18 - Differential Impedance
Risetime = 15 ps (20-80%)



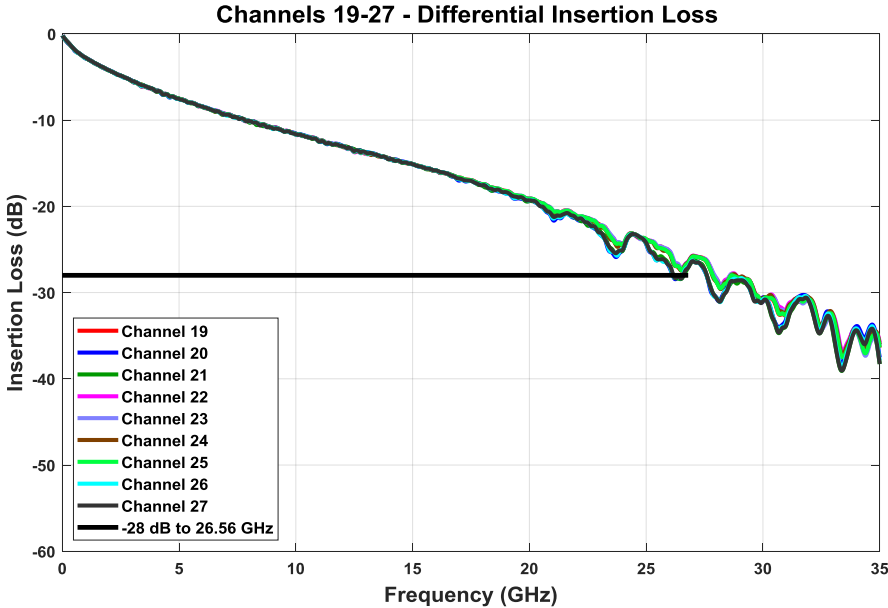
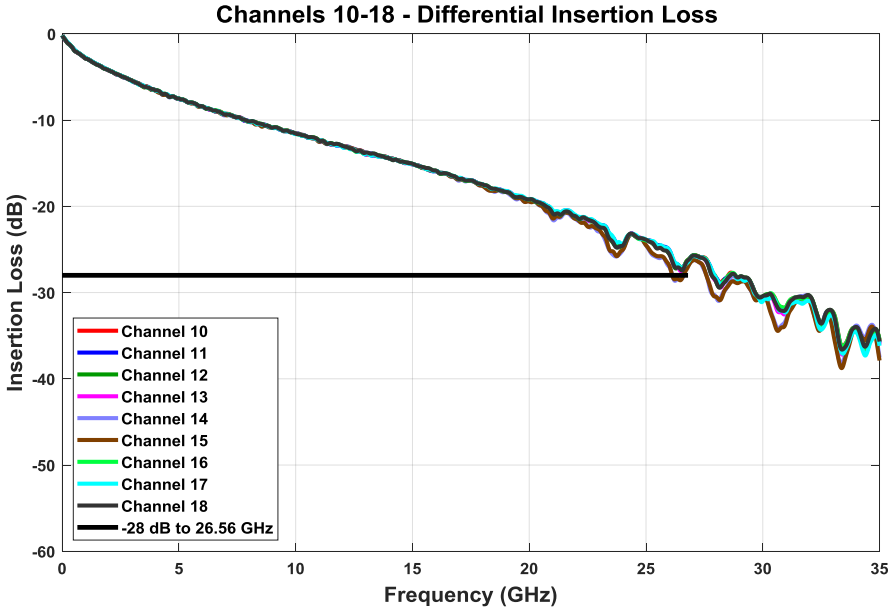
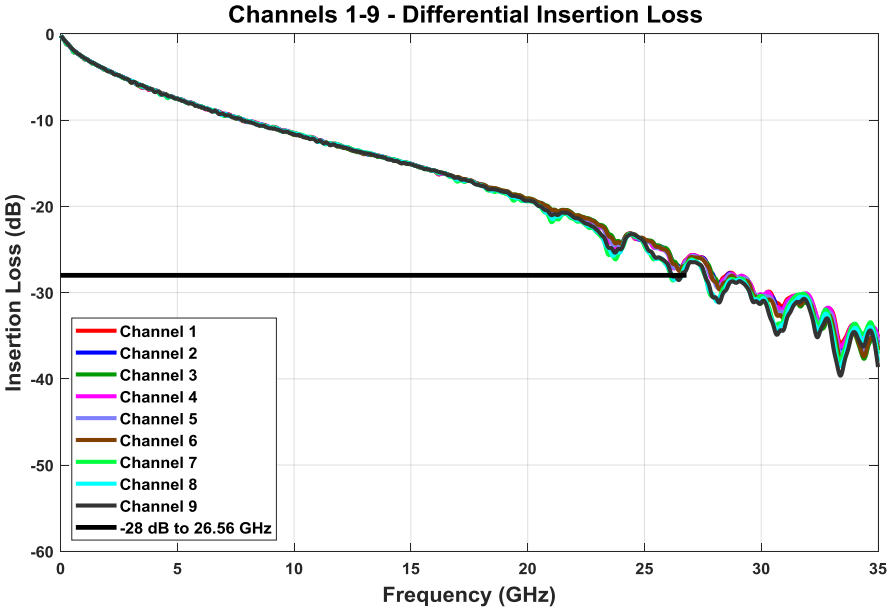
Channels 19-27 - Differential Impedance
Risetime = 15 ps (20-80%)



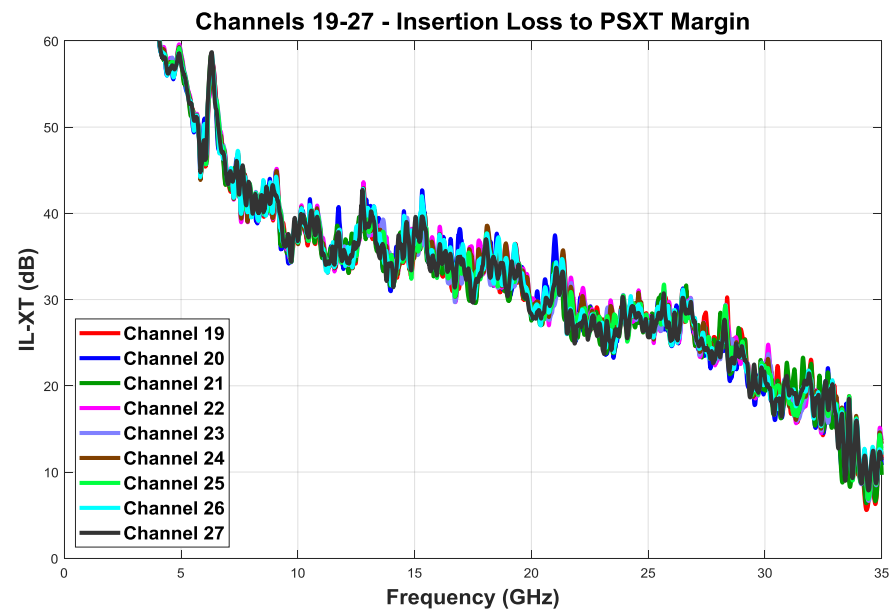
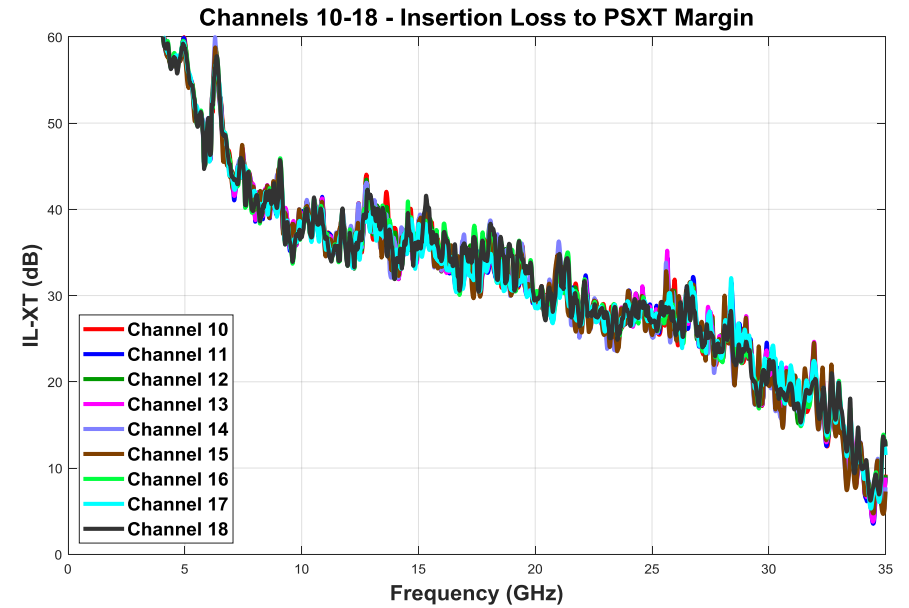
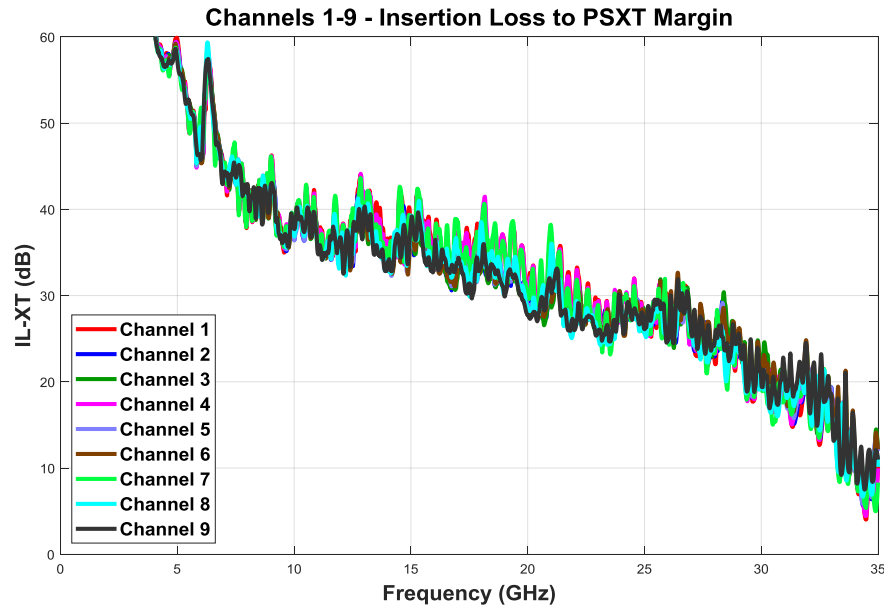
Differential Return Loss



Differential Insertion Loss



Insertion Loss to PSXT Margin



COM Results – 20-Tap DFE

	12	25	30
Ch. 1	3.62	3.38	2.83
Ch. 2	3.96	3.78	3.02
Ch. 3	3.92	3.69	3.07
Ch. 4	3.45	3.49	2.85
Ch. 5	3.94	3.78	2.82
Ch. 6	3.96	3.81	2.85
Ch. 7	2.88	2.90	2.14
Ch. 8	3.22	3.12	2.25
Ch. 9	3.54	3.38	2.37

	12	25	30
Ch. 10	3.78	3.58	2.95
Ch. 11	4.07	3.57	3.01
Ch. 12	3.62	3.74	2.87
Ch. 13	3.57	3.53	2.90
Ch. 14	3.00	3.07	2.23
Ch. 15	3.30	3.21	2.34
Ch. 16	3.84	3.49	2.89
Ch. 17	4.05	3.64	2.97
Ch. 18	3.69	3.43	2.72

	12	25	30
Ch. 19	3.88	3.53	2.87
Ch. 20	3.14	3.04	2.16
Ch. 21	3.32	3.27	2.33
Ch. 22	3.73	3.57	2.91
Ch. 23	3.97	3.70	2.94
Ch. 24	3.80	3.26	2.71
Ch. 25	3.89	3.36	2.93
Ch. 26	3.14	3.12	2.33
Ch. 27	3.38	3.30	2.35

12, 25, & 30 are the package lengths in mm.

Trace Impedance Tolerance Comparison

	12	25	30
Ch. 1	3.62	3.38	2.83
Ch. 2	3.96	3.78	3.02
Ch. 3	3.92	3.69	3.07
Ch. 10	3.78	3.58	2.95
Ch. 11	4.07	3.57	3.01
Ch. 16	3.84	3.49	2.89
Ch. 17	4.05	3.64	2.97
Ch. 22	3.73	3.57	2.91
Ch. 23	3.97	3.70	2.94

	Trace 1	Conn	Trace 2
Ch. 1	85	0	85
Ch. 2	92.5	0	92.5
Ch. 3	100	0	100
Ch. 10	85	0	92.5
Ch. 11	85	0	100
Ch. 16	92.5	0	85
Ch. 17	92.5	0	100
Ch. 22	100	0	85
Ch. 23	100	0	92.5

0 mm connector de-mate

Trace Impedance Tolerance Comparison

	12	25	30
Ch. 4	3.45	3.49	2.85
Ch. 5	3.94	3.78	2.82
Ch. 6	3.96	3.81	2.85
Ch. 12	3.62	3.74	2.87
Ch. 13	3.57	3.53	2.90
Ch. 18	3.69	3.43	2.72
Ch. 19	3.88	3.53	2.87
Ch. 24	3.80	3.26	2.71
Ch. 25	3.89	3.36	2.93

	Trace 1	Conn	Trace 2
Ch. 4	85	0.5	85
Ch. 5	92.5	0.5	92.5
Ch. 6	100	0.5	100
Ch. 12	85	0.5	92.5
Ch. 13	85	0.5	100
Ch. 18	92.5	0.5	85
Ch. 19	92.5	0.5	100
Ch. 24	100	0.5	85
Ch. 25	100	0.5	92.5

0.5 mm connector de-mate

Trace Impedance Tolerance Comparison

	12	25	30
Ch. 7	2.88	2.90	2.14
Ch. 8	3.22	3.12	2.25
Ch. 9	3.54	3.38	2.37
Ch. 14	3.00	3.07	2.23
Ch. 15	3.30	3.21	2.34
Ch. 20	3.14	3.04	2.16
Ch. 21	3.32	3.27	2.33
Ch. 26	3.14	3.12	2.33
Ch. 27	3.38	3.30	2.35

	Trace 1	Conn	Trace 2
Ch. 7	85	1	85
Ch. 8	92.5	1	92.5
Ch. 9	100	1	100
Ch. 14	85	1	92.5
Ch. 15	85	1	100
Ch. 20	92.5	1	85
Ch. 21	92.5	1	100
Ch. 26	100	1	85
Ch. 27	100	1	92.5

1 mm connector de-mate

Chassis Tolerance Comparison

	12	25	30		Trace 1	Conn	Trace 2	
Ch. 1	3.62	3.38	2.83		Ch. 1	85	0	85
Ch. 4	3.45	3.49	2.85		Ch. 4	85	0.5	85
Ch. 7	2.88	2.90	2.14		Ch. 7	85	1	85
Ch. 2	3.96	3.78	3.02		Ch. 2	92.5	0	92.5
Ch. 5	3.94	3.78	2.82		Ch. 5	92.5	0.5	92.5
Ch. 8	3.22	3.12	2.25		Ch. 8	92.5	1	92.5
Ch. 3	3.92	3.69	3.07		Ch. 3	100	0	100
Ch. 6	3.96	3.81	2.85		Ch. 6	100	0.5	100
Ch. 9	3.54	3.38	2.37		Ch. 9	100	1	100

Chassis Tolerance Comparison

	12	25	30		Trace 1	Conn	Trace 2	
Ch. 10	3.78	3.58	2.95		Ch. 10	85	0	92.5
Ch. 12	3.62	3.74	2.87		Ch. 12	85	0.5	92.5
Ch. 14	3.00	3.07	2.23		Ch. 14	85	1	92.5
Ch. 16	3.84	3.49	2.89		Ch. 16	92.5	0	85
Ch. 18	3.69	3.43	2.72		Ch. 18	92.5	0.5	85
Ch. 20	3.14	3.04	2.16		Ch. 20	92.5	1	85

Chassis Tolerance Comparison

	12	25	30		Trace 1	Conn	Trace 2	
Ch. 11	4.07	3.57	3.01		Ch. 11	85	0	100
Ch. 13	3.57	3.53	2.90		Ch. 13	85	0.5	100
Ch. 15	3.30	3.21	2.34		Ch. 15	85	1	100
Ch. 22	3.73	3.57	2.91		Ch. 22	100	0	85
Ch. 24	3.80	3.26	2.71		Ch. 24	100	0.5	85
Ch. 26	3.14	3.12	2.33		Ch. 26	100	1	85

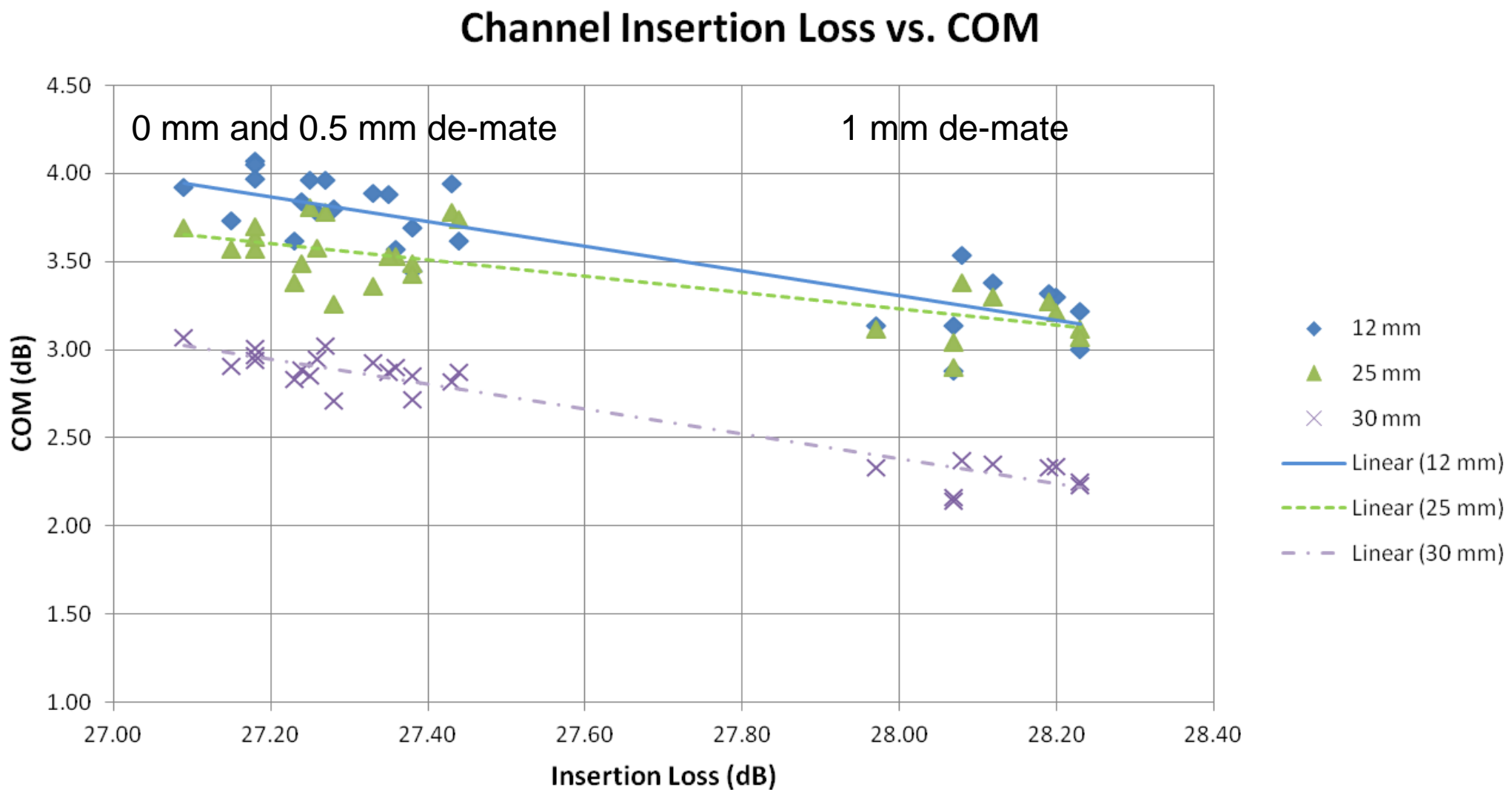
Chassis Tolerance Comparison

	12	25	30		Trace 1	Conn	Trace 2	
Ch. 17	4.05	3.64	2.97		Ch. 17	92.5	0	100
Ch. 19	3.88	3.53	2.87		Ch. 19	92.5	0.5	100
Ch. 21	3.73	3.57	2.91		Ch. 21	92.5	1	100
Ch. 23	3.97	3.70	2.94		Ch. 23	100	0	92.5
Ch. 25	3.89	3.36	2.93		Ch. 25	100	0.5	92.5
Ch. 27	3.38	3.30	2.35		Ch. 27	100	1	92.5

COM vs. Channel Insertion Loss

Channel #	Channel IL	12	25	30
1	27.23	3.62	3.38	2.83
2	27.27	3.96	3.78	3.02
3	27.09	3.92	3.69	3.07
4	27.38	3.45	3.49	2.85
5	27.43	3.94	3.78	2.82
6	27.25	3.96	3.81	2.85
7	28.07	2.88	2.90	2.14
8	28.23	3.22	3.12	2.25
9	28.08	3.54	3.38	2.37
10	27.26	3.78	3.58	2.95
11	27.18	4.07	3.57	3.01
12	27.44	3.62	3.74	2.87
13	27.36	3.57	3.53	2.90
14	28.23	3.00	3.07	2.23
15	28.20	3.30	3.21	2.34
16	27.24	3.84	3.49	2.89
17	27.18	4.05	3.64	2.97
18	27.38	3.69	3.43	2.72
19	27.35	3.88	3.53	2.87
20	28.07	3.14	3.04	2.16
21	28.19	3.32	3.27	2.33
22	27.15	3.73	3.57	2.91
23	27.18	3.97	3.70	2.94
24	27.28	3.80	3.26	2.71
25	27.33	3.89	3.36	2.93
26	27.97	3.14	3.12	2.33
27	28.12	3.38	3.30	2.35

COM vs. Channel Insertion Loss



Conclusions

- Chassis tolerance can affect COM by 0.3-0.8 dB.
 - With the 1 mm de-mate, the insertion loss of the channel increases by about 1 dB.
- Trace impedance tolerance can affect COM by 0.3-0.5 dB.
 - To get the same amount of loss between the three different impedance traces, the higher impedance traces are longer than the shorter impedance traces.
 - 85 ohm trace – 8” (0.2032 m)
 - 92.5 ohm trace – 8.6” (0.2184 m)
 - 100 ohm trace – 9.25” (0.2350 m)
- COM appears to be very sensitive to insertion loss right at the 28 dB channel loss target.

COM Settings

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.3e-4 1.3e-4]	nF	[TX RX]
z_p select	[3]		[test cases to run]
z_p (TX)	[12 30 25]	mm	[test cases]
z_p (NEXT)	[12 30 25]	mm	[test cases]
z_p (FEXT)	[12 30 25]	mm	[test cases]
z_p (RX)	[12 30 25]	mm	[test cases]
C_p	[1.1e-4 1.1e-4]	nF	[TX RX]
C_v	[0 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.41	V	
A_fe	0.41	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.025:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		[min:step:max]
c(-3)	[0]		[min:step:max]
c(-4)	[0]		[min:step:max]
c(1)	[-0.3:0.025:0]		[min:step:max]
N_b	20	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	
Include PCB	0		logical
ffe_enable	1		logical
ffe_pre_tap_length	3		UI
ffe_tap_step_size	0.01		UI
ffe_main_cursor	1		
ffe_post_tap1_max	0.5		
ffe_tapn_max	0.125		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	FFE3_DFE20_results_(date)	
SAVE_FIGURES	1	logical
Port Order	[1 3 2 4]	
RUNTAG	FFE3_DFE20	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
DER_0	1.00E-04	
Include PCB	0	Value
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR Butterworth	1	logical
beta_x	1.70E+09	
rho_x	0.18	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	92.5	Ohm (tdr sel)
Table 92-12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 4.114e-04 2.547e-04]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	110	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

COM version: com_ieee8023_93a_251.m

- Thanks.
- Questions?